Mechanisms Underlying the Bidirectional V_T Shift after Negative Bias Temperature Instability Stress in Carbon-Doped Fully Recessed AlGaIn/GaN MIS-HEMTs

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Abstract— In this brief, we investigate the bidirectional threshold voltage drift (ΔV_T) following negative bias temperature instability (NBTI) stress in Carbon-doped fully recessed AlGaIn/GaN MIS-HEMTs. Several stress conditions were applied at different: *i)* gate bias ($V_{GS,STR}$); *ii)* stress time (t_{STR}); and *iii)* temperature (T). Both negative and positive ΔV_T (thermally activated with different activation energies, E_A) were observed depending on the magnitude of $V_{GS,STR}$. In accordance with the literature, observed $\Delta V_T < 0$ V ($E_A \approx 0.5$ eV) under moderate stress is attributed to the emission of electrons from oxide and interface traps. Instead, $\Delta V_T > 0$ V ($E_A \approx 0.9$ eV) under high stress is attributed to the increased negatively ionized acceptor trap density in the buffer associated with Carbon doping.

Index Terms— AlGaIn/GaN MIS-HEMTs, NBTI, Threshold Voltage Instability, Carbon Doping.

I. INTRODUCTION

GALLIUM Nitride (GaN)-based devices have gained huge popularity in recent years thanks to their outstanding performance in terms of power density and operating frequency compared to Si counterparts for power switching and RF applications [1]. Conventional GaN High Electron Mobility Transistors (HEMTs) are normally-on devices, while normally-off operation is desirable for commercial devices. To this end, research and industry efforts have been focused towards the development of fully recessed metal-insulator-semiconductor (MIS)-HEMTs [2]. However, the presence of a gate oxide and the associated defect-prone oxide/semiconductor interface

leads to threshold voltage (V_T) instability, severely impacting device stability and operation [2]. Assessing the V_T stability after negative bias temperature stress (NBTI) is important even in normally-off HEMTs, since $V_{GS} \ll V_T$ is required to avoid false turn-on when devices are pulsed at large drain voltages [3]. Moreover, if large, negative gate biases are adopted, NBTI tests are a proxy for OFF-state conditions (experienced by the device under pulse-mode operation) as similar, large values of drain-gate voltage can be achieved with both stress setups.

Different NBTI trends were observed in the literature that can be categorized as follows depending on the sign of the observed V_T shifts (ΔV_T): 1) $\Delta V_T < 0$ V [4]–[6]; 2) $\Delta V_T > 0$ V [3], [7], [8]; and 3) ΔV_T of both signs, depending on device type or stress conditions [9], [10]. While $\Delta V_T < 0$ V following NBTI is commonly attributed to the emission of electrons from traps in the gate oxide or at the interface with the semiconductor, a univocal explanation for $\Delta V_T > 0$ V as a consequence of high negative gate bias stress is still lacking. Moreover, $\Delta V_T > 0$ was also observed in off-state operating conditions, attributed to a hole generation mechanism [8], [11]. For this reason, it is worthwhile performing an in-depth analysis of V_T stability after NBTI stress by exploring a wide range of stress conditions to provide a comprehensive explanation for the observed results.

In this brief, we report on an extensive characterization of V_T stability in fully recessed AlGaIn/GaN MIS-HEMTs under different stress conditions in terms of: *i)* gate bias ($V_{GS,STR}$); *ii)* stress time (t_{STR}); and *iii)* temperature (T). Depending on the $V_{GS,STR}$ magnitude, we observed bidirectional ΔV_T (i.e., negative, and positive) and thermally activated with different activation energies, E_A . Particularly, we observed $\Delta V_T < 0$ V (with $E_A \approx 0.5$ eV) under moderate stress (i.e., $V_{GS,STR} = -7$ V) and $\Delta V_T > 0$ V (with $E_A \approx 0.9$ eV) with high stress (i.e., $V_{GS,STR} = -17$ V). The former behavior ($\Delta V_T < 0$ V) can mainly be attributed to the emission of electrons from traps located in the gate oxide and/or at the interface with the semiconductor [4], [5], [9]. The latter behavior ($\Delta V_T > 0$ V), instead, can be

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Fig. 1. Sketch of the cross-section of the fully recessed AlGaIn/GaN MIS-HEMT devices under study (not to scale). Dimensions are in μm .

attributed to the increased negatively ionized acceptor traps in the buffer.

II. DEVICES DESCRIPTION

Tested devices were fully recessed AlGaIn/GaN MIS-HEMTs grown by metal-organic chemical vapor deposition on a Si(111) p-type substrate with $1\ \mu\text{m}$ gate length. A schematic view of the device cross-section is shown in Fig. 1. The channel is composed of a Low-Carbon-doped (LC, $\sim 10^{16}\ \text{cm}^{-3}$) GaN layer of $0.3\ \mu\text{m}$. The GaN buffer layer instead is $4.7\ \mu\text{m}$ thick and is highly C-doped ($\sim 10^{18}\ \text{cm}^{-3}$). The AlGaIn barrier layer is $20\ \text{nm}$ with 25% Al concentration. The gate dielectric ($20\ \text{nm}\ \text{Al}_2\text{O}_3$) is fully recessed and partially penetrates into the LC GaN (typical penetration depth is around $10\ \text{nm}$). This allows to effectively suppress the 2DEG when no gate bias is applied thus obtaining $V_T > 0\ \text{V}$. Ohmic contacts were formed by Ti/Al-based metallization defined by means of a liftoff process [12]. Nominal 2DEG density and mobility are $8 \times 10^{12}\ \text{cm}^{-2}$ and $1500\ \text{cm}^2/\text{Vs}$, respectively. Representative transfer (I_D - V_{GS}) and output (I_D - V_{DS}) curves of these devices are shown in Fig. 2 (blue squares). The characterization was performed on different devices with good measurement repeatability.

III. STRESS MEASUREMENT METHODOLOGY

The NBTI stress characterization was carried out by means of a Keithley 4200 semiconductor parameter analyzer, with a thermal chuck employed for setting the device-under-test (DUT) temperature during the measurements. When applying the gate stress bias, drain and source contacts were grounded. The substrate contact was grounded by wiring the thermal chuck to the ground signal applied to the source contact. During stress, the device is periodically turned-on by means of a stairway-like gate signal to monitor the V_T evolution [6]. To this end, the gate is swept between $-2\ \text{V}$ and $2\ \text{V}$ with steps of $0.1\ \text{V}$ each lasting $10\ \mu\text{s}$, while the drain is fixed to $0.1\ \text{V}$. In correspondence of each step, the drain current (I_D) and gate voltage (V_{GS}) are acquired, allowing the reconstruction of the I_D - V_{GS} characteristics. Since the induced stress was monitored for up to $t_{STR} = 1000\ \text{s}$, the gate stairway signal was applied to the DUT at logarithmically-spaced time instants to ensure a uniform distribution of V_T acquisitions [13]. The chosen I_D - V_{GS}

Fig. 2. (a) Transfer (I_D - V_{GS}) characteristics of tested devices for two different V_{DS} bias (see legend). (b) Output (I_D - V_{DS}) characteristics of tested devices for five different V_{GS} bias.

sweep rate represents the best compromise between speed and accuracy, since the short time required for the V_T measurement minimizes the fast recovery between stress phases [6] but still provides enough samples for a correct I_D - V_{GS} acquisition. For each I_D - V_{GS} , the V_T was extracted with the constant-current method ($I_D = 200\ \mu\text{A}$). ΔV_T is then simply calculated as $(V_T - V_{T0})$ with the reference V_{T0} acquired before starting the stress phase from a fresh I_D - V_{GS} curve. To determine the time constants of the V_T transients to be used in the Arrhenius plots (to extract the activation energy, E_A), the curves were fitted by means of stretched exponential functions and the relative time constants were extracted in correspondence of the peak in the $dV_T/d\log t_{STR}$ signals.

IV. EXPERIMENTAL RESULTS

Two different stress conditions were investigated in this work, i.e., moderate ($V_{GS,STR} = -7\ \text{V}$) and high stress ($V_{GS,STR} = -17\ \text{V}$), observing ΔV_T of both signs. The measured ΔV_T evolution is shown in Figs. 3 and 4 for the moderate and high stress conditions, respectively. Fig. 3a) shows that, for moderate stress, V_T drifts to the negative direction (i.e., becomes less than V_{T0}) with a saturation ΔV_T value of about $-0.8\ \text{V}$ to $-1\ \text{V}$ at $t_{STR} = 1000\ \text{s}$. This effect is widely reported in the literature and is attributed to the emission of electrons from traps located in the gate oxide or at the interface with the semiconductor [5], [9], which is known to be a thermally activated process [4]. In the devices tested in this work, for this process $E_A \approx 0.5\ \text{eV}$ was estimated, see Fig. 3b). The time window considered for the time constants extraction was the full stress measurement range, i.e., $1\ \text{ms}$ - $1000\ \text{s}$. The $\Delta V_T < 0\ \text{V}$ process can also be attributed to the de-ionization of acceptor traps in the buffer (related to C-doping) as a consequence of the applied negative gate stress [6].

Conversely, Fig. 4a) shows that the high stress condition causes V_T to drift in the positive direction (i.e., V_T becomes larger than V_{T0}). The positive drift is found to be weakly dependent on temperature for t_{STR} in the range of $1\ \text{ms}$ to $1\ \text{s}$, whereas it exhibits a clear temperature-dependent component for $t_{STR} > 1\ \text{s}$. The E_A of the latter process was found to be $\approx 0.9\ \text{eV}$, see Fig. 4b). The time window considered for the extraction of the time constants in the Arrhenius plot in this case was limited to the range for which an appreciable temperature dependence was observed, i.e., $1\ \text{s}$ - $1000\ \text{s}$. Note that because no appreciable V_T shift was observed for $t_{STR} > 1\ \text{s}$ at $T \leq 50\ ^\circ\text{C}$, extraction of E_A from the linear fitting excluded data in this temperature range.

Fig. 3. a) Measured ΔV_T vs t_{STR} for different temperatures (see legend) at $V_{GS,STR} = -7$ V. b) Arrhenius plot of the stress data (symbols). The linear fitting (dashed line) gives an activation energy $E_A \approx 0.5$ eV.

Fig. 4. a) Measured ΔV_T vs t_{STR} for different temperatures (see legend) at $V_{GS,STR} = -17$ V. b) Arrhenius plot of the stress data (symbols). The linear fitting (dashed line) gives an activation energy $E_A \approx 0.9$ eV.

Fig. 5. Measured I_G - V_{GS} curves for different temperatures (see legend) below threshold.

Fig. 6. I_G vs reciprocal of thermal energy to extract the activation energy for the process of $E_A \approx 0.35$ eV, which was found to be independent of applied $V_{GS,STR}$.

The fast $\Delta V_T > 0$ V can be attributed to the capture of electrons injected by the gate terminal in the oxide [7], whereas the thermally activated increase is induced by a slower process with $E_A \approx 0.9$ eV.

To further investigate on the origin of this 0.9-eV thermally activated positive V_T shift, we report the gate leakage current I_G vs $V_{GS,STR}$ in Fig. 5. We found that for both $V_{GS,STR} = -7$ V and -17 V, the gate leakage current is thermally activated with $E_A \approx 0.35$ eV, as shown in Fig. 6. The different activation energy of I_G compared to that of ΔV_T indicates that gate leakage is not the root cause for the temperature dependence of ΔV_T . $E_A \approx 0.9$ eV actually indicates that the observed behavior is likely caused by the dynamics of buffer acceptor traps (related to C-doping) that are energetically located at about 0.9 eV from GaN valence band edge [14]. In fact, buffer traps are known to strongly affect

the behavior of AlGaIn/GaN power MIS-HEMTs, as also supported by numerical simulations [15]–[20]. In this context, the thermally activated positive ΔV_T (with $E_A \approx 0.9$ eV) under high $|V_{GS,STR}|$ can be attributed to hole emission from the 0.9-eV C_N acceptor traps and the consequent increase in negatively ionized C_N levels. As suggested by device simulations in [19], we speculate that the emitted holes attracted at the dielectric/channel interface can recombine with electrons injected from the gate terminal. However, this phenomenon needs further investigation and will be subject of future work.

V. CONCLUSIONS

An in-depth experimental investigation of NBTI behavior in fully recessed AlGaIn/GaN MIS-HEMTs has been presented. Results obtained by means of fast I_D - V_{GS} characterization under

relatively low negative gate bias stress (i.e., $V_{GS,STR} = -7$ V) revealed conventional negative V_T drift associated to the thermally activated emission of electron from interface and/or oxide traps. This process was characterized by an activation energy of about 0.5 eV. Conversely, the positive V_T shift observed for $V_{GS,STR} = -17$ V for long stress time was ascribed to the increased negatively ionized acceptor trap density in the buffer, supported by the correlation between the extracted activation energy and the widely accepted energy level of Carbon doping related traps, both of about 0.9 eV.

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