electronics

MDPI

Article

Cryo-CMOS Multi-Frequency Modulator for 2-Qubit Controller

Alessandro Badiali [1,2] and Mattia Borgarino [2,3,*]

[1] Department of Electrical, Computer and Biomedical Engineering, University of Pavia, 27100 Pavia, Italy; alessandro.badiali01@universitadipavia.it
[2] Enzo Ferrari Engineering Department, University of Modena and Reggio Emilia, 41125 Modena, Italy
[3] Consorzio Nazionale Interuniversitario per le Telecomunicazioni (CNIT), 43124 Parma, Italy
* Correspondence: mattia.borgarino@unimore.it; Tel.: +39-059-205-6168

Abstract: This paper addresses the design of a CMOS modulator to control two quantum bits. The proposed architecture offers several advantages that are addressed and discussed in this paper. The proposed architecture is investigated through both mathematical modeling and Verilog simulations. Moreover, the circuit was designed using the cryogenic Design Kit of the 130 nm SiGe BiCMOS technology of the IHP foundry. The observed agreement between the modeling, Verilog, and transistor-level simulations proves the physical feasibility of the proposed architecture.

Keywords: quantum computing; cryogenic electronics; circuit design; RF CMOS; qubit control; SSB modulation

1. Introduction

Quantum computing represents a revolutionary paradigm of computability aimed at exploiting quantum algorithms, which are based on quantum mechanical phenomena, such as the superposition of states and entanglement, to solve problems not efficiently addressable with classical algorithms [1–3]. The most promising problems of practical interest are mathematically demanding, involve small datasets, and allow for the solving of quantum algorithms with exponential speed-up [4]. Prime number factorization, which is efficiently performed by quantum Shor's algorithm in a polynomial time [5], is a historical example of such a class of mathematical problems. To preserve their speed-up, quantum algorithms should run on a quantum microprocessor that essentially is an array of quantum bits, or qubits for short. During the execution of a quantum algorithm, qubits are entangled and/or manipulated to form quantum gates, which are the elementary bricks of the quantum processor. Entanglement also allows for the formation of logic qubits, which are useful for minimizing errors [6].

Any two-state quantum physical system, whether intrinsic, a subset, or engineered, can encode a qubit [3,6]. Several solid-state technologies are available for implementing a qubit, with superconducting qubits being the most widely adopted nowadays. The spin and charge of an electron confined in a Quantum Dot (QD) may also be exploited to manufacture a solid-state qubit. Historically, the single electron spin was the first contemplated option for quantum computation [7]. Today, QD-based qubits remain promising candidates by virtue of their scalability, small footprint, long coherence time, and compatibility with Complementary Metal-Oxide-Semiconductor (CMOS) microelectronic technology [8–11].

Microwave pulses enable the manipulation of superconducting and electron spin qubits. The frequency of the microwave pulse should match the resonance frequency $f_{R,i}$ ($i = 1, \ldots, N$) of the wanted quantum transition corresponding to the quantum gate to reproduce [12]. A common approach, widely adopted in research laboratories, involves generating microwave pulses using rack-mount instrumentation operating at room temperature. However, since a qubit must operate at deep-cryogenic temperatures (10 Mk–4 K) to preserve its quantum peculiarity, these pulses are then transmitted to the qubits via

check for updates

Citation: Badiali, A.; Borgarino, M. Cryo-CMOS Multi-Frequency Modulator for 2-Qubit Controller. *Electronics* **2024**, *13*, 2546. https://doi.org/10.3390/electronics13132546

Academic Editors: Yahya M. Meziani and Andrea Delgado

Received: 14 May 2024
Revised: 20 June 2024
Accepted: 26 June 2024
Published: 28 June 2024

microwave cables [13]. Regrettably, the cables are not only bulky, but they also convey a considerable amount of heat into the cryostat hosting the qubits. Sustaining cryogenic temperatures under such circumstances may prove challenging. These difficulties and limitations pose significant hurdles, especially considering that the targeted number of qubits for the next decade is in the range of 100,000 [14].

Miniaturized microwave sources, tailored as cryogenic integrated circuits, appear to be very promising for the fabrication of solid-state quantum microprocessors. They can indeed be placed close to the qubits, thus alleviating, if not entirely avoiding, the aforementioned issues. The ultimate goal is the integration of the qubits along with the control and read-out circuitry on the same silicon die. The actual state-of-the-art envisages a chipset consisting of the quantum chip carrying the qubits and the classical chip carrying the microwave source. Several options are possible. They can be Josephson junction-based superconducting circuits [15,16] or cryogenic CMOS Radio Frequency Integrated Circuits (RFICs) [11,17,18]. The former allow for ultimate performance in terms of dissipated power but at the expense of a larger footprint, and the latter consumes a smaller silicon area, but they dissipate more. What makes the CMOS RFICs particularly appealing is their straightforward compatibility with the CMOS microelectronic technology. Photonics microwaves may be a further possible approach [19]. This paper reports on a cryogenic CMOS modulator.

Regardless of the specific way of implementing the microwave sources, the microwave pulses must be applied for a precise time interval to execute a quantum gate [12], and they undergo Amplitude Modulation (AM). A straightforward AM modulator generates a spectrum that exhibits the carrier and the Double Side Band (DSB) of the modulating envelope. Feasible as a balanced AM modulator [20], a Double-Side Band Suppressed-Carrier (DSB-SC) modulator suppresses the carrier but not the DSB. This is not acceptable, because the modulated microwave pulse can address several resonance frequencies simultaneously, as depicted in Figure 1. This figure shows that a Lower or Upper Single-Side Band (LSSB or USSB) modulator, whose fundamental building block diagram is shown in Figure 2, addresses only one single resonance frequency without interfering with the others. It is worth noticing that several cryogenic microwave RFICs adopt an SSB modulation scheme [11,18,21].

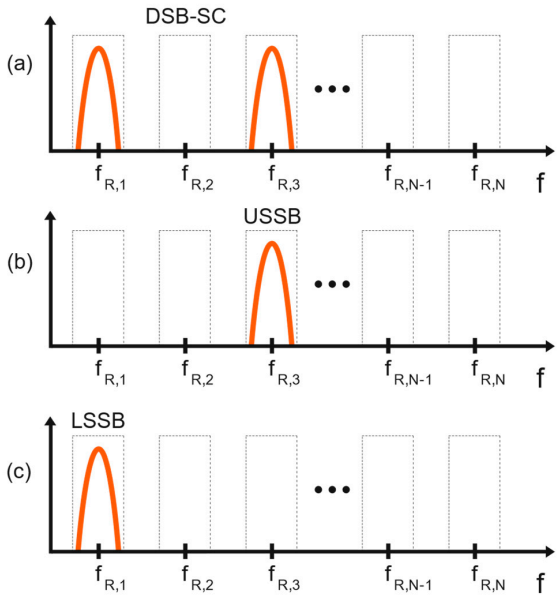


Figure 1. Quantum microprocessor as an array (dotted rectangles) of N resonance frequencies $f_{R,i}$ ($i = 1, \ldots N$) and microwave pulse spectra (red curves) for a DSB-SC (**a**), USSB (**b**), and LSSB (**c**) modulation scheme.

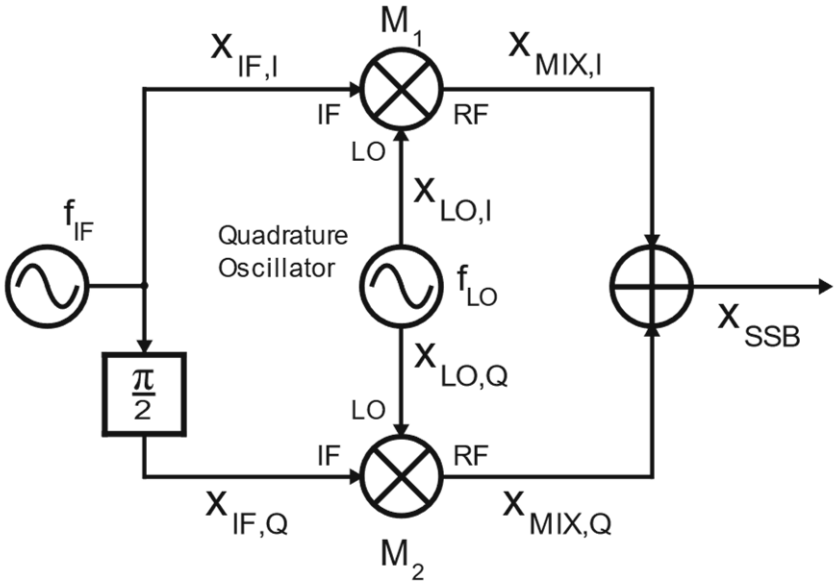


Figure 2. Building block diagram of a basic SSB modulator.

The mixer M_1 (M_2) receives, as inputs, the in-phase (quadrature) Local Oscillator (LO) carrier $x_{LO,I}$ ($x_{LO,Q}$) at frequency f_{LO} and the Intermediate Frequency (IF) modulating signal $x_{IF,I}$ ($x_{IF,Q}$) at frequency f_{IF}. A quadrature or Hilbert filter generates $x_{IF,Q}$ from $x_{IF,I}$. It is worth noting that the filter is physically feasible only with approximation, because its impulse response is an anti-causal signal [20]. Therefore, the use of the Hilbert filter should be avoided whenever possible. For this reason, a quadrature oscillator typically generates the LO carrier. The outputs $x_{MIX,I}$ and $x_{MIX,Q}$ of the two mixers are then algebraically summed to obtain an SSB modulated signal x_{SSB}.

This paper proposes a modulator, designed around a low-frequency USSB modulator and a frequency divider, for the control of two qubits. It is worth noting that one-qubit and two-qubit quantum gates form a universal set for quantum computing, with single-qubit rotations and two-qubit quantum gates being the most common [22].

This paper is organized as follows. Section 2 details the architecture and the mathematical analysis of the proposed modulator, along with its advantages. Sections 3–6 address the schematics and simulations of the circuits forming the proposed modulator. The circuits were designed using Cadence Virtuoso in the SG13G2 130 nm SiGe BiCMOS technology by IHP (Innovation for High-Performance Microelectronics) in Frankfurt am Oder, Germany. In particular, the recently released cryogenic Design Kit was used. In all designed circuits, the source and body terminals of the transistors are tied together to avoid the body effect. Apart from the schematics view, this is physically feasible, because the adopted technology is triple well. Section 7 reports on the simulations of the whole modulator. Finally, Section 8 draws conclusions and proposes future outlooks. All simulations were carried out at 4 K. No further temperatures were addressed, because the cryostat temperature is expected to be well controlled.

2. Architecture

Figure 3 depicts the building block diagram of the proposed modulator. It consists of a low-frequency USSB modulator followed by the higher frequency up-conversion mixer M_3. Two IF sinusoidal tones at frequency f_{IF1} and f_{IF2} allow for the control of two qubits. There are two possible ways to generate the IF signal x_{IF}, both involving amplitude modulation and the sum of signals. However, they differ in the execution order.

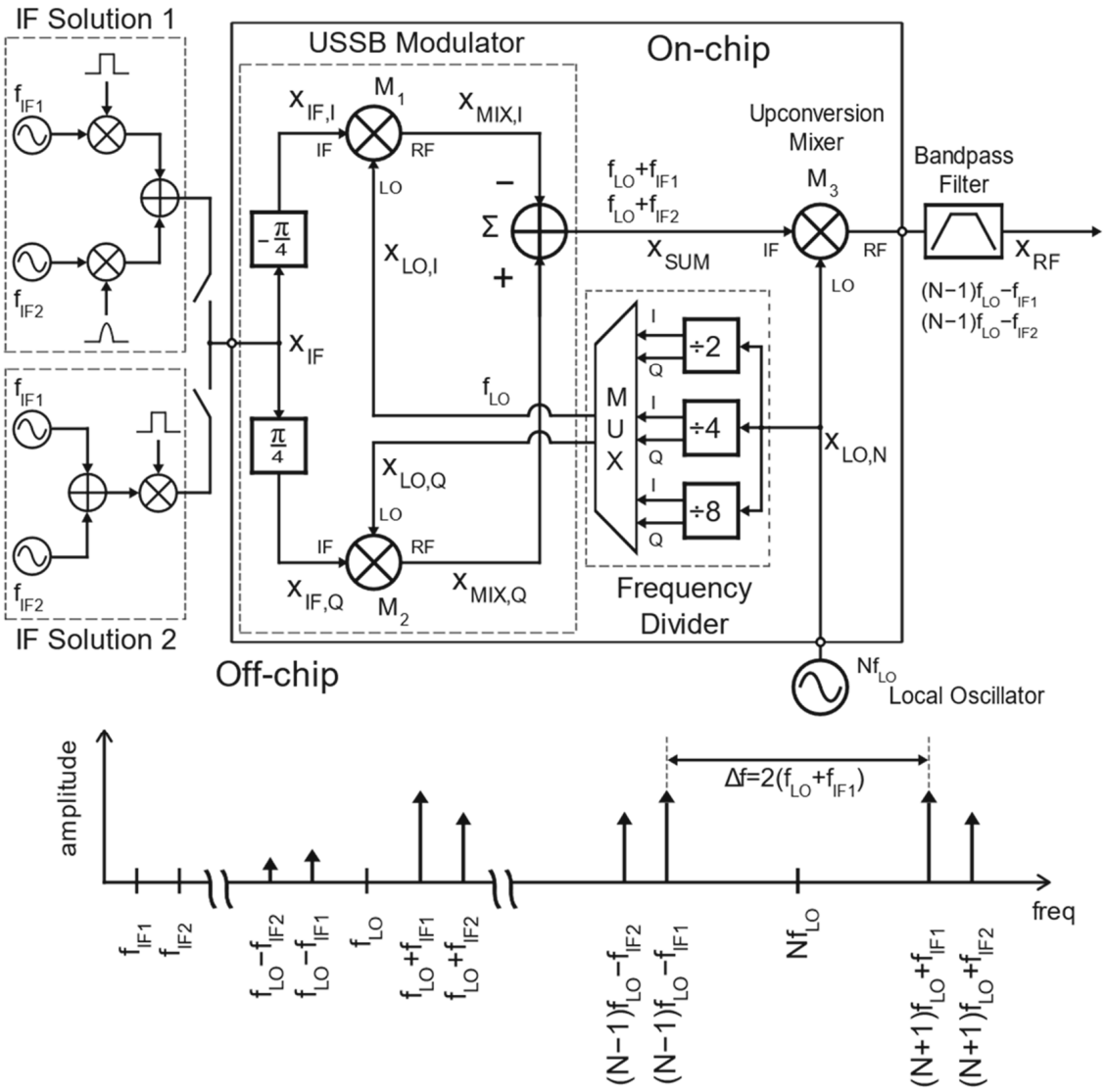


Figure 3. Building block diagram of the proposed modulator.

In Solution 1, each IF signal is first modulated and then added to the other modulated signal. Although this solution requires a modulator for each IF signal, it offers the advantage of allowing for the use of different envelopes for the two IF signals. This may be useful to minimize, by phase compensation when needed, the AC Stark shift of the resonance frequency [21].

On the other hand, Solution 2 first adds and then collectively modulates the IF signals. This solution utilizes only one modulator, but it forces the same envelope for both signals, reducing flexibility.

For the sake of simplicity, in the following analysis, it is assumed that the modulating signals are not applied and that all the mixers behave like a Gilbert multiplier [23,24]. It is worth pointing out that the mixer, conceived by Howard E. Jones in 1963 [25], and the Gilbert cell are different engines [26]. The Gilbert cell generates only second-order intermodulation products, whereas the mixer also generates intermodulation products of higher orders. Since the SSB modulator mainly exploits second-order intermodulation products, a simplified analysis treats a mixer as a multiplier.

Let the two IF signals be $A_{IF1}sin(2\pi f_{IF1}t)$ and $A_{IF2}sin(2\pi f_{IF2}t)$. This, therefore, results in the $x_{IF}(t)$ signal to be as follows:

$$x_{IF}(t) = A_{IF}[sin(2\pi f_{IF1}t) + sin(2\pi f_{IF2}t)] \quad (1)$$

The $\pm\pi/4$ phase shifters yield the two following signals, $x_{IF,I}(t)$ and $x_{IF,Q}(t)$:

$$x_{IF,I}(t) = A_{IF}\left[sin\left(2\pi f_{IF1}t - \frac{\pi}{4}\right) + sin\left(2\pi f_{IF2}t - \frac{\pi}{4}\right)\right] \quad (2)$$

$$x_{IF,Q}(t) = A_{IF}\left[sin\left(2\pi f_{IF1}t + \frac{\pi}{4}\right) + sin\left(2\pi f_{IF2}t + \frac{\pi}{4}\right)\right] \quad (3)$$

Equations (2) and (3) show that $x_{IF,I}(t)$ and $x_{IF,Q}(t)$ are in quadrature, because they exhibit a relative phase shift of $\pi/2$. Unlike the use of a single Hilbert filter on one branch as in Figure 2, the employment of two $\pi/4$ phase shifters makes the architecture more symmetric.

A frequency divider, with a division ratio of N, generates the LO signals $x_{LO,I}(t)$ and $x_{LO,Q}(t)$ in quadrature [27] from a sinusoidal tone at frequency Nf_{LO}. The division ratio N can be chosen to be equal to 2, 4, or 8 by selecting the output of the appropriate frequency divider by means of a multiplexer (MUX). Therefore, the LO signals $x_{LO,I}(t)$ and $x_{LO,Q}(t)$ are as follows:

$$x_{LO,I}(t) = A_{LO}sin(2\pi f_{LO}t) \quad (4)$$

$$x_{LO,Q}(t) = A_{LO}cos(2\pi f_{LO}t) \quad (5)$$

At the RF output ports of the mixers M_1 and M_2, the signals $x_{MIX,I}(t)$ and $x_{MIX,Q}(t)$ are consequently the following:

$$\begin{aligned} x_{MIX,I}(t) = k\tfrac{A_{LO}A_{IF}}{2}\{&cos\left[2\pi(f_{LO} - f_{IF1})t + \tfrac{\pi}{4}\right] - cos\left[2\pi(f_{LO} + f_{IF1})t - \tfrac{\pi}{4}\right] \\ &+cos\left[2\pi(f_{LO} - f_{IF2})t + \tfrac{\pi}{4}\right] - cos\left[2\pi(f_{LO} + f_{IF2})t - \tfrac{\pi}{4}\right]\} \end{aligned} \quad (6)$$

$$\begin{aligned} x_{MIX,Q}(t) = k\tfrac{A_{LO}A_{IF}}{2}\{&-sin\left[2\pi(f_{LO} - f_{IF1})t - \tfrac{\pi}{4}\right] + sin\left[2\pi(f_{LO} + f_{IF1})t + \tfrac{\pi}{4}\right] \\ &-sin\left[2\pi(f_{LO} - f_{IF2})t - \tfrac{\pi}{4}\right] + sin\left[2\pi(f_{LO} + f_{IF2})t + \tfrac{\pi}{4}\right]\}d \end{aligned} \quad (7)$$

where the following trigonometric identities are noted: $sin\alpha sin\beta = [cos(\alpha - \beta) - cos(\alpha + \beta)]/2$ and $sin\alpha cos\beta = [sin(\alpha - \beta) + sin(\alpha + \beta)]/2$. The constant k, of physical dimension [V^{-1}], causes the amplitude of the signals $x_{MIX,I}(t)$ and $x_{MIX,Q}(t)$ to be measured in Volt and not in $Volt^2$. In a real circuit, its presence is embedded in the transfer function of a real multiplier [26].

The signal $x_{SUM}(t)$ at the output of the sum node Σ is, therefore, as follows:

$$\begin{aligned} x_{SUM}(t) &= x_{MIX,Q}(t) - x_{MIX,I}(t) \\ &= \tfrac{\sqrt{2}}{2}kA_{LO}A_{IF}\{sin[2\pi(f_{LO} + f_{IF1})t] + cos[2\pi(f_{LO} + f_{IF1})t]\} \\ &\quad + \tfrac{\sqrt{2}}{2}kA_{LO}A_{IF}\{sin[2\pi(f_{LO} + f_{IF2})t] + cos[2\pi(f_{LO} + f_{IF2})t]\}, \\ &= kA_{LO}A_{IF}cos\left[2\pi(f_{LO} + f_{IF1})t - \tfrac{\pi}{4}\right] + kA_{LO}A_{IF}cos\left[2\pi(f_{LO} + f_{IF2})t - \tfrac{\pi}{4}\right] \end{aligned} \quad (8)$$

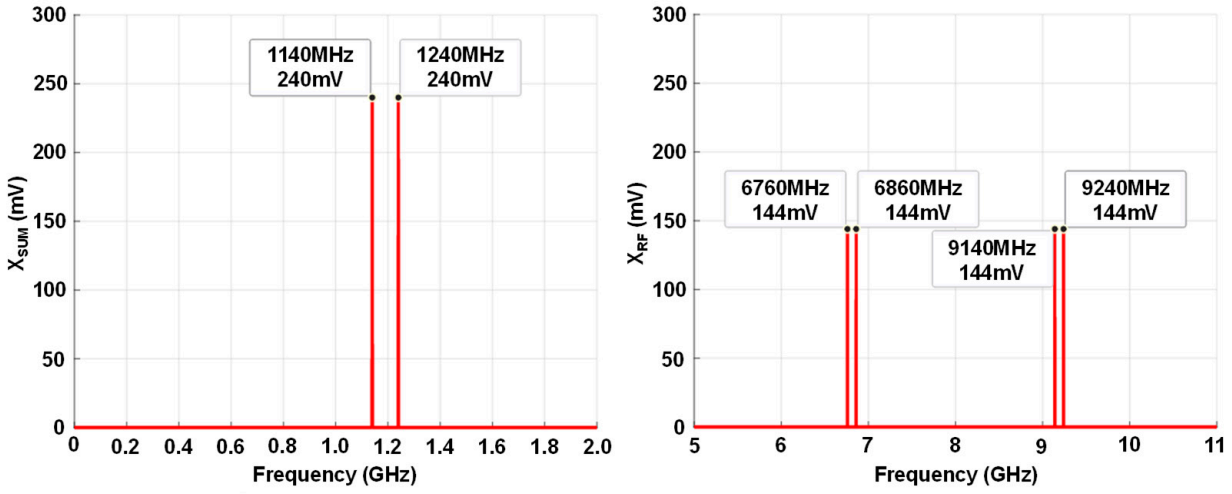
where the trigonometric identity $asinx + bcosx = Acos(x + \phi)$, with $A = \sqrt{a^2 + b^2}$ and $tan\phi = -a/b$, is noted. It is worth pointing out that the frequency components of the two signals $x_{MIX,I}(t)$ and $x_{MIX,Q}(t)$ undergo a destructive or constructive interference, as a consequence of their algebraic sum. In particular, subtracting the two signals as in Equation (8) leads to destructive interference for the components at frequencies $f_{LO} - f_{IF1}$ and $f_{LO} - f_{IF2}$, and to constructive interference for the components at frequencies $f_{LO} + f_{IF1}$ and $f_{LO} + f_{IF2}$. Therefore, the modulator in Figure 3 behaves as a USSB. Vice versa, adding the signals leads to constructive interference for the components at frequencies $f_{LO} - f_{IF1}$ and $f_{LO} - f_{IF2}$, and destructive interference for the components at frequencies $f_{LO} + f_{IF1}$ and $f_{LO} + f_{IF2}$.

Eventually, the mixer M_3 up-converts the signal $x_{SUM}(t)$ by means of the LO tone at frequency Nf_{LO}. The resulting RF output signal $x_{RF}(t) = x_{SUM}(t) \cdot x_{LO,N}(t)$ is as follows:

$$\begin{aligned} x_{RF}(t) = k\,\tfrac{A_{IF}A_{LO}^2}{2} sin\{2\pi[(N-1)f_{LO} - f_{IF1}]t + \tfrac{\pi}{4}\} \\ +k\tfrac{A_{IF}A_{LO}^2}{2} sin\{2\pi[(N+1)f_{LO} + f_{IF1}]t - \tfrac{\pi}{4}\} \\ +k\tfrac{A_{IF}A_{LO}^2}{2} sin\{2\pi[(N-1)f_{LO} - f_{IF2}]t + \tfrac{\pi}{4}\} \\ +k\tfrac{A_{IF}A_{LO}^2}{2} sin\{2\pi[(N+1)f_{LO} + f_{IF2}]t - \tfrac{\pi}{4}\}, \end{aligned} \tag{9}$$

where the trigonometric identity $sin\alpha cos\beta = [sin(\alpha-\beta) + sin(\alpha+\beta)]/2$ was used once again. The output spectrum exhibits thus four different frequency components. In Equation (9), the constant k of physical dimension [V^{-2}] causes the amplitude of the signal $x_{RF}(t)$ to be measured in Volt and not in $Volt^3$. In a real circuit, its presence is embedded in the transfer function of a real multiplier [26].

The building block diagram in Figure 3 has been Verilog coded within Cadence Virtuoso. Figure 4 shows the one-sided spectra of $x_{SUM}(t)$ and $x_{RF}(t)$, simulated for f_{LO} = 1 GHz, N = 8, f_{IF1} = 140 MHz, f_{IF2} = 240 MHz, A_{LO} = 1200 mV, and A_{IF} = 200 mV. Consistent with Equation (8), the spectrum exhibits two frequency components at the frequencies 1.140 GHz and 1.240 GHz, each with an amplitude of 240 mV. Similarly, in accordance with Equation (9), the signal exhibits components at the frequencies of 6.760 GHz, 6.860 GHz, 9.140 GHz, and 9.240 GHz, each with an amplitude of 144 mV. The Verilog simulations implicitly assumed the constants k to be unitary.



(**a**) (**b**)

Figure 4. Voltage one-sided spectrum of $x_{SUM}(t)$ (**a**) and $x_{RF}(t)$ (**b**).

Table 1 below succinctly summarizes the previous comparison.

Table 1. Amplitudes of the output tones for the modulator in Figure 3.

Frequency [MHz]	Calculated [mV] (from Equation (9))	Calculated [mV] (from Equation (8))	Simulated [mV]
1140	-	240	240
1240	-	240	240
6760	144	-	144
6860	144	-	144
9140	144	-	144
9240	144	-	144

The single-step frequency conversion in the SSB modulator depicted in Figure 2 generates second-order intermodulation products at the frequencies $f_{LO} \pm f_{IF}$. These frequencies are intended to match a qubit resonance frequency $f_{R,i}$ located close to f_{LO}. Typically, the frequency f_{LO} is in the order of a few GHz, and f_{IF} ranges from tens to hundreds of MHz. The narrow frequency separation $2f_{IF}$ urges to resort to a bandpass filter of the very high-quality factor Q. The practical approach involves thus interferometry at RF frequencies, at which, nevertheless, parasitic capacitances may introduce significant imbalances.

On the other hand, Figure 3 shows that the frequency spacing between the second-order intermodulation products in the proposed modulator is $2(f_{LO} + f_{IFi})$. For f_{LO} = 1 GHz, this spacing is large enough to accommodate a couple of qubits at the frequencies of the lower (higher) intermodulation products without taking care of the possible AC Stark effect, which the intermodulation products at higher (lower) frequencies may induce. An off-chip bandpass filter may be used to reduce the magnitude of the unused second-order intermodulation products. Since f_{LO} is much lower than f_{IFi}, the quality factor Q of the filter can be estimated to be in the order of tens of $(N-1)/4$ for the lower frequency intermodulation products and of tens of $(N+1)/4$ for the higher frequency intermodulation products. It is worth noticing that the frequency divider keeps the Q relaxed, because it makes Q dependent on N but independent of f_{LO}. In this way, the design of the filter is simpler, and it can be used to limit the potential impact of the image tone to the Spurious Free Dynamic Range (SFDR) in cases where it is desired, in spite of the fact that the second-order intermodulation products are well frequency spaced.

Moreover, the frequency divider allows for the use of only one Local Oscillator (LO). In Figure 3, the LO is assumed to be off-chip. The use of one single LO simplifies the experimental set-up. In cases where the LO is on-chip, it would take the form of a Phase Locked Loop (PLL), which is a complex circuit. The use of one single LO would save the silicon area and reduce power dissipation.

The frequency divider offers the further advantage of avoiding the use of a Hilbert filter or of a quadrature oscillator, because the divide-by-2 frequency dividers generate the in-phase and quadrature tones necessary for the USSB modulator [27].

In summary, the frequency divider offers several advantages. Firstly, it reduces the necessity for a bandpass filter, making it less essential. Moreover, should a bandpass filter be desired, the frequency divider alleviates the constraints on its quality factor. Additionally, the frequency divider reduces the requirement for frequency synthesis to just a single PLL, and it eliminates the need for Hilbert filters or quadrature oscillators.

3. Polyphase Filter

The $\pm\pi/4$ phase shifters in Figure 3 were designed as a Polyphase Filter (PPF), whose schematic is depicted in Figure 5.

It is the cascade of two double-stage, type II PFFs [28]. By assuming periodic signals, the first filter produces a $\pi/2$ dephased couple of differential signals from the single input differential signal applied at the input nodes V_- and V_+. In this way, the four-output single-ended signals split the full 2π angle into four phases, which is the reason why the filter is dubbed four-phase. The principle can be extended to a $4n$-phase PPF, which receives n input differential signals and returns $2n$ output differential signals, which are $4n$ single-ended signals. Following this, the second filter is an eight-phase PPF, because it receives two differential signals from the first PPF, and it generates four output differential signals, splitting the 2π angle into eight phases. Each filter was designed to be two-stage ones, in order to enlarge the bandwidth [28]. By keeping $R_1 = R_2 = R_3 = R_4 = R$, the capacitance of the capacitor C_1 (C_4) was chosen, such that $\omega_1 = 1/R_1C_1 = 2\pi f_L$ ($\omega_4 = 1/R_4C_4 = 2\pi f_H$), with f_L (f_H) being the lower (higher) cut-off frequency of the filter. For minimum phase errors, the capacitance of the capacitor C_2 (C_3) was chosen, such that $\omega_2 = 1/R_2C_2$ ($\omega_3 = 1/R_3C_3$) is the geometric mean of ω_1 and ω_3 (ω_2 and ω_4) [28], so that

$$\omega_2 = \sqrt{\omega_1\sqrt{\omega_2\omega_4}}, \tag{10}$$

$$\omega_3 = \sqrt{\omega_4 \sqrt{\omega_1 \omega_3}}, \tag{11}$$

from which the following is derived:

$$\omega_2 = \sqrt[3]{\omega_1^2 \omega_4}, \tag{12}$$

$$\omega_3 = \sqrt[3]{\omega_1 \omega_4^2}. \tag{13}$$

Since the frequencies of the IF signals are 140 MHz and 240 MHz, the PPF was designed with f_L = 100 MHz and f_H = 300 MHz. The obtained capacitances, calculated for R = 1 kΩ, are C_1 = 1.60 pF (ω_1 = 625 Mrad/s), C_2 = 1.11 pF (ω_2 = 900 Mrad/s), C_3 = 0.77 pF (ω_3 = 1299 Mrad/s), and C_4 = 0.53 pF (ω_4 = 1887 Mrad/s).

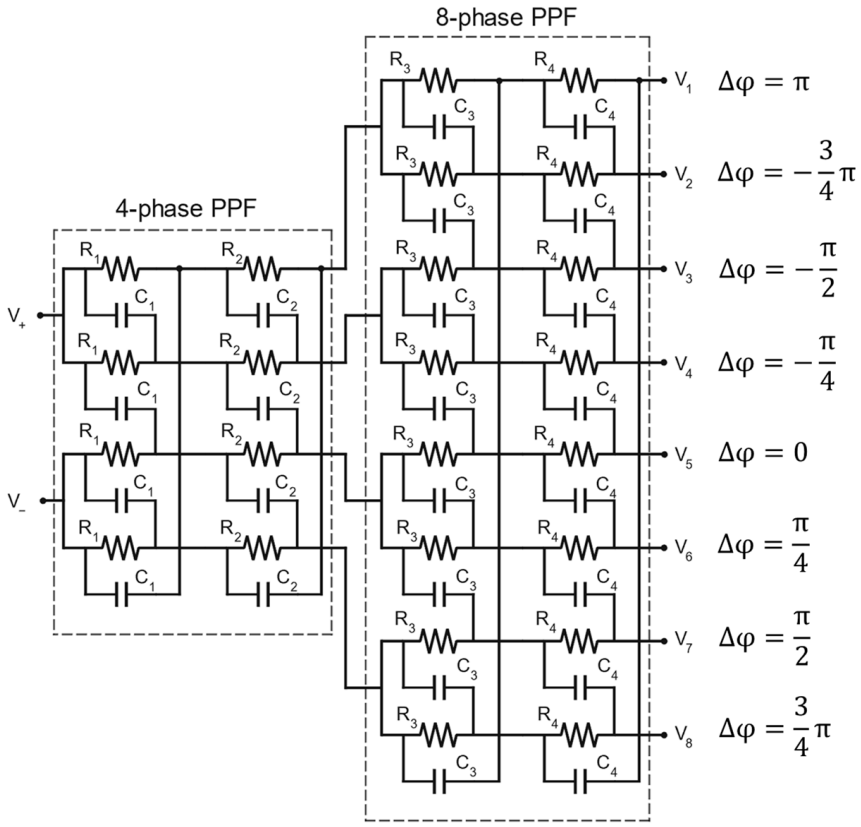


Figure 5. Polyphase filter.

Figure 6a shows the simulated phases of the eight single-ended voltage signals V_i (i = 1...8) at the output of the PPF. At f_L = 100 MHz, the values match with the desired phases reported in Figure 5. For higher frequencies, the phases roll off, but what is most important is that the relative phase is kept constant. Figure 6b plots the ratio between the amplitude of each output single-ended signal V_i and the amplitude of the differential input signal of the PPF. This figure shows that the four used V_i signals exhibit the same amplitude even if not constant over the bandwidth. Some amount of splitting in the curves has to be expected, because of the approximated physical feasibility of a Hilbert filter. By means of a phasorial picture, Figure 7 shows that, in accordance with the architecture in Figure 3, only the even phases were used; in particular, the signals V_4 and V_8 were used to obtain the differential signal $x_{IF,I}(t)$ and the signals V_6 and V_2 to obtain the differential signal $x_{IF,Q}(t)$. It is worth noting that varactors may make the polyphaser filters tunable to compensate for some unbalances [29]. Nevertheless, since the used Design Kit is a cryogenic one and the polyphaser filter operates at low frequencies, the filter was tailored as a fixed RC network.

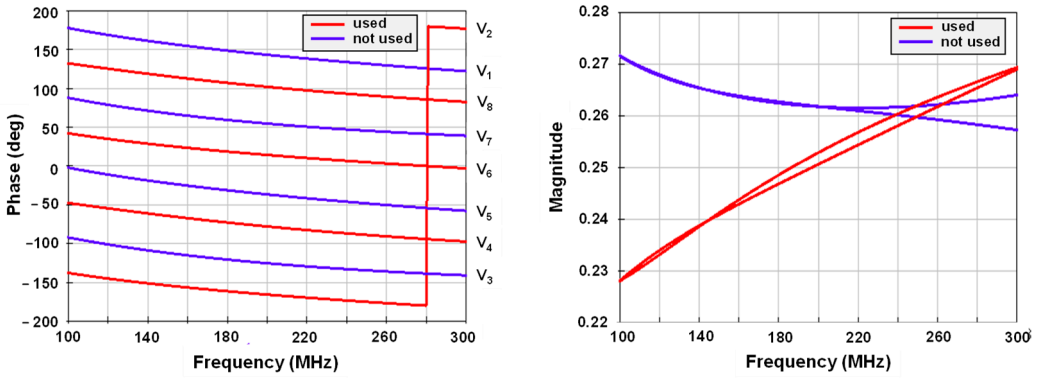


Figure 6. Simulated frequency responses of the PPF. Phase (**a**) and amplitude (**b**) responses of the eight signals at the output of the PPF; only the signals highlighted in red were used to obtain the signals $x_{IF,I}(t)$ and $x_{IF,Q}(t)$.

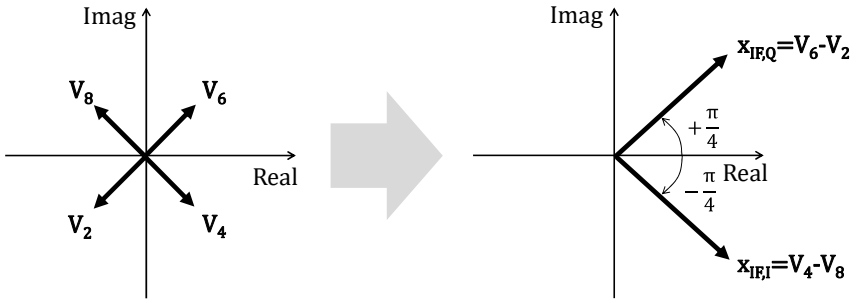


Figure 7. Voltage output signals V_2, V_4, V_6, and V_8 of the eight-phase PPF used to obtain the signals $x_{IF,I}(t)$ and $x_{IF,Q}(t)$.

4. Frequency Divider

Figure 8 details the frequency divider in Figure 3. Its main components are three chains of divide-by-2 frequency dividers and one multiplexer. In addition, inter-stage and output buffers isolate the dividers from the following stages.

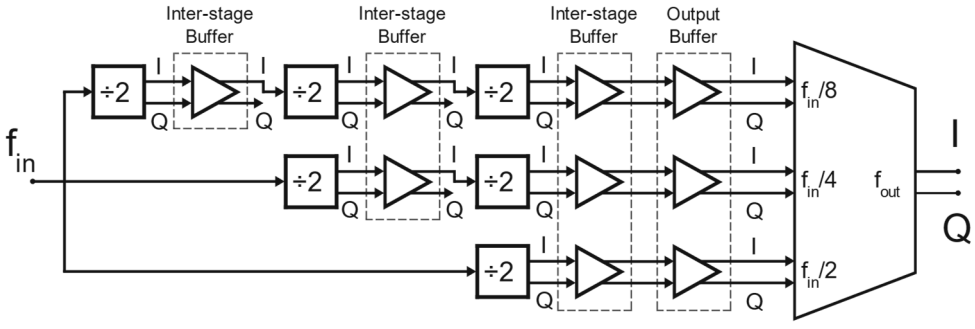
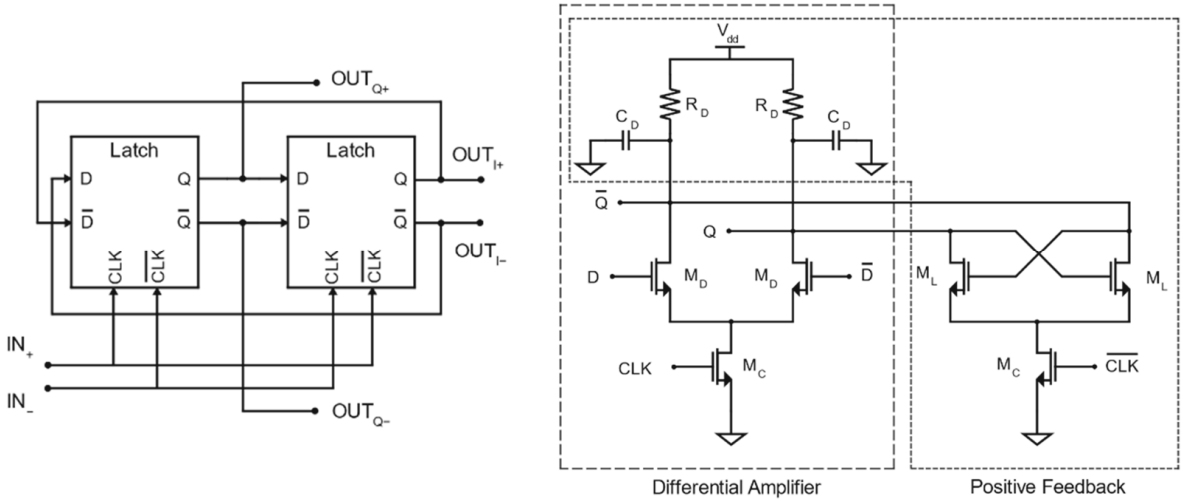


Figure 8. Frequency divider scheme. All the signals are differential.

4.1. Latches

Figure 9a shows that the divide-by-2 frequency divider is a traditional register obtained by arranging a couple of latches in a master–slave configuration [30]. It generates both In-phase (I) and Quadrature (Q) differential signals, because each single-ended output signal undergoes a phase shift equivalent to the full angle divided by four, i.e., the number of the output signals [27].



(**a**) (**b**)

Figure 9. (**a**) Divide-by-2 frequency divider; (**b**) schematic of the latch.

Figure 9b shows that each latch is formed by a differential pair (M_D) and a cross-coupled pair (M_L) of N-Channel MOSFET. These pairs share the same differential resistive load formed by the resistors R_D and the capacitors C_D. When the clock CLK is high (low), the pair M_D (M_L) form a differential amplifier (Current Mode Logic, or CML, latch), while the other pair M_L (M_D) is deactivated.

Therefore, when the clock is high, the differential voltage between the inputs D and $\overline{D}$ is amplified by the M_D pair, while, when the clock is low, the cross-coupled pair M_L latches the state. The left section of the circuit samples and amplifies the input differential signal, while the right section of the circuit executes the latching operation, nay it determines the sign of the sampled differential signal. The amplification, carried out by the M_D pair, aids and thus speeds up the decision process. In the transition from the amplification to the latch phase, the information is stored on the capacitors at the nodes Q and $\overline{Q}$. The combination of the CML logic positive feedback and the amplification ensures the high sensitivity and rapid propagation of even small voltage variations throughout the circuit, facilitating high-speed operations.

When the clock is not applied, only the bias voltage is applied to the gate of the M_C transistors, and the frequency divider works as a CML ring oscillator, with a self-oscillation frequency f_{SO}. This phenomenon is due to the negative feedback of the master–slave arrangement. The self-oscillation condition is given by [31]:

$$g_{mL}\left(1 + j\frac{W_D}{W_L}\right) = \frac{1}{R_D} + j2\pi f_{SO} C_D \tag{14}$$

where W_D and W_L are the channel width of the driving M_D and latching M_L transistors, respectively. Equation (14) is equivalent to the two following equations:

$$g_{mL} = \frac{1}{R_D} \tag{15}$$

$$f_{SO} = \frac{1}{2\pi}\frac{W_D}{W_L}\frac{1}{R_D C_D} \tag{16}$$

Equation (15) gives evidence that the M_L transistors should generate a small-signal-equivalent negative resistance which is able to compensate for the losses caused by the load resistors R_D. Equation (16) is the mathematical expression for f_{SO}.

In the case of n latches, even with n, f_{SO} can also be expressed as follows [32]:

$$f_{SO} = \frac{1}{2\pi} \frac{sin\frac{\pi}{n}}{cos\frac{\pi}{n} + \frac{|I_{LSO}|}{|I_{DSO}|}} \frac{1}{R_D C_D} \tag{17}$$

where $|I_{LSO}|$ and $|I_{DSO}|$ are the oscillation amplitudes of the currents flowing under the self-oscillation conditions, through the M_D and M_L transistors, respectively.

For $n = 2$, Equation (17) reduces to the following:

$$f_{SO} = \frac{1}{2\pi} \frac{|I_{DSO}|}{|I_{LSO}|} \frac{1}{R_D C_D}. \tag{18}$$

A comparison of Equations (16) and (18) shows that $|I_{LSO}|/W_L = |I_{DSO}|/W_D$.

On the other hand, when the clock is applied, the frequency divider behaves as an injection-locked oscillator.

The frequency f_{SO} can be interpreted as the output frequency generated by the divide-by-2 frequency divider for a clock signal of zero amplitude. For a criterion of continuity on the clock amplitude, the minimum clock voltage amplitude $V_{CLK,min}$ useful to lock the circuit occurs, therefore, for $f_{CLK} = 2f_{SO}$, with f_{CLK} being the clock frequency. The amplitude $V_{CLK,min}$ increases by increasing the frequency offset $\Delta f = |2f_{SO} - f_{CLK}|$. The plot of $V_{CLK,min}$ versus f_{CLK}, dubbed the sensitivity curve, thus exhibits a V shape centered around $2f_{SO}$.

Equation (19) below approximately describes the sensitivity curve [33]:

$$V_{CLK,min} = K_{inj} \frac{\left|\frac{f_{CLK}}{2f_{SO}} - 1\right|}{\sqrt{1 + \left(\frac{f_{CLK}}{2f_{SO}}\right)^2}}, \tag{19}$$

where K_{inj} is a parameter relating the current injected by the clock signal and the DC current. Equation (19) shows that $V_{CLK,min}$ approaches K_{inj} when f_{CLK} approaches zero or infinity.

Figure 10 plots the sensitivity curves of the three divide-by-2 frequency dividers tuned for f_{SO} which is equal to 4 GHz, 2 GHz, and 1 GHz. Table 2 reports the used sizing of the transistors, resistors, and capacitors for the three divide-by-2 frequency dividers.

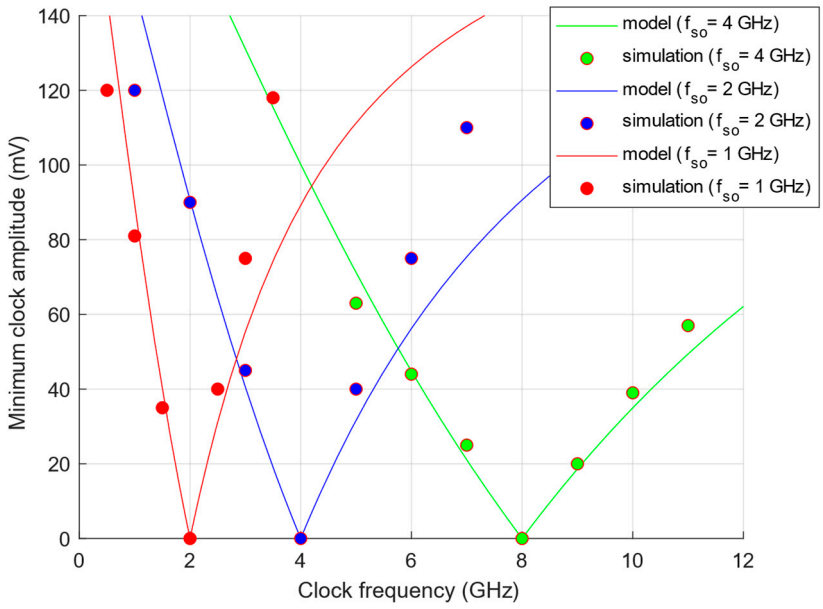


Figure 10. Sensitivity curves of the divide-by-2 frequency dividers.

Table 2. Sizing of the transistor, resistor, and capacitor in the latch.

f_{SO} [GHz]	L [nm]	W_D (µm)	W_L [µm]	W_C [µm]	R_D [kΩ]	C_D [fF]
4	130	4	4	3	1	17.3
2	130	4	4	3	1	53.5
1	130	4	4	3	1	126

This figure shows that simulation and fitting diverge with an increasing Δf and that this effect is more pronounced for a lower f_{SO}. Equation (19) adequately describes the sensitivity curves only when the ratio $\frac{\Delta f}{2f_{SO}}$ is small, that is for a f_{CLK} that is close to $2f_{SO}$, or for a f_{SO} that is larger than Δf, as in [33] and as in the highest frequency case in Figure 10.

4.2. Multiplexer and Buffers

Figure 11 shows that the cores of the multiplexer are four arrays of three N-channel pass transistors, two for the in-phase and two for the in-quadrature input differential signal. Three NOR gates generate, from the off-chip digital signals S_0 and S_1, the digital signals F_0, F_1, and F_2, controlling the pass transistors. When $S_0 = 0$ and $S_1 = 0$, only F_0 is high, and the MUX is configured to transmit the differential signals at frequency $f_{IN}/2$. When $S_0 = 1$ and $S_1 = 0$, only F_1 is high, and the MUX transmits the differential signals at frequency $f_{IN}/4$. When $S_0 = 0$ and $S_1 = 1$, only F_2 is high, and the MUX transmits the differential signals at frequency $f_{IN}/8$. Eventually, when $S_0 = 1$ and $S_1 = 1$, all the signals F_0, F_1, and F_2 are low, and the MUX is opaque. The NOR gates thus guarantee that two paths can never be activated simultaneously.

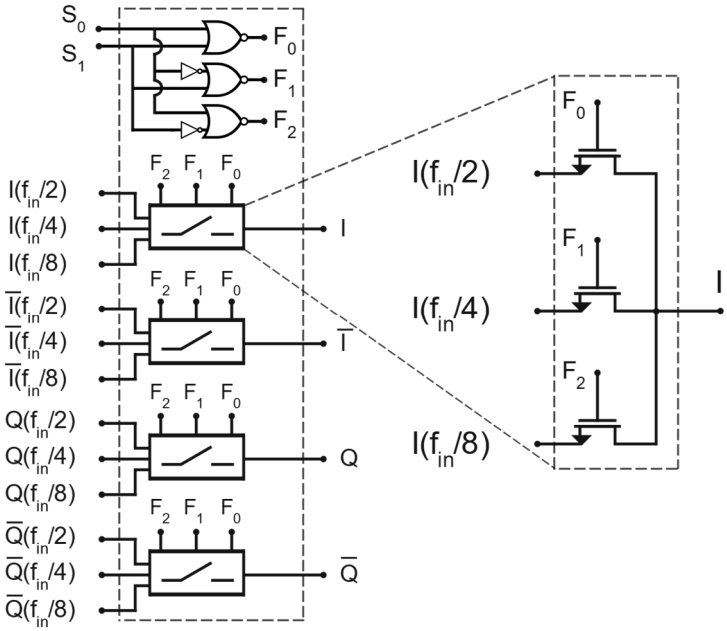


Figure 11. MUX is constituted of pass transistors that receive a control signal obtained with CMOS NOR logic gates.

Figure 12 depicts the circuits used for the inter-stage and output buffers in Figure 8. They isolate the output of the divide-by-2 frequency dividers from the capacitive load due to the following stages, avoiding, in this way, a frequency shift of the sensitivity curve. Since the I and Q signals in Figure 8 are differential, each buffer contains four of these circuits, one for each of the four phases.

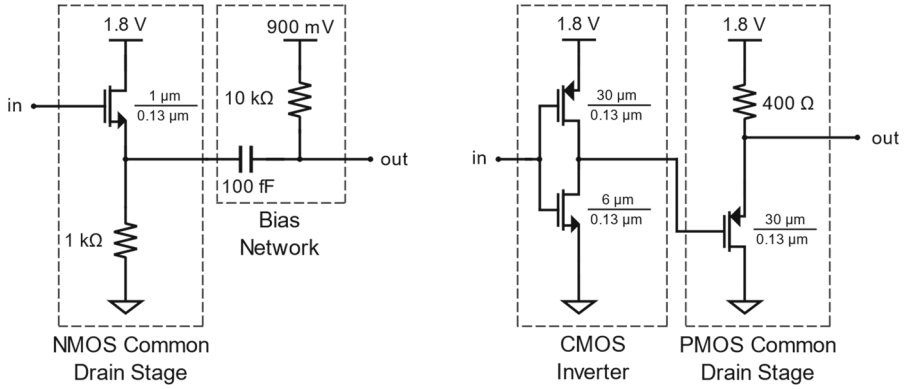


Figure 12. Circuit used for the inter-stage (**a**) and output (**b**) buffers.

5. Design of the Low-Frequency Mixer

Figure 13 depicts the schematic of the mixers M_1 and M_2 used for the USSB in Figure 3. The transistors M_1 and M_2 form the transconductance stage and operate under small-signal conditions. They convert the Intermediate Frequency (IF) voltage signals, applied to their gates, into IF small-signal currents $i_{IF,12} = g_m v_{GS1,2}$, where g_m and $v_{GS1,2}$ are, respectively, the transconductance and the small-signal gate–source voltage of the transistors M_1 and M_2, with $g_{m1} = g_{m2} = g_m$ and $v_{GS1} = -v_{GS2}$. The transistors $M_3 - M_6$ constitute the switching stage. To this aim, the LO signal must be sufficiently large to make these transistors behave as switches. In this way, they invert the polarity of the IF currents at the LO frequency rate, enabling frequency conversion by time variance.

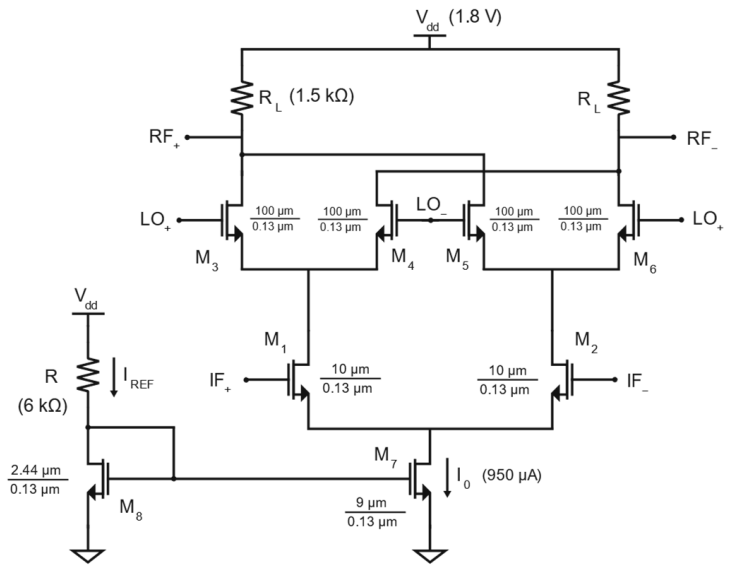


Figure 13. Circuit of the mixers in the USSB in Figure 3.

The switching activity generates small-signal currents with an RF spectrum reach of intermodulation products at the frequency $mf_{LO} \pm nf_{IF}$, where m and n are integer numbers, resulting from the two input tones at the frequencies f_{LO} and f_{IF}. They can be addressed by means of the short-circuit currents $i_{SC}(t)$ at the output nodes RF_+ and RF_-. By assuming that the input IF voltage signals on the gates of M_1 and M_2 are cosinusoidal tones of the amplitude v_{IF} and the frequency f_{IF} and are in phase opposition, you can write the following:

$$i_{SC}(t) = A(t)\, g_m v_{GS1,2} cos(\omega_{IF} t), \tag{20}$$

where $A(t)$ is a periodic square wave oscillating between -1 and $+1$ at the frequency ω_{LO}. It describes the periodic inversion polarity of the current due to the switching activity. The expansion of $A(t)$ in its Fourier series yields the following:

$$i_{SC}(t) = \frac{4}{\pi} g_m v_{IF} \left\{ sin(\omega_{LO} t) + \sum_{n=1}^{+\infty} \frac{sin[(2n+1)\omega_{LO} t]}{2n+1} \right\} cos(\omega_{IF} t), \tag{21}$$

which can be rewritten as follows:

$$i_{SC}(t) = \frac{2}{\pi} g_m v_{IF} \left\{ sin[(\omega_{LO} \pm \omega_{IF})t] + \sum_{n=1}^{+\infty} \frac{sin[[(2n+1)\omega_{LO} \pm \omega_{IF}]t]}{2n+1} \right\}, \tag{22}$$

where Werner's trigonometric identity $sin\alpha cos\beta = [sin(\alpha - \beta) + sin(\alpha + \beta)]/2$ is noted. The approximation of a mixer with a multiplier, under which only the second-order intermodulation products are of interest (see Section 2), leads to the following simplified mathematical expression of $i_{SC}(t)$:

$$i_{SC}(t) \cong \frac{2}{\pi} g_m v_{IF} sin[(\omega_{LO} \pm \omega_{IF})t]. \tag{23}$$

By supposing that the transistors $M_3 - M_6$ switch ideally, and by neglecting the capacitive parasitics, the Driving Point Impedance (DPI) technique [34] calculates the RF small-signal output differential voltage $v_{RF,DIFF}(t) = v_{RF+}(t) - v_{RF-}(t)$ as $i_{SC}(t)$ by the differential output resistance $R_{OUT,DIFF} = 2R_L$:

$$v_{RF,DIFF}(t) = \frac{4 g_m v_{IF} R_L}{\pi} sin[(\omega_{LO} \pm \omega_{IF})t]. \tag{24}$$

Since the amplitude of the IF input differential voltage signal $v_{IF,DIFF}$ is equal to $2v_{IF}$, Equation (24) yields the voltage conversion gain of the mixer equal to $2R_L g_m/\pi$, in agreement with [35]. On the other hand, if the transistors $M_3 - M_6$ do not switch ideally and/or capacitive parasitics should be accounted for, it is more efficient to analyze the circuit in the frequency domain. From Equation (23), the one-sided spectrum $I_{SC}(\omega)$ of $i_{sc}(t)$ is as follows:

$$I_{SC}(\omega) = \frac{2}{\pi} g_m v_{IF} \delta[\omega - (\omega_{LO} \pm \omega_{IF})], \tag{25}$$

where $\delta(\omega)$ is the Dirac's delta function. The spectrum $I_{SC}(\omega)$ exhibits, therefore, two lines of the magnitude $2g_m v_{IF}/\pi$. After the DPI technique, the one-sided spectrum $V_{RF,DIFF}(\omega)$ of $v_{RF,DIFF}(t)$ is as follows:

$$V_{RF,DIFF}(\omega) = \frac{2 g_m v_{IF} Z_{OUT,DIFF}(\omega)}{\pi} \delta[\omega - (\omega_{LO} \pm \omega_{IF})]. \tag{26}$$

where $Z_{OUT,DIFF}(\omega)$ is the differential output impedance.

Figure 3 shows the adopted sizing of the transistors and resistors. The bias DC gate voltage for M_1 and M_2 was set to 850 mV. With that sizing, the transistors M_1 and M_2 are biased in the saturation region with g_m= 7.725 mS.

The mixer was simulated for v_{IF} = 1 mV and f_{IN} = 10 MHz and for an LO square wave oscillating between 0 and 1.7 V at a frequency of f_{LO} = 1 GHz. For these amplitudes, the transistors M_1 and M_2 are in the saturation region all the time, so they operate as class A transconductors, while the transistors $M_3 - M_6$ are in the saturation region under DC conditions, nay for the mean value of the clock, in the triode region when the clock is high and in the off state when the clock is low. Figure 14a depicts the obtained one-sided spectrum. As expected from Equation (25), the spectrum exhibits two lines with the same magnitude and at the frequencies of 1010 MHz and 990 MHz. In particular, the value of the magnitude is also in agreement with Equation (25). Given g_m= 7.725 mS and v_{IF} = 1 mV, the resultant calculation yields $2g_m v_{IF}/\pi$ = 4.92 µA.

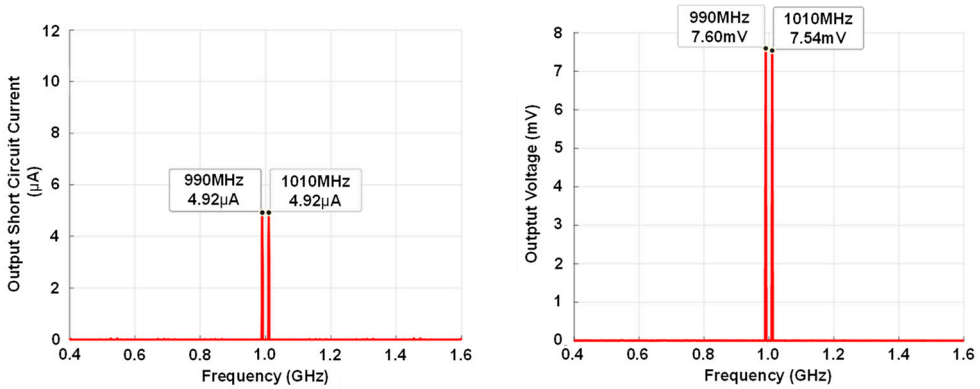


Figure 14. (**a**) Short-circuit current spectrum measured at the outputs of the mixer of Figure 15; (**b**) voltage spectrum of the outputs of the mixer.

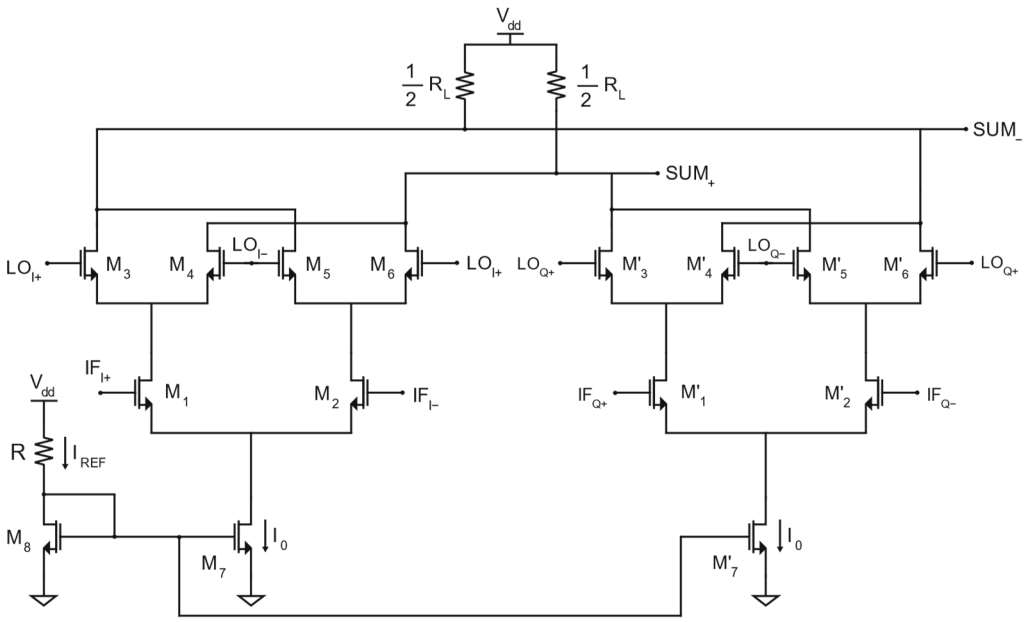


Figure 15. Schematic of the complete first mixing stage.

The differential output impedance $Z_{OUT,DIFF}(\omega)$ was simulated by means of the Periodic Scattering Parameter (PSP) simulation, with the square waveform large signal LO setting the time variance rate of the circuit. The modulus of $Z_{OUT,DIFF}(\omega)$ was found to be equal to 1.42 kΩ at 990 MHz and 1.40 kΩ at 1010 MHz. In good agreement with the simulated spectrum $V_{RF,DIFF}(\omega)$ in Figure 14b, Equation (26) indeed yields a magnitude of about 7.00 mV for the line at 990 MHz and of 6.89mV for the line at 1010 MHz. The error between simulations and calculation is about 8%. Table 3 below collects and compares the amplitudes discussed above.

Table 3. Amplitudes of the output tones for the mixer in Figure 13.

Frequency [MHz]	Calculated [mV] (from Equation (26))	Simulated	Error [%]
990	6.98	7.60	8.16
1010	6.89	7.54	8.62

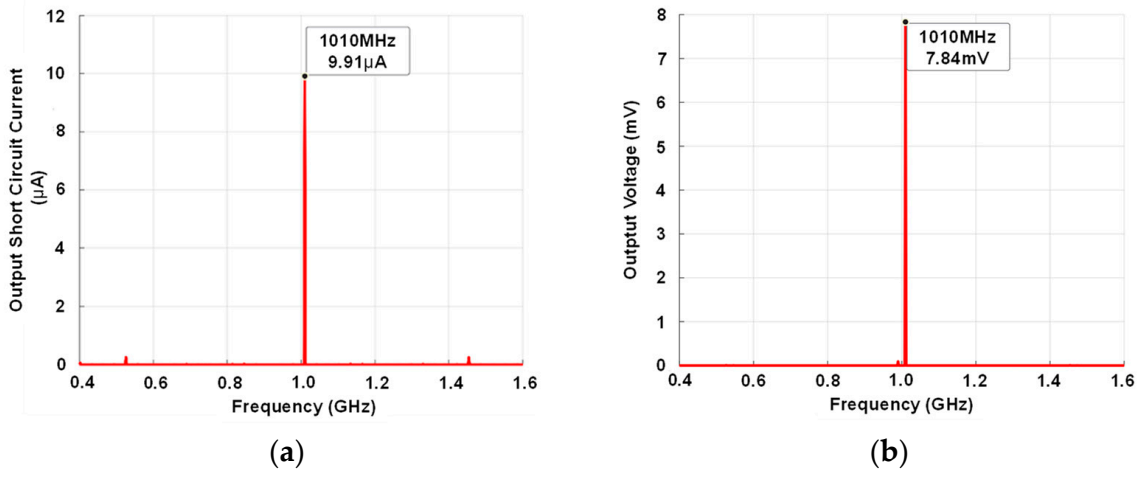
Figure 15 shows that the node Σ in the USSB modulator in Figure 3 was obtained by appropriately combining the RF currents generated by the couple of mixers. In particular, the positive phase current coming out from one mixer was combined with the negative phase current coming out from the other mixer. Since the two mixers share the same differential resistive loads, the DC current flowing through the load resistors in Figure 15 is two times the DC current flowing through the load resistors in Figure 13. The load resistors for the double mixer were thus sized as half of the load resistors for the single mixer to keep the same DC operating point used for the single mixer.

By means of the same analysis approach used for the single mixer in Figure 13, it is straightforwardly demonstrated (see Appendix A) that, for the mixer in Figure 15, the mathematical expression of the second-order intermodulation component of the output short-circuit current is as follows:

$$i_{SC}(t) = \frac{4}{\pi} g_m v_{IF} sin[(\omega_{LO} + \omega_{IF})t]. \quad (27)$$

Equation (27) shows that the one-sided spectrum $I_{SC}(t)$ of the short current $i_{SC}(t)$ is a single line at the frequency $\omega_{LO} + \omega_{IF}$ and of magnitude $4g_m v_{IF}/\pi$. It is worth noticing that this magnitude is two times the magnitude of the $I_{SC}(t)$ of the single mixer in Equation (23). This stems from the fact that the short-circuit currents of the double mixer result from the constructive interference of two short-circuit currents.

Figure 16a depicts the one-sided spectrum of the output short-circuit current simulated under the same conditions used for the single mixer, that is v_{IF} = 1 mV, f_{LO} = 1 GHz, and f_{IF} = 10 MHz. Since the transconductances of the transconductor transistors are the same for the two mixers, that is g_m = 7.725 mS, and because the single and double mixers were designed to have the same bias point, the simulated magnitude agrees with Equation (27), which yields $4g_m v_{IF}/\pi$ = 9.84 µA. The magnitude of the one-sided spectrum of the output differential voltage was calculated by means of the DPI. The PSP simulations yielded the modulus of $Z_{OUT,DIFF}(\omega)$, which is equal to 727.4 Ω at 1010 MHz. In agreement, within an error of about 9%, with the simulated spectrum $V_{RF,DIFF}(\omega)$ in Figure 16b, the DPI yields a magnitude of 7.16 mV for the magnitude of $V_{RF,DIFF}(\omega)$ at 1010 MHz. Table 4 summarizes these calculated and simulated amplitudes.



(**a**) (**b**)

Figure 16. One-sided spectrum of (**a**) the short-circuit current and (**b**) the output differential voltage.

Table 4. Amplitudes of the output tones for the mixer in Figure 15.

Frequency [MHz]	Calculated [mV] (from Equation (27))	Simulated	Error [%]
1010	7.16	7.84	8.67

6. Design of the High-Frequency Mixer

Figure 17 depicts the schematic of the up-conversion mixer M_3. It is the same mixer in Figure 13, apart from the two RC bias networks for the transistors M_1 and M_2. The resistance and capacitance are, respectively, 6 kΩ and 2 pF. The supply voltage V_{DD}, tail current I_0, and DC gate bias for M_1 and M_2 are the same as those adopted for the mixer in Figure 13.

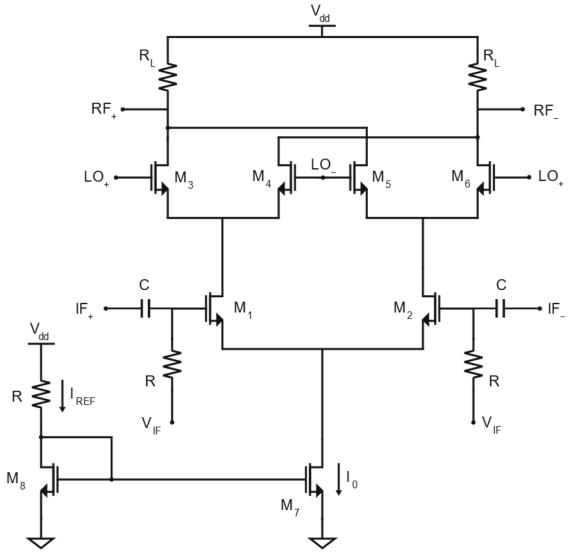


Figure 17. Mixer used for the up-conversion in Figure 3.

Figure 18 depicts the one-sided spectrum of the short-circuit current simulated for v_{IF} = 1 mV and f_{IF} = 1 GHz and for an LO square wave oscillating between 0 and 1.7 V at a frequency f_{LO} = 8 GHz. Apart from the higher f_{IF} and f_{LO}, these are the same conditions used for the simulation of the mixer in Figure 13. It is also worth noting that f_{LO} = 8 GHz corresponds to N = 8 in the architecture depicted in Figure 3. The spectrum exhibits two lines with the same magnitude of about 4.87 μA, in agreement with Equation (25), within a discrepancy of 1%, which yields 4.92 μA for g_m = 7.725 mS and v_{IF} = 1 mV.

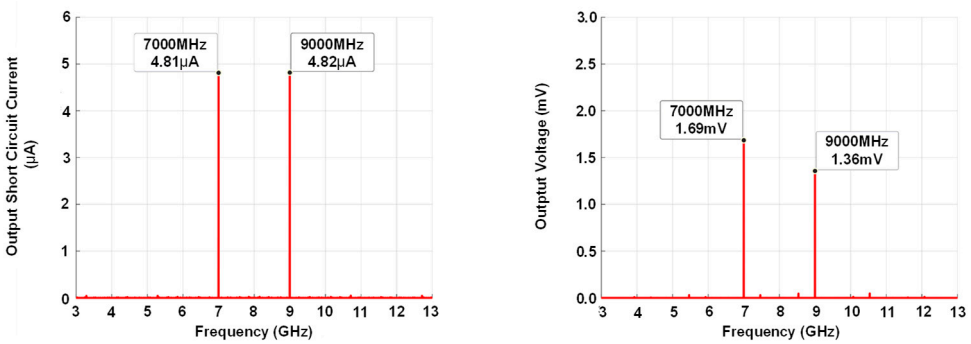


Figure 18. One-sided spectrum of (**a**) the short-circuit current and (**b**) the output differential voltage.

Once again, the one-sided spectrum $V_{RF,DIFF}(\omega)$ of the differential output voltage was calculated by means of the DPI technique. The PSP simulations yielded a modulus of the differential output impedance of 318 Ω (240 Ω) at the frequency of 7 GHz (9 GHz), corresponding to a magnitude of $V_{RF,DIFF}(\omega)$, which is equal to 1.57 mV (1.18 mV), in agreement with the simulated magnitude of 1.69 mV (1.36 mV), within a discrepancy of about 7% (13%).

Table 5 below collects and compares the amplitudes discussed above.

Table 5. Amplitudes of the output tones for the mixer in Figure 17.

Frequency [MHz]	Calculated [mV] (from Equation (26))	Simulated	Error [%]
7000	1.57	1.69	7.10
9000	1.18	1.36	13.24

7. Simulation of the Modulator

This section addresses the transistor-level simulation of the modulator whose architecture is depicted in Figure 3. The two input IF differential signals are two sinusoidal tones of amplitude 10 mV and frequencies 140 MHz and 240 MHz. The LO differential signal was a square wave of amplitude 1.7 V. Figure 19 shows the spectrum of the output differential signal generated by the modulator when the division ratio $N = 8$, that is when the LO frequency f_{LO} is 8 GHz. The spectrum exhibits four tones at the frequencies of 6.76 GHz, 6.86 GHz, 9.14 GHz, and 9.24 GHz, in agreement with the Verilog simulation in Figure 4b. Figures 20 and 21 also demonstrate the same agreement between circuit-level and Verilog simulations for $N = 4$ ($f_{LO} = 4$ GHz) and $N = 2$ ($f_{LO} = 2$ GHz), respectively.

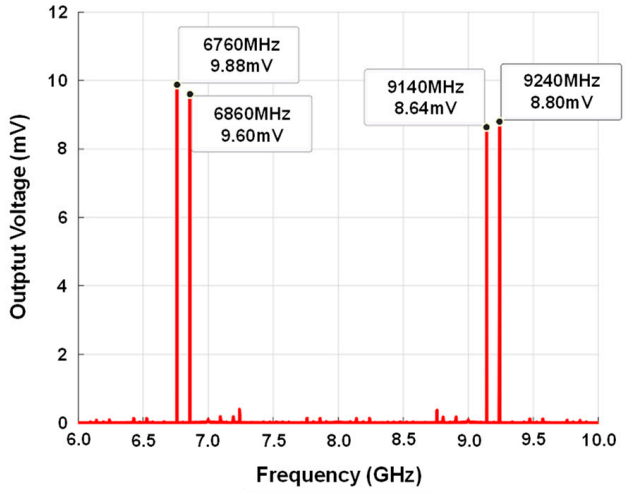


Figure 19. One-sided spectrum of the output signal generated by the modulator for $N = 8$.

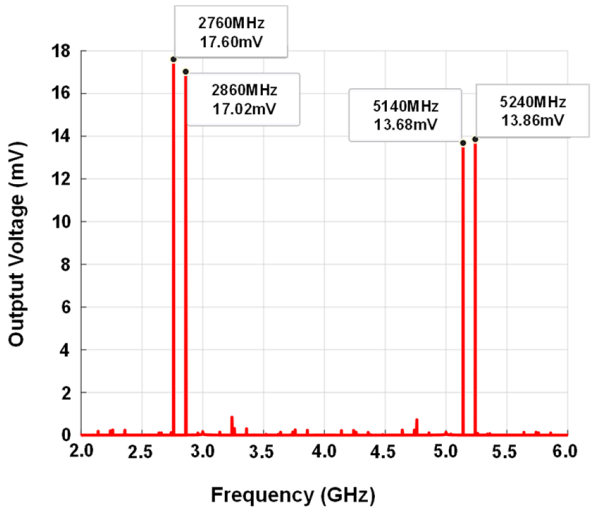


Figure 20. One-sided spectrum of the output signal generated by the modulator for $N = 4$.

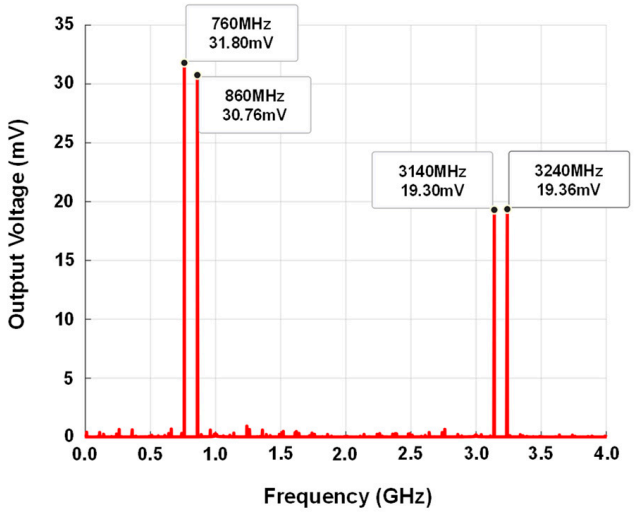


Figure 21. One-sided spectrum of the output signal generated by the modulator for $N = 2$.

An assessment of the correctness of the amplitudes needs the evaluation of the voltage conversion gain of the mixers at the frequencies of interest. For the mixer in Figure 15, it is necessary to determine the voltage conversion gain for the output frequencies of 1140 MHz and 1240 MHz. In this case, the mixer cannot be simulated on its own as in Section 5 because of the loading effect due to the up-conversion mixer. The simulations showed a voltage conversion gain of approximately 3.1, which is lower than the gain deduced from Figure 16, as expected.

On the other hand, the conversion gain of the up-conversion mixer in Figure 17 can be calculated following the same approach used in Section 6, because the mixer was not closed on an output load. The conversion gain was calculated for each of the twelve frequencies addressed in Figures 19–21. For instance, for the frequencies in Figure 20, the following moduli for the differential output impedances were obtained from the PSP simulations: 507.6 Ω at 2760 MHz, 502.5 Ω at 2860 MHz, 323.7 Ω at 5140 MHz, and 316.5 Ω at 5240 MHz. The resulting calculated voltage conversion gain is about 1.24 at 2760 MHz and 2860 MHz and about 0.80 at 5140 MHz and 5240 MHz. For the other frequencies, a voltage conversion gain of 2.18 for the frequency couple 760 MHz and 860 MHz was found, of 1.12 for the couple 3140 MHz and 3240 MHz, of 0.80 for the couple 6760 MHz and 6860 MHz, and of 0.58 for the couple 9140 MHz and 9240 MHz. Figure 22 summarizes these voltage conversion gains.

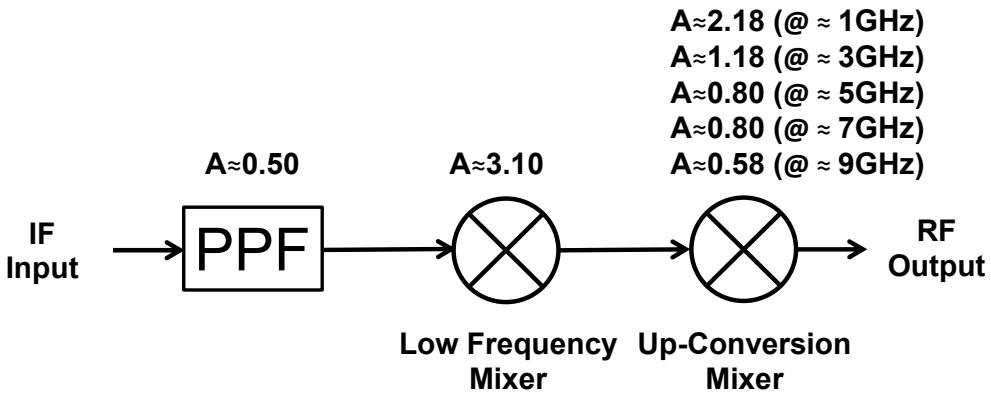


Figure 22. Rough representation of the modulator. All the signals are differential.

By means of the rough representation of the modulator in Figure 22, it is possible to calculate the amplitudes of the lines in the spectra in Figures 19–21. Note that after

Figure 6b, the PPF exhibits an attenuation of about 0.5, because all the signals in Figure 22 are differential. It is worth noting that plots in Figure 6b are indeed the attenuation for each single-ended signal V_i ($i = 1...8$) with respect to the input differential signal.

Since the input signal exhibits a differential amplitude of 10 mV, Figure 22 yields a differential amplitude of the lines around 5 GHz, that is at 5140 MHz and 5240 MHz, of 12.4 mV, which matches with the spectrum in Figure 20, within an error of about 10%. For the lines around 1 GHz, that is at 760 MHz and 860 MHz, Figure 22 yields a differential amplitude of 33.8 mV, which agrees with the spectrum in Figure 21, within an error of about 7%. For the lines around 9 GHz, that is at 9140 MHz and 9240 MHz, Figure 22 yields a differential amplitude of 9.0 mV, in agreement with the spectrum in Figure 19, within an error of about 3%. For the lines around 3 GHz, the agreement remains acceptable within an error margin of 10%, whereas for the lines around 7 GHz, the error margin is 20%. Table 6 below summarizes the above comparison.

Table 6. Output differential amplitudes for the different output frequencies.

Frequency [GHz]	Simulated [mV]	Calculated [mV]	Average Error [%]
1	31.3	33.8	7.4
3	17.3	18.3	5.5
5	13.8	12.4	11.3
7	9.7	12.4	21.8
9	8.7	9.0	3.3

The linearity of the modulator was assessed by means of transient simulations. A first set of simulations was carried out for $N = 4$ and for a single 140 MHz input IF sinusoidal tone, whose differential amplitude spanned from 10 mV to 100 mV. The picked-up differential output signal was the tone at the 2.86 GHz frequency (see Figure 20). The voltage gain was plotted versus the differential amplitude of the IF input signal. Table 7 collects the obtained results. It shows that a decrease of 1 dB in the voltage gain occurs for a voltage input of 80 mV. The 1 dB compression point thus corresponds to an input differential voltage amplitude of about 80 mV.

Table 7. Voltage gain of the modulator versus the amplitude of the input 140 MHz IF signal for $N = 4$.

Input [mV]	Output [mV]	Voltage Gain (dB)
10	17.02	4.62
40	66.28	4.39
60	95.02	3.97
80	118.86	3.46
100	137.08	2.73

A second set of simulations were carried out for $N = 4$ and for a couple of input IF sinusoidal tones at the frequency of 140 MHz and 240 MHz and with the same magnitude of 10 mV. The highest output intermodulation component was found at 2.96 GHz, with a negligible amplitude of about 0.5 µV, in agreement with Figure 20. It is worth noting that, in the literature, the pulse amplitude at the port of a qubit driver is estimated to be in the range of a few mVs [36].

The proposed modulator dissipates about 100 mW, which is entirely ascribed to the frequency divider. On the other hand, the two mixers dissipated about 5 mW. Even if it were improved, the power dissipation is compatible with the power budget of 1 W estimated for a cryostat working at 4 K [36] and in the same order of magnitude of the dissipated power claimed in [17,18,37,38], as reported in Table 8. The 2 mW power dissipation claimed in [36] for a 28 nm bulk-CMOS cryo-controller remains outstanding. It is worth noticing that the adopted mixers are passive.

The low- frequency SSB mixer sets the noise figure of the modulator to about 23 dB, which should mainly be ascribed to the input PPF, whose simulated minimum noise figure is about 13 dB, a value in agreement with the following formula [39]:

$$NF_{MIN} = 10log\left[2^N\left(1+\sqrt{2}\right)\right] \quad (28)$$

which provides the minimum noise figure for an N layer polyphaser filter. Equation (28) yields NF_{MIN} = 16 dB for N = 4. The up-conversion mixer exhibits a DSB NF of about 5 dB. Since the noise figure of transmitters are not usually reported in the literature, it may be useful to cite the noise figure of 20–25 dB for the 180 nm CMOS 5 GHz quadrature down-converter described in [40], which shares, with the proposed modulator, mixers similar to the mixer in Figure 3 and a PPF in the input signal path.

Eventually, Table 8 below helps to compare the proposed modulator with other qubit controllers in the literature. The Multi Project Wafer (MPW) costs are those available on the websites of the IC services Europractice (Europe) and CMC Microsystems (Canada). Only this paper and [41] keep a cost low by using bulk CMOS. All the other implementations exhibit higher MPW costs because of the adopted FinFET technology.

Table 8. Comparison summary.

	This Work	**[17]**	**[18]**	**[36]**	**[37]**	**[38]**	**[41]**	**[42]**
Operating temperature [K]	4	3	3	3	3	4	3.5	3
Qubit technology	Spin and Trans.	Spin	Spin and Trans.	Trans.	Spin and Trans.	Spin	Trans.	Trans.
Dissipated power [mW]	100	360	384	2	384	190	12	23
Frequency range [GHz]	0.9–9	2–20	5–20	4–8	2–20	11–17	4.6–8.1	4.5–5.5
Number of qubits	2	32	32	1	2	16	1	1
IF signal source	Off-chip	On-chip	On-chip	On-chip	On-chip	On-chip	On-chip	On-chip
LO signal source	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip
CMOS technology	130 nm bulk	22 nm FinFET	22 nm FinFET	28 nm bulk	22 nm FinFET	22 nm FinFET	40 nm bulk	14 nm FinFET
MPW cost [kEUR/mm^2]	7.3	27.2	27.2	14	27.2	27.2	6.1	14.7

8. Conclusions

This paper reported on the design of a modulator aimed to control 2 qubits. The circuit was tailored as an RFIC and designed by using the cryogenic Design Kit of SG13G2 130 nm SiGe BiCMOS technology by the IHP foundry (Innovation for High-Performance Microelectronics) in Frankfurt am Oder, Germany.

A low-frequency Upper Single-Side Band (USSB) modulator and a following high-frequency up-conversion mixer form the core of the proposed modulator. An off-chip microwave source provides a large LO signal for the mixers. In particular, a frequency divider allows for the use of this external LO signal for both the low-frequency modulator

and the high-frequency mixer. This is the most interesting peculiarity of the proposed modulator, because the frequency divider leads to several advantages.

It enables the carrier and its image at the output of the up-conversion mixer to be sufficiently spaced in frequency to accommodate a couple of qubits with resonance frequencies close to the carrier or its image. For instance, with reference to Figure 20, you can address two qubits of resonance frequencies equal to 2760 MHz and 2860 MHz (5140 MHz and 5240 MHz) without taking care of the tones at higher (lower) frequencies. Nevertheless, the magnitudes of the unused tones can be reduced by introducing an off-chip band-pass filter, whose quality factor is relaxed by the use of the frequency divider. In addition, the frequency divider reduces the need for frequency synthesis to a single PLL, and it avoids the use of Hilbert filters or quadrature oscillators to generate the in-phase and in-quadrature tones for the USSB.

The frequency divider was designed to divide by 2, 4, and 8. This makes the proposed modulator a multi-frequency one, because it allows for addressing qubits, whose resonance frequencies are close to 1 GHz, 3 GHz, 5 GHz, 7 GHz, and 9 GHz. This may be useful, because each qubit technology has different resonance frequency ranges. Indeed, for Nitrogen-Vacancy qubits, the typically exploited resonance frequency is 2.87 GHz [43]; for superconducting qubits, the resonance frequency spans between 500 MHz and 10 GHz; for trapped ion qubits, the frequency range is in the order of a few GHz; and semiconductor spin qubits cover a frequency range from hundreds of MHz to up to tens of GHz [44].

Nevertheless, it is worth noticing that even though the modulator does not use any integrated inductor, the sensitivity curves of the frequency dividers make it narrowband. The architecture can be re-employed for addressing a different set of frequencies but at the effort of retuning the sensitivity curves of the frequency dividers, which is mainly possible by choosing the capacitor C_D appropriately (see Table 2).

The agreement between the mathematical modeling, the Verilog, and the transistor-level simulations, together with the general good consistency between the transistor-level simulations of the individual building blocks (polyphase filter and the lower and higher frequency mixers) and of the whole modulator, proves that the architecture of the proposed modulator is effectively implementable in the IHP 130 nm cryogenic BiCMOS technology.

The main advantage offered by the proposed architecture is that the SSB interferometry takes place at a lower frequency with respect to other controllers claimed in the literature, where the interferometry occurs at a high frequency (see, for instance, references [21,36,37]). A low-frequency interferometric structure is less sensible to gain and phase impairments due to the parasitics. This may relax the requirement for stringent IQ calibration, in contrast to [21]. A final radiofrequency SSB signal may be obtained by adopting a classical filtering, because the frequency divider relaxes the quality factor of the filter.

The price to be paid is the power dissipated by this frequency divider, which is the main limitation of the proposed modulator. On the other hand, the estimated linearity and noise figure appear to be comparable.

Author Contributions: Conceptualization, A.B. and M.B.; methodology, A.B. and M.B.; software, A.B.; validation, A.B.; formal analysis, A.B.; investigation, A.B.; data curation, A.B.; writing—original draft preparation, A.B.; writing—review and editing, M.B.; supervision, M.B. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data are contained within the article.

Acknowledgments: Thanks are due to the IHP foundry (Frankfurt am Oder, Germany) for making available their cryogenic 130 nm SiGe BiCMOS Design Kit SG13G2C.

Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A

Figure 15 shows that when LO_{I+} is high, the transconductor transistor M_1 contributes to the short-circuit current $i_{SC}(t)$ on the drain of the transistor M_3. Since, as for the single mixer, the transistors M_1, M_2, M'_1, and M'_2 are all identical and fully differentially driven, their sources are at the virtual ground, after Equation (20) you can write the mathematical expression of this contribution:

$$i_{SC}(t) = g_m v_{IN} cos(\omega_{IF} t) \tag{A1}$$

On the other hand, when LO_{I-} is high, the transconductor transistor M_2 contributes via M_5 to $i_{SC}(t)$ at the node SUM_ so that you can write the mathematical expression of this contribution as follows:

$$i_{SC}(t) = -g_m v_{IN} cos(\omega_{IF} t) \tag{A2}$$

Similarly, when LO_{Q+} is high the transistor M'_2 provides, via M'_6, the following contribution to the short circuit at the node SUM_:

$$i_{SC}(t) = -g_m v_{IN} sin(\omega_{IF} t) \tag{A3}$$

whereas the transistor M'_1 contributes, via M'_4, with the following current when LO_{Q-} is high:

$$i_{SC}(t) = g_m v_{IN} sin(\omega_{IF} t) \tag{A4}$$

Figure A1 reminds that the two LO large differential signals controlling the switching transistors in the two mixers in Figure 15 are time shifted of a quarter of period, because they are at the quadrature. They split, therefore, the switching activity of the double mixer into four phases instead of the two phases of the single mixer in Figure 13.

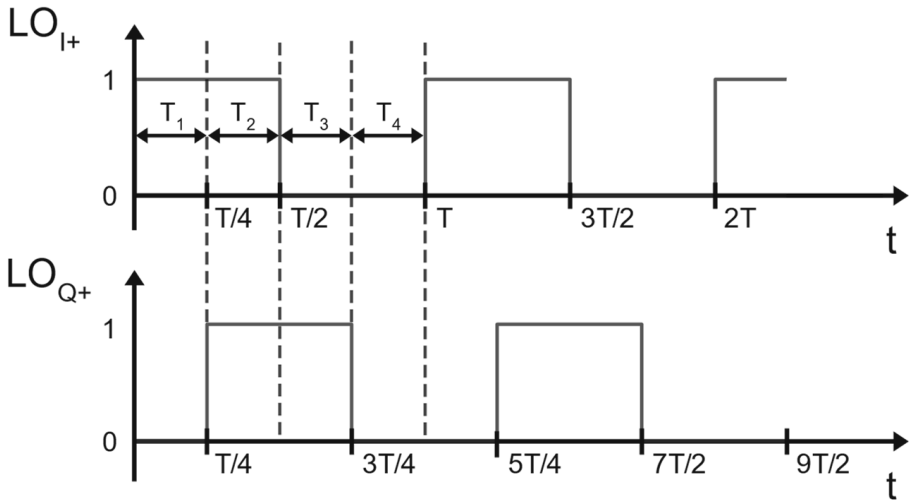


Figure A1. LO_{I+} and LO_{Q+} square wave LO signals.

During the time interval T_1 when LO_{I+} and LO_{Q-} are high, Equations (A1) and (A4) the short-circuit current on the drain of M_3:

$$i_{SC}(t) = g_m v_{IN} [cos(\omega_{IF} t) + sin(\omega_{IF} t)] \tag{A5}$$

During the time interval T_2 when LO_{I+} remains still high but LO_{Q+} has switched from low to high, Equations (A1) and (A3) yield:

$$i_{SC}(t) = g_m v_{IN} [cos(\omega_{IF} t) - sin(\omega_{IF} t)] \tag{A6}$$

During the time interval T_3 when LO_{I-} has switched from low to high and LO_{Q+} remains still high, Equations (A2) and (A3) yield:

$$i_{SC}(t) = g_m v_{IN}[-cos(\omega_{IF}t) - sin(\omega_{IF}t)] \tag{A7}$$

Eventually, during the time interval T_4 when LO_{I-} remains still high but LO_{Q-} has switched back from low to high, Equations (A2) and (A4) yield:

$$i_{SC}(t) = g_m v_{IN}[-cos(\omega_{IF}t) + sin(\omega_{IF}t)] \tag{A8}$$

Equation from (A5) to (A8) can be grouped in the following one:

$$i_{SC}(t) = g_m v_{IN}\left[A_I(t)cos(\omega_{IF}t) + A_Q(t)sin(\omega_{IF}t)\right] \tag{A9}$$

where the two square-wave functions $A_I(t)$ and $A_Q(t)$ are depicted in Figure A2.

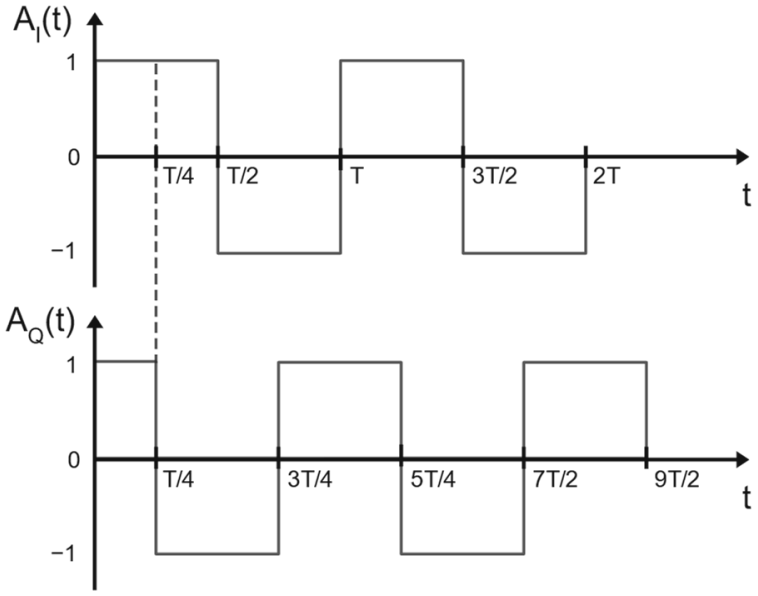


Figure A2. In-phase and quadrature square waves $A_I(t)$ and $A_Q(t)$.

The Fourier series expansion of $A_I(t)$ and $A_Q(t)$ are, respectively:

$$A_I(t) = \frac{4}{\pi}\sum_{n=0}^{+\infty}\frac{sin[(2n+1)\omega_{LO}t]}{2n+1} \tag{A10}$$

$$A_Q(t) = -\frac{4}{\pi}\sum_{n=0}^{+\infty}\frac{sin\left[(2n+1)\omega_{LO}\left(t-\frac{T_{LO}}{4}\right)\right]}{2n+1} \tag{A11}$$

where T_{LO} is the period of the LO square-wave large signal. By approximating the mixer with a multiplier, only the second order intermodulation products are of interest, and Equation (A9) reduces to:

$$i_{SC}(t) = \frac{4}{\pi}g_m v_{IN}\left\{sin(\omega_{LO}t)cos(\omega_{IF}t) - sin\left[\omega_{LO}\left(t-\frac{T}{4}\right)\right]sin(\omega_{IF}t)\right\} \tag{A12}$$

By remarking that $\omega_{LO}T_{LO}/4 = \pi/2$, Equation (A12) takes the following shorter form:

$$i_{SC}(t) = \frac{4}{\pi}g_m v_{IN}[sin(\omega_{LO}t)cos(\omega_{IF}t) + cos(\omega_{LO}t)sin(\omega_{IF}t)] \tag{A13}$$

where it was reminded that $sin(\alpha - \pi/2) = -cos(\alpha)$. By also reminding the Werner's trigonometric identity $sin\alpha cos\beta = [sin(\alpha + \beta) + sin(\alpha - \beta)]/2$, Equation (A13) yields:

$$i_{SC}(t) = \frac{2}{\pi} g_m v_{IN} \{sin[(\omega_{LO} + \omega_{IF})t] + sin[(\omega_{LO} - \omega_{IF})t] + sin[(\omega_{LO} + \omega_{IF})t] - sin[(\omega_{LO} - \omega_{IF})t]\} = \frac{4}{\pi} g_m v_{IN} sin[(\omega_{LO} + \omega_{IF})t] \quad \text{(A14)}$$

which proves Equation (27). It is worth point out that Equation (A14), deduced from the analysis of the circuit in Figure 15, reproduces the destructive interference of the tone at lower frequency as already observed during the general discussion of the building block diagram in Figure 3.

References

1. Harrow, A.; Montanaro, A. Quantum computational supremacy. *Nature* **2017**, *549*, 203–209. [CrossRef] [PubMed]
2. Möller, M.; Vuik, C. On the impact of quantum computing technology on future developments in high-performance scientific computing. *Ethics Inf. Technol.* **2017**, *19*, 253–269. [CrossRef]
3. Nielsen, M.; Chuang, I. *Quantum Computation and Quantum Information*, 10th Anniversary ed.; Cambridge University Press: Cambridge, UK, 2010. [CrossRef]
4. Hoefler, T.; Häner, T.; Troyer, M. Disentangling Hype from Practicality: On Realistically Achieving Quantum Advantage. *Commun. ACM* **2023**, *66*, 82–87. [CrossRef]
5. Shor, P.W. Polynomial-Time Algorithms for Prime Factorization and Discrete Logarithms on a Quantum Computer. *SIAM J. Comput.* **1997**, *26*, 1484–1509. [CrossRef]
6. Chae, E.; Choi, J.; Kim, J. An elementary review on basic principles and developments of qubits for quantum computing. *Nano Converg.* **2024**, *11*, 11. [CrossRef] [PubMed]
7. Loss, D.; DiVincenzo, D.P. Quantum computation with quantum dots. *Phys. Rev. A* **1998**, *57*, 120–126. [CrossRef]
8. Veldhorst, M.; Hwang, J.C.C.; Yang, C.H.; Leenstra, A.W.; de Ronde, B.; Dehollain, J.P.; Muhonen, J.T.; Hudson, F.E.; Itoh, K.M.; Morello, A.; et al. An addressable quantum dot qubit with fault-tolerant control-fidelity. *Nat. Nanotechnol.* **2014**, *9*, 981–985. [CrossRef] [PubMed]
9. Urdampilleta, M.; Niegemann, D.J.; Chanrion, E.; Jadot, B.; Spence, C.; Mortemousque, P.-A.; Bäuerle, C.; Hutin, L.; Bertrand, B.; Barraud, S.; et al. Gate-based high fidelity spin readout in a CMOS device. *Nat. Nanotechnol.* **2019**, *14*, 737–741. [CrossRef] [PubMed]
10. Nikandish, R.; Blokhina, E.; Leipold, D.; Bogdan Staszewski, R. Semiconductor Quantum Computing: Toward a CMOS quantum computer on chip. *IEEE Nano Technol. Mag.* **2021**, *15*, 8–20. [CrossRef]
11. Anders, J.; Babaie, M.; Bardin, J.C.; Bashir, I.; Billiot, G.; Blokhina, E.; Bonen, S.; Charbon, E.; Chiaverini, J.; Chuang, I.L.; et al. CMOS integrated circuits for the quantum information sciences. *IEEE Trans. Quantum Eng.* **2023**, *4*, 1–30. [CrossRef]
12. Borgarino, M.; Badiali, A. Quantum Gates for Electronics Engineers. *Electronics* **2023**, *12*, 4664. [CrossRef]
13. Arute, F.; Arya, K.; Babbush, R.; Bacon, D.; Bardin, J.C.; Barends, R.; Biswas, R.; Boixo, S.; Brandao, F.G.S.L.; Buell, D.A.; et al. Quantum supremacy using a programmable superconducting processor. *Nature* **2019**, *574*, 505–510. [CrossRef] [PubMed]
14. Castelvecchi, D. IBM Quantum Computer Passes Calculation Milestone. *Nature* **2023**, *618*, 656–657. [CrossRef] [PubMed]
15. Naaman, O.; Strong, J.A.; Fergusin, D.G.; Egan, J.; Bailey, N.; Hinkey, R.T. Josephson junction microwave modulators for qubit control. *J. Appl. Phys.* **2017**, *121*, 073904. [CrossRef]
16. Razmkhah, S.; Bozbey, A.; Febvre, P. Superconductor modulation circuits for Qubit control at microwave frequencies. In Proceedings of the ASEF Applied Superconductivity Conference, Honolulu, HI, USA, 23–28 October 2022; pp. 1–6. [CrossRef]
17. Patra, B.; van Dijk, J.P.G.; Subramanian, S.; Corna, A.; Xue, X.; Jeon, C.; Sheikh, F.; Juarez-Hernandez, E.; Esparza, B.P.; Rampurawala, H.; et al. A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4×32 Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers. In Proceedings of the 2020 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, USA, 16–20 February 2020; pp. 304–306. [CrossRef]
18. Van Dijk, J.P.G.; Patra, B.; Subramanian, S.; Xue, X.; Samkharadze, N.; Corna, A.; Jeon, C.; Sheikh, F.; Juarez-Hernandez, E.; Esparza, B.P.; et al. A Scalable Cryo-CMOS Controller for the Wideband Frequency-Multiplexed Control of Spin Qubits and Transmons. *IEEE J. Solid-State Circuits* **2020**, *55*, 2930–2946. [CrossRef]
19. Kudelin, I.; Groman, W.; Ji, Q.-X.; Guo, J.; Kelleher, M.L.; Lee, D.; Nakamura, T.; McLemore, C.A.; Shirmohammadi, P.; Hanifi, S.; et al. Photonic chip-based low-noise microwave oscillator. *Nature* **2024**, *627*, 534–539. [CrossRef] [PubMed]
20. Carlson, A.B. *Communication Systems*, 3rd ed.; McGraw-Hill International Edition; McGraw-Hill: New York, NY, USA, 1988; ISBN 0-07-009960-X.
21. Van Dijk, J.P.G.; Patra, B.; Pellerano, S.; Charbon, E.; Sebastiano, F.; Babaie, M. Designing a DDS-Based SoC for High-Fidelity Multi-Qubit Control. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 5380–5393. [CrossRef]
22. Bergou, J.A.; Hillery, M. *Introduction to the Theory of Quantum Information Processing*; Springer: New York, NY, USA, 2013; ISBN 978-1461470915.

23. Gilbert, B. A DC-500MHz amplifier/multiplier principle. In Proceedings of the 1968 IEEE International Solid-State Circuits Conference Digest of Technical Papers, Philadelphia, PA, USA, 14–16 February 1968; Volume XI, pp. 114–115.
24. Gilbert, B. A Precise Four-Quadrant Multiplier with Subnanosecond Response. *IEEE J. Solid-State Circuits* **1968**, *3*, 356–373. [CrossRef]
25. Jones, H.E. Dual Output Synchronous Detector Utilizing Transistorized Differential Amplifiers. U.S. Patent 3,241,078; filed 18 June 1963, issued 15 March 1966,
26. Lee, T. Tales of the Continuum: A Subsampled History of Analog Circuits. *IEEE Solid-State Circuits Soc. Newsl.* **2007**, *12*, 38–51. [CrossRef]
27. Bonfanti, A.; Tedesco, A.; Samori, C.; Lacaita, A. A 15-Ghz Broad-Band ÷2 Frequency Divider in 0.13-µm CMOS for Quadrature Generation. *IEEE Microw. Wirel. Compon. Lett.* **2005**, *15*, 724–726. [CrossRef]
28. Seungsoo, K.; Hyunchol, S. A 0.6–2.7 GHz Semidynamic Frequency Divide-by-3 Utilizing Wideband RC Polyphase Filter in 0.18µm CMOS. *IEEE Microw. Wirel. Compon. Lett.* **2008**, *18*, 701–703. [CrossRef]
29. Sanderson, D.I.; Svitek, R.M.; Raman, S. A 5-6-GHz polyphase filter with tunable I/Q phase balance. *IEEE Microw. Wirel. Compon. Lett.* **2004**, *14*, 364–366. [CrossRef]
30. Rabaey, J.M.; Chandrakasan, A.; Nikolic, B. *Digital Integrated Circuit—A Design Perspective*, 2nd ed.; Prentice Hall: Hoboken, NJ, USA, 2002; ISBN 978-0130909963.
31. Luo, J.; Zhang, L.; Wang, Y.; Yu, Z. Behavioral Analysis and Optimization of CMOS CML Dividers for Millimeter-Wave Applications. *IEEE Trans. Circuits Syst. II Express Briefs* **2015**, *62*, 256–260. [CrossRef]
32. Zhu, M.; Zhao, D. Geometric Analysis and Systematic Design of Millimeter-Wave Low-Power Frequency Dividers in 65-nm CMOS. *IEEE Access* **2020**, *8*, 20658–20665. [CrossRef]
33. Gira, G.; Ferraro, E.; Borgarino, M. On the VCO/Frequency Divider Interface in Cryogenic CMOS PLL for Quantum Computing Applications. *Electronics* **2021**, *10*, 2404. [CrossRef]
34. Kelly, R.D. Electronic Circuit Analysis and Design by Driving-Point Impedance Techniques. *IEEE Trans. Educ.* **1970**, *E-13*, 154–167. [CrossRef]
35. Razavi, B. *RF Microelectronics*, 2nd ed.; Prentice Hall: Hoboken, NJ, USA, 2012; ISBN 978-0-13-713473-1.
36. Bardin, J.C.; White, T.; Giustina, M.; Satzinger, K.J.; Arya, K.; Roushan, P.; Chiaro, B.; Kelly, J.; Chen, Z.; Burkett, B.; et al. Design and Characterization of 28nm Bulk-CMOS Cryogenic Quantum Controller Dissipating Less Than 2mW at 3K. *IEEE J. Solid-State Circuits* **2019**, *54*, 2043–3060. [CrossRef]
37. Xue, X.; Patra, B.; van Dijk, J.P.G.; Samkharadze, N.; Subramanian, S.; Corna, A.; Wuetz, B.P.; Jeon, C.; Sheikh, F.; Juarez-Hernandez, E.; et al. CMOS-based cryogenic control of silicon quantum circuits. *Nature* **2021**, *593*, 205–210. [CrossRef] [PubMed]
38. Park, J.-S.; Subramanian, S.; Lampert, L.; Mladenov, T.; Klotchkov, I.; Kurian, D.J.; Juarez-Hernandez, E.; Perez-Esparza, B.; Kale, S.R.; Beevi, K.T.A.; et al. A Fully Integrated Cryo-CMOS SoC for Qubit Control in Quantum Computers Capable of State Manipulation, Readout and High-Speed gate Pulsing of Spin Qubits in Intel 22nm FFL FinFET Technology. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 13–22 February 2021; Session 13. [CrossRef]
39. Ladvanszky, J.; Schultes, G. Noise Figure Minimization of RC Polyphase Filters. In Proceedings of the European Conference on Circuits Theory and Design, Cracow, Poland, 1–4 September 2003.
40. Teo, T.H.; Xiong, Y.-Z. Design of I-Q down-converter in CMOS for wireless network application. In Proceedings of the International Conference on Solid-State Devices and Material, Kobe, Japan, 12–15 September 2005; pp. 934–935. [CrossRef]
41. Kang, K.; Minn, D.; Bae, S.; Lee, J.; Kang, S.; Lee, M.; Song, H.-J.; Sim, J.-Y. A 40-nm Cryo CMOS Quantum Controller IC for Superconducting Qubit. *IEEE J. Solid-State Circuits* **2022**, *57*, 3274–3287. [CrossRef]
42. Frank, D.J.; Chakraborty, S.; Tien, K.; Rosno, P.; Fox, T.; Yeck, M.; Glick, J.A.; Robertazzi, R.; Richetta, R.; Bulzacchelli, J.F.; et al. A Cryo-CMOS Low-Power Semi-Autonomous Qubit State Controller in 14nm FinFET Technology. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 20–26 February 2022; Session 22. [CrossRef]
43. Horowitz, V.R.; Alemán, B.J.; Christle, D.J.; Cleland, A.N.; Awschalom, D.D. Electron spin resonance of nitrogen-vacancy centers in optically trapped nanodiamonds. *Proc. Natl. Acad. Sci. USA* **2012**, *109*, 13493–13497. [CrossRef]
44. Bardin, J.; Slichter, D.H.; Reilly, D.J. Microwave in Quantum Computing. *IEEE J. Microw.* **2021**, *1*, 403–427. [CrossRef]