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Mechanisms of step-stress degradation in Carbon-doped 0.15 μm AlGaN/GaN HEMTs for power RF applications

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***Abstract*—We discuss the degradation mechanisms of C-doped 0.15-μm gate AlGaN/GaN HEMTs tested by drain step-stress experiments. Experimental results show that these devices exhibit cumulative degradation effects during the step stress experiments in terms of either (*i*) transconductance (g_m) decrease without any threshold-voltage (V_T) change under OFF-state stress, or (*ii*) both V_T and g_m decrease under ON-state stress conditions. To aid the interpretation of the experiments, two-dimensional hydrodynamic device simulations were carried out. Based on obtained results, we attribute the g_m decrease accumulating under OFF-state stress to hole emission from C_N acceptor traps in the gate-drain access region of the buffer, resulting in an increase in the drain access resistance. On the other hand, under ON-state stress, channel hot electrons are suggested to be injected into the buffer under the gate and in the gate-drain region where they can be captured by C_N traps, leading to V_T and g_m degradation, respectively.**

***Index Terms*—GaN HEMTs, Step Stress, Carbon Doping, Hot Electrons, Reliability.**

I. Introduction

Gallium Nitride (GaN)-based high electron mobility transistors (HEMTs) are considered to be a key enabling technology for high frequency communication systems [1], [2]. High mobility and breakdown voltage of GaN-based devices are fundamental physical properties that allow realizing highly efficient power amplifiers [3], [4]. Short channel length (i.e., <1μm) GaN HEMTs are pursued to achieve the high f_T and f_{max} required for microwave operation. However, shortening the gate length affects the electrostatic integrity of the device due to undesirable short-channel effects (SCEs) with detrimental effect on the linear power gain. Moreover, a large breakdown voltage is required to increase the RF output power. To keep SCEs under control and to increase the breakdown voltage, foreign impurities are introduced in the GaN buffer underneath the channel layer so as to pin the Fermi-level well below the conduction band edge, hence reducing buffer conductivity [5], [6].

The most widely employed impurity species in GaN RF HEMTs is iron (Fe) [6], while carbon (C) is more generally used in power devices for switching converters [7]. However, due to similarity of HEMT epitaxial layers growth conditions for both RF and power applications, C can also be incorporated as background impurity in nominally Fe-doped only buffer [8]. C is also being investigated as an alternative to Fe as buffer doping species (i.e., it is intentionally incorporated) for RF applications as well [9]. Despite GaN HEMTs complying with stability/reliability requirements of commercial applications have already been demonstrated, a deeper assessment of the related limiting mechanisms is required for the further development of the technology [10].

In this work, we present results from OFF- and ON-state drain step-stress tests on 0.15-μm gate C-doped AlGaN/GaN HEMTs, extending a recent conference paper of ours [9] by providing a more complete assessment of the proposed physical degradation mechanisms. Distinctive degradation modes are in

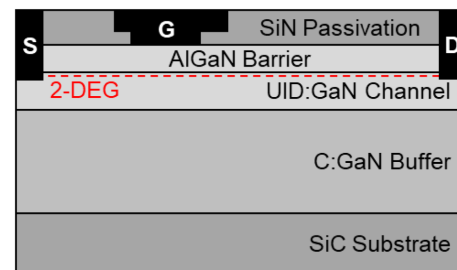

Fig. 1. Sketch of the 0.15 μm AlGaN/GaN C-doped HEMT under study in this work.

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fact pointed out by our measurements for OFF-state and ON-state stresses and attributed, also with the aid of simulation results, to the different charging mechanisms of C-related acceptor traps in the C-doped buffer for the two stress conditions.

Specifically, OFF-state degradation is shown to be characterized by a transconductance (g_m) decrease, especially in the high-current regime, which is attributed to hole emission from C-related acceptors and the consequent increase in the drain access resistance. ON-state stress instead results in threshold-voltage (V_T) increase as well as g_m decrease (both peak and high-current values), which can be explained by the injection of channel hot electrons (CHEs) into the buffer and to the surface, and consequent electron trapping into C-related acceptors and surface traps, respectively.

Since dominant C-related traps are C_N levels at 0.9 eV from the GaN valence band, i.e., at 2.5 eV from the conduction band, they “naturally” behave as hole traps, by emitting holes when the depletion region in the weakly p-type buffer widens in response to the negative gate-drain voltage applied under the OFF-state stress conditions. If emitted holes do not exit from the device or recombine with electrons, they can be re-trapped by C_N levels as the OFF-state stress bias is removed, leading to a long-time-constant drain current (and transconductance) recovery, which does not necessarily finish before the application of the subsequent stress step.

On the other hand, ON-state stress completely perturbs this quasi-equilibrium picture because of the injection of channel electrons into the buffer. Part of these electrons can be trapped by neutral C_N levels. The attending electron-hole recombination inside the traps leads to a virtually permanent negative charge buildup, owing to the 2.5 eV offset from the conduction band, that can only be recovered by high temperature or suitable illumination.

The paper is organized as follows. In Section II, a description of the tested devices and of the step-stress measurement setup is provided. In Section III, we present the results of the stress characterizations. In Section IV, we provide the simulation results supporting the interpretation of the observed experimental behavior. Section V draws the conclusions of this work.

II. Devices and Experimental Setup

Devices under test (DUTs) are Schottky-gate AlGaN/GaN HEMTs with 0.15-μm gate length (L_G) and 4-μm long drain-to-source spacing (L_{SD}), fabricated onto SiC wafers and featuring a C-doped GaN buffer layer for achieving a high voltage-handling capability and a 100-nm undoped GaN channel to minimize current-collapse effects [9]. DUTs were fabricated by Leonardo on commercial wafers. Key performance parameters are as follows: f_T = 20.4 GHz, f_{max} = 43 GHz, maximum power gain G_{max}=19 dB (at 5.5 GHz), output power P_{out}= 7 W/mm (at 5.5 GHz), drain efficiency DE = 70% (at 5.5 GHz). Figure 1 shows a sketch of the device cross-section.

DC drain-current (I_D) vs gate-source-voltage (V_{GS}) curves were acquired at constant drain-source voltage (V_{DS}) prior to applying the step-stress sequence, representing the curve labeled ($V_{GS,STR}$, $V_{DS,STR}$) = (0, 0) V in the plots. DUTs were submitted to both OFF-state and ON-state step-stress tests by

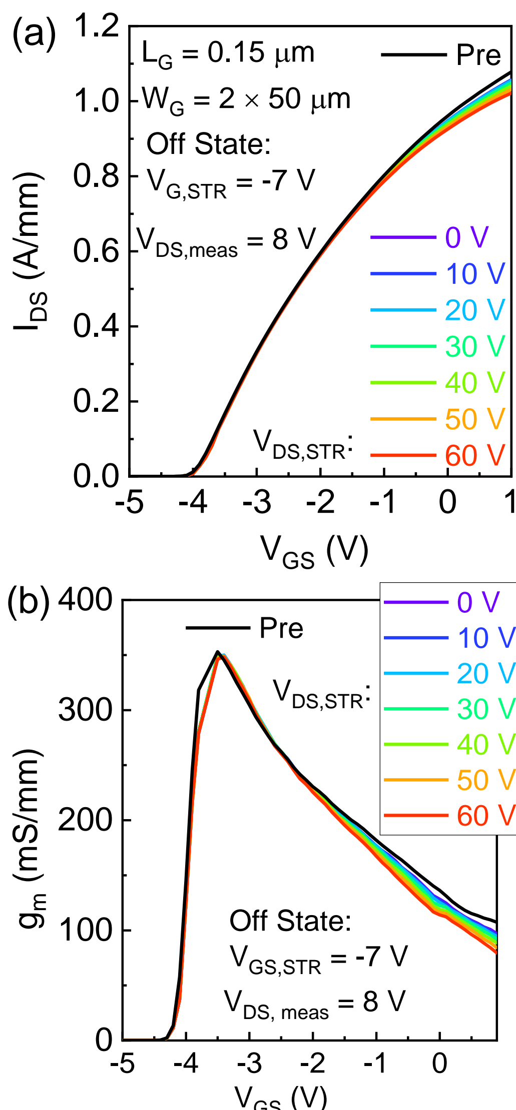

Fig. 2. (a) Drain-current (I_D) and (b) transconductance (g_m) vs gate-source-voltage (V_{GS}) curves measured after each step of the drain step-stress experiment carried out on the DUTs under OFF-state conditions.

applying either $V_{GS,STR}$ = –7 V or V_{GS} = 0 V, respectively. $V_{DS,STR}$ was ramped from 0 V to 60 V in both conditions with 5-V steps. Each stress step was maintained for 120 s followed by a 300-s unbiased step after which a complete DC I_D-V_{GS} is acquired.

III. Stress Experiments

Key experimental results are shown in Figs. 2 and 3, reporting the I_D-V_{GS} and g_m-V_{GS} curves measured after each stress step under either OFF-state, see Fig. 2, or ON-state conditions, see Fig. 3.

The OFF-state stress resulted, after the final step at ($V_{GS,STR}$, $V_{DS,STR}$) = (–7, 60) V in a small $g_{m,max}$ (at V_{DS} = 8 V) drop of 1.2%, see Fig. 2(b), while V_T (the V_{GS} when I_{DS} = 1 mA/mm at V_{DS} = 8 V) showed no appreciable drift, see Fig. 2(a). Conversely, the ON-state stress induced after the ($V_{GS,STR}$, $V_{DS,STR}$) = (0, 60) V step a 9.6% g_m decrease, see Fig. 3(a), accompanied by a 0.32 V V_T increase, see Fig. 3(b). Devices

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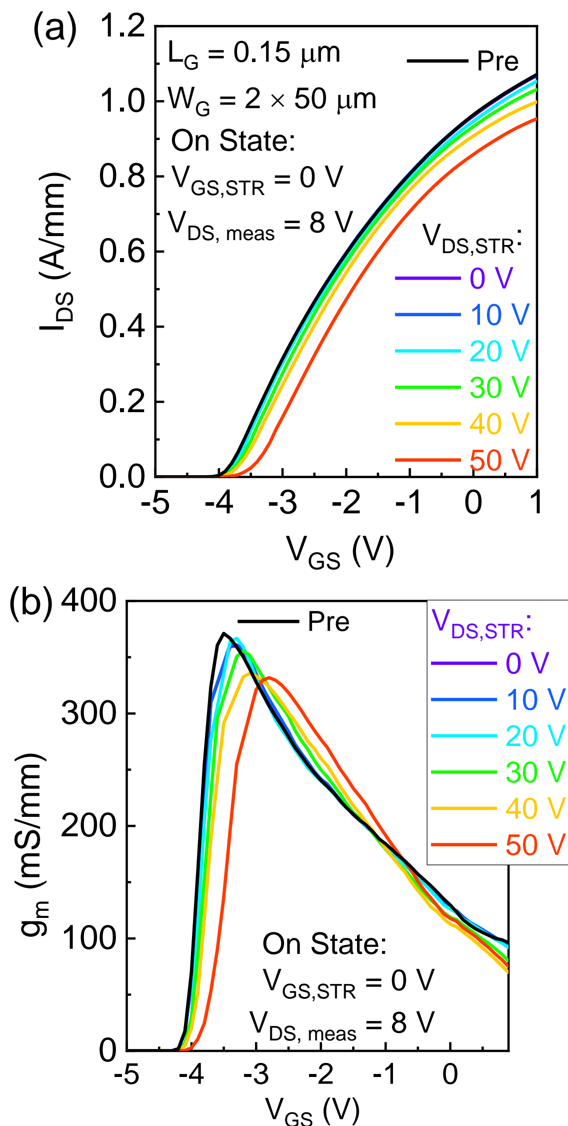

Fig. 3. (a) Drain-current (I_D) and (b) transconductance (g_m) vs gate-source-voltage (V_{GS}) curves measured after each step of the drain step-stress experiment carried out on the DUTs under ON-state conditions.

fabricated with the same processing onto wafers with Fe-doped buffer and subjected to same step-stress experiments exhibit much smaller degradation effects for both OFF- and ON-state stress conditions, indicating that degradation effects observed in the step-stress experiments are related to C-doping in the buffer [9].

OFF-state degradation can be explained as follows. Prolonged bias in the OFF-state is well-known to trigger dispersion effects related to C-doping [7], [11]–[13], which can be explained by the 'hole-redistribution' model as long as the source-drain punch-through current remains negligible [14]. According to the latter, during the OFF-state stress, holes are predominantly emitted from C_N states within the gate-drain depleted region of the buffer, move to the gate-source and the bottom regions of the buffer and get captured by the same C_N states therein, so that they need to be re-emitted from the latter traps, move back and then be re-captured in gate-drain region, in order for the pre-stress conditions to be recovered, as the stress bias is removed. The hole emission process from C_N states has time constants in the order of hundreds of seconds at room temperature [14], [15]. Therefore, after each stress step, a full recovery from degradation cannot be achieved within the 300-s unbiased phase. As a result, degradation accumulates leading to an increasing g_m drop, especially in the high V_{GS} regime, see Fig. 2(b). The negligible V_T drift observed during the OFF-state tests indicates that no significant charge build-up occurs below the gated region of the device. This result can also be interpreted with the 'hole-redistribution' model as being due to the complete charge redistribution below the gate contact following the unbiased phase after each stress step. This point is further clarified in Sec. IV.

Results in Fig. 3 indicate a more pronounced degradation after ON-state stress compared to the OFF-state case. Moreover, not only $g_{m,max}$ incrementally decreases after each stress step but also V_T drifts significantly. At $V_{GS,STR}$ = 0 V, significant current flow occurs in the channel, and energetic electrons can acquire enough energy to spill over to the buffer. When significant electron injection occurs in the C-doped buffer, the unoccupied C_N states can easily trap injected electrons, resulting in an increased negatively ionized trap density, in turn resulting in reduced 2DEG conductivity [16], [17]. Depending on whether electron trapping happens below the gate or/and in the gate-to-drain access region, a V_T increase or a $g_{m,max}$ drop, or both effects, is/are induced [5], [18]. Both parameters are found to degrade in Fig. 3, indicating that CHE injection must have interested both buffer regions. This hypothesis is further confirmed by the fact that this degradation is non-recoverable and that accumulates over each stress step, see Fig. 3. In fact, under negligible electron injection conditions in the buffer (as in the OFF-state case considered above) C_N states act as hole traps, i.e. they change their charge state by interacting with the valence band (emitting and capturing holes) [14]. Instead, when significant electron injection occurs (as in the ON-state case) C_N states can act as electron traps. The significant energy depth of this level with respect to the conduction band renders the emission of the trapped electrons virtually impossible by simple thermal emission at room temperature. From this, one can deduce that electron trapping into C_N states gives rise to a semi-permanent degradation. Recovery from this phenomenon can only be achieved by applying a high-temperature recovery step and/or by shining UV light to enhance electron emission from traps or generate an excess of holes to promote electron-hole recombination within the traps.

It is important to highlight that both OFF- and ON-state degradation effects observed in the step-stress experiments shown here are peculiar of C-doped devices. Even in Fe-doped devices the negative charge stored within the buffer increases during both OFF-state and ON-state stress [9]. This happens as a result of electron trapping into the Fe-related acceptor traps at 0.56 eV from the conduction band. However, in the case of Fe doping, an unbiased phase of 300 s following each stress step is long enough to completely revert this process, thanks to the ≈10-ms time constant characterizing electron emission to the conduction band from the Fe states [19].

We eventually point out that the ON-state stress results presented here do not contradict the 'hole-redistribution' model, as in fact this model can only be applied for stress bias conditions under which C doping is able to effectively avoid

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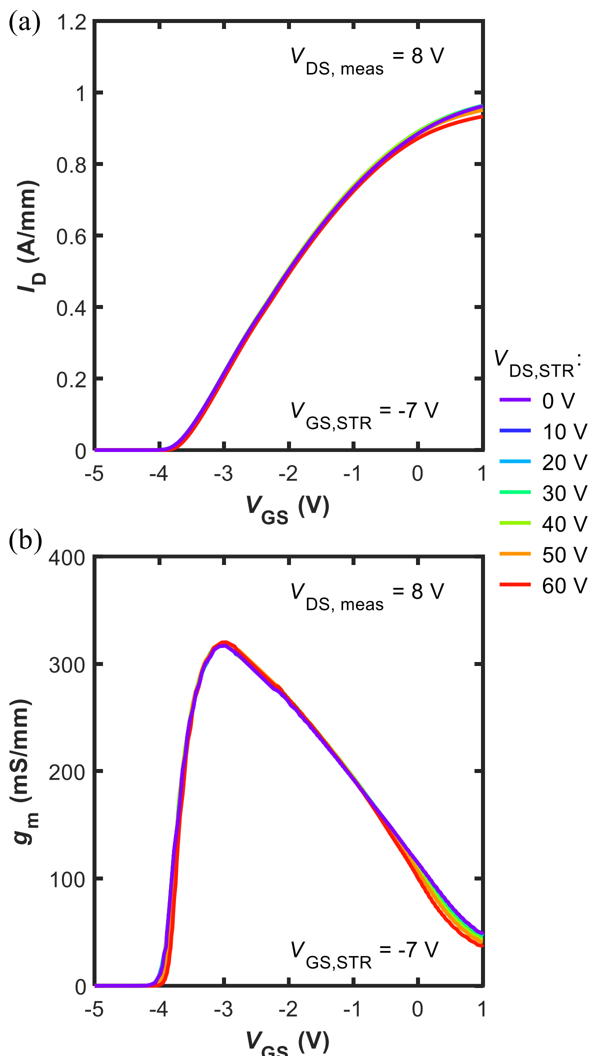

Fig. 4. Simulated (a) drain-current (I_D) and (b) transconductance (g_m) vs gate-source-voltage (V_{GS}) curves prior to stress (0 V curve) and after 120-s OFF-state stress, i.e., $V_{GS,STR}$ = –7 V, $V_{DS,STR}$ = 10-60 V, followed by 300-s recovery at (0, 0) V.

significant electron injection from the source and/or from the substrate into the buffer [14].

IV. Stress Simulations

To validate the hypothesis regarding the physical mechanisms formulated in Sec. III, two-dimensional (2D) numerical device simulations were performed with the SDevice™ simulator [20]. To take hot electron effects into account in a more accurate way, charge transport was modelled by means of the hydrodynamic equations. Other models (piezoelectric polarization charge, trap dynamics, etc.) were employed analogously to what done in our previous works [21]. C doping in the GaN buffer was modeled by considering a dominant deep acceptor trap at 0.9 eV above E_V partially compensated by a shallow donor trap at 0.11 eV below E_C [22]. The adopted C doping model, described more in detail in [22], is consistent with the current understanding of the energy levels associated with C introduction into GaN [23], described succinctly as follows. While early DFT calculations based on LDA and GGA approximations predicted the substitutional C_N state to be a shallow acceptor [24], more accurate DFT calculations using the HSE functional

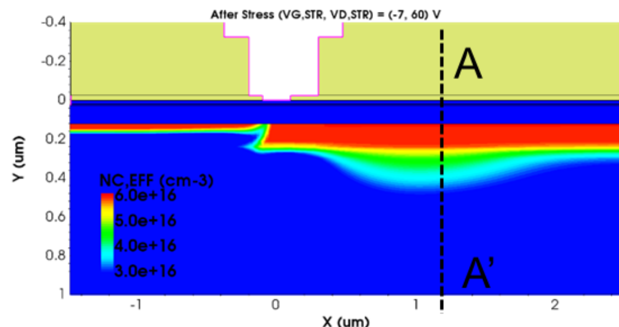

Fig. 5. Simulated net ionized acceptor trap density ($N_{C,EFF} = N_{ACC}^{-} - N_{DON}^{+}$) immediately after stress (i.e., prior to recovery) under OFF-state stress, i.e., ($V_{GS,STR}$, $V_{DS,STR}$) = (–7, 60) V. Cutline A-A' used in Figs. 6 and 7 is indicated.

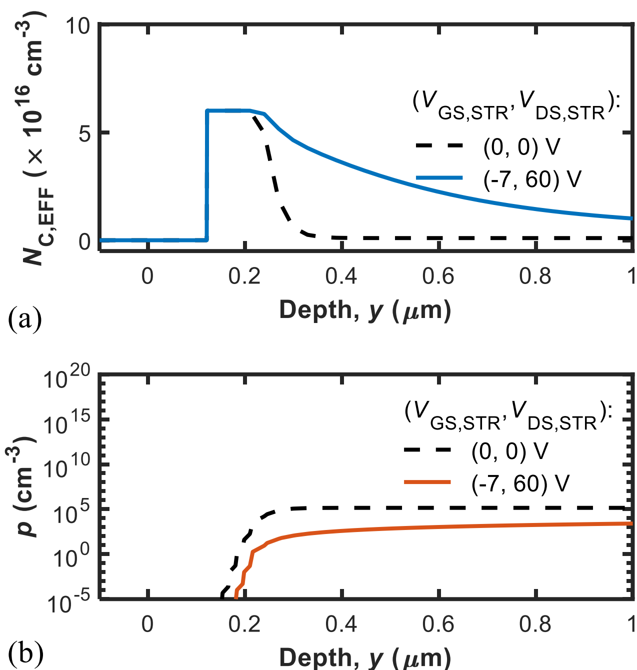

Fig. 6. Simulated (a) $N_{C,EFF}$ and (b) p along the vertical cutline A-A' (see Fig. 5) prior to and after OFF-state stress. Increase of $N_{C,EFF}$ near the surface of the buffer (i.e., near the channel/buffer interface) correlates with depletion region widening and consequent hole emission from traps.

consistently predicted the C_N acceptor level in the 0.9-1.1 eV range above the valence band maximum [25]. This is in good agreement with extensive experimental findings, including *(i)* measurement of thermally activated reduction in the resistivity of carbon-doped GaN [26]; *(ii)* observation of p-type conductivity and its thermal activation energy [27]; *(iii)* a hole trap detection by DLTS and minority carrier transient spectroscopy [28]; *(iv)* results from photocapacitance, pulsed photoionization, and DLOS [29]; *(v)* yellow luminescence studies [28], [30].

The adopted active trap concentrations were 8×10^{16} cm^{-3} and 2×10^{16} cm^{-3}, for C-related acceptors and donors, respectively. Poole-Frenkel enhancement of hole emission from acceptor traps was included in the setup [15].

To provide insight into the observed degradation effects, we mimicked measurement conditions as follows. V_{GS} and V_{DS} were kept constant to their stress values for 120 s at each ($V_{GS,STR}$, $V_{DS,STR}$) condition. Recovery was performed after stress for 300

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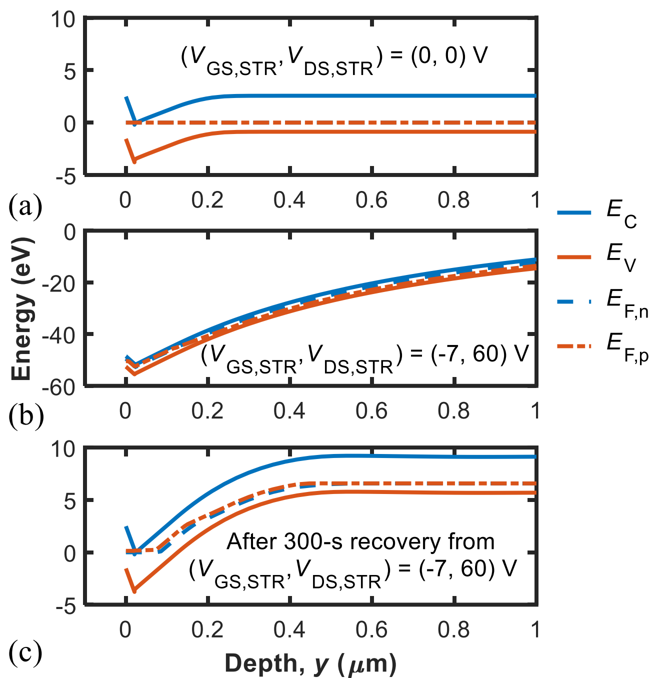

Fig. 7. Simulated band diagrams along the vertical cutline A-A' (see Fig. 5): (a) at (0, 0) V, (b) at the end of the 120-s stress at (–7, 60) V and (c) at the end of the subsequent 300-s rest phase at (0, 0) V. Stress increases the depletion region width at channel/buffer interface which is not completely recovered after the 300-s phase, leading to the g_m drop shown in Fig. 4.

s by grounding gate and drain contacts (source and substrate where grounded during the whole simulation). I_D-V_{GS} curves at V_{DS} = 8 V were acquired after the recovery interval was completed. Ramp time during I_D-V_{GS} acquisition was 1 s.

Notice that for ensuring convergence of the simulations, the stress steps could not be applied sequentially one after the other. Moreover, since the focus of this work is on the impact of buffer traps on degradation, trapping in the passivation layer was not included in the simulation setup, which however might contribute to the total degradation after ON-state stress [31]. For these reasons, the simulations tend to underestimate the total amount of degradation compared to the actual data. Nevertheless, simulation results still allow to obtain a clear picture of the physical mechanisms taking place in the buffer during stress and as such the adopted simplification does not affect the intepretation.

Figure 4 shows the simulation results under the OFF-state in terms of I_D- and g_m-V_{GS} curves. These curves are taken up to $V_{DS,STR}$ = 60 V with 10-V step. At first glance one can see how simulations allow to qualitatively reproduce the experimental features related to OFF-state step stress. Particularly, Fig. 4 shows a small $g_{m,max}$ degradation, a more appreciable g_m drop at high V_{GS} and a negligible V_T shift, in agreement with experiments illustrated in Fig. 2. Figure 5 shows the contour plot of net ionized trap concentration ($N_{C,EFF}$) in the OFF-state stress condition taken right after 120-s of stress at V_{DS} = 60 V. As it can be seen in Fig. 5, under OFF-state stress the negative charge buildup due to C_N acceptors extends through the upper portion of the gate-drain region and is correlated to the depletion of holes (emitted by the traps). This is further shown in Fig. 6, which plots $N_{C,EFF}$ and the free hole density (p) along the cutline A-A' shown in Fig. 5 in the gate-drain access region.

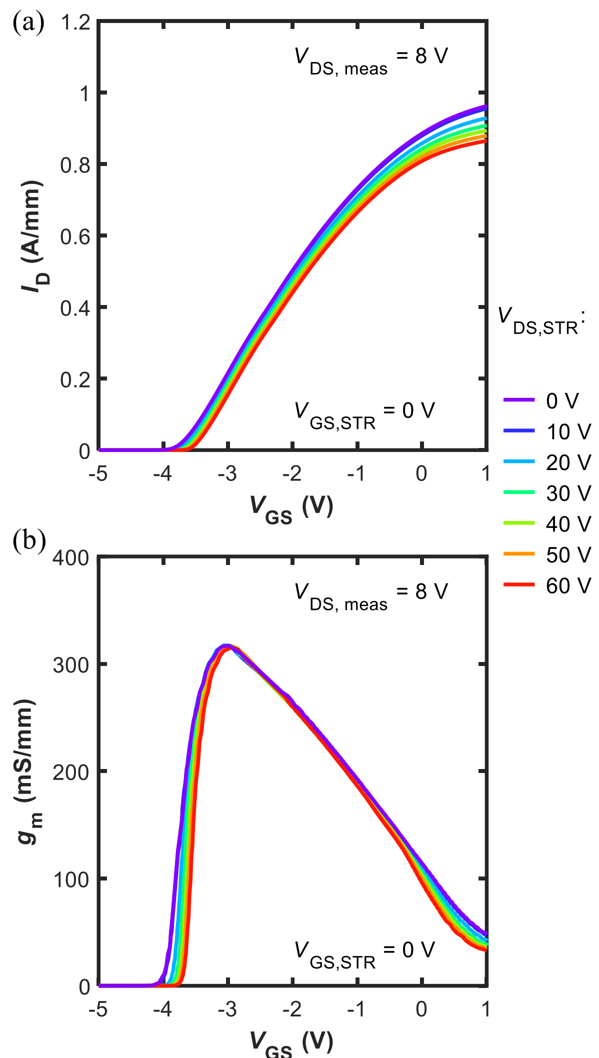

Fig. 8. Simulated (a) drain-current (I_D) and (b) transconductance (g_m) vs gate-source-voltage (V_{GS}) curves prior to stress (0 V curve) and after 120-s ON-state stress, i.e., $V_{GS,STR}$ = 0 V, $V_{DS,STR}$ = 10-60 V, followed by 300-s recovery at (0, 0) V.

As it can be noted, $N_{C,EFF}$ increases compared to the pre-stress conditions and simultaneously p decreases, confirming that the negative charge buildup is due to hole emission following the depletion region widening. Figure 7 shows the band diagram along the same A-A' cutline used in Fig. 6, (a) at (0, 0) V bias prior to stress application, (b) at the end of the 120-s stress phase at (–7, 60) V and (c) at the end of the subsequent 300-s rest phase at (0, 0) V. The OFF-state stress increases the depletion region in the buffer as indicated by the enlargement and widening of the upward band bending in Fig. 7(b), compared to the pre-stress conditions illustrated by Fig. 7(a). During the subsequent 300-s rest phase at (0, 0) V, the buffer depletion region shrinks but does not recover to pre-stress conditions, as it can be appreciated by comparing Fig. 7(c) with Fig. 7(a). This incomplete recovery explains the cumulative effect of stress steps in terms of the increasing g_m drop as observed in the measurements, see Fig. 2(b).

Figure 8 shows the simulated I_D- and g_m-V_{GS} curves after ON-state stress. Simulation results show a positive V_T shift, in agreement with the experimental findings shown in Fig. 3. However, simulations underestimate the degradation of $g_{m,max}$

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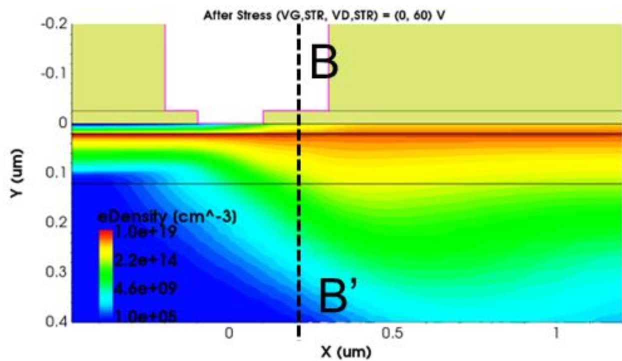

Fig. 9. Simulated electron density (n) immediately after stress (i.e., prior to recovery) under ON-state stress, i.e., ($V_{GS,STR}$, $V_{DS,STR}$) = (0, 60) V. Cutline B-B' used in Fig. 9 is indicated.

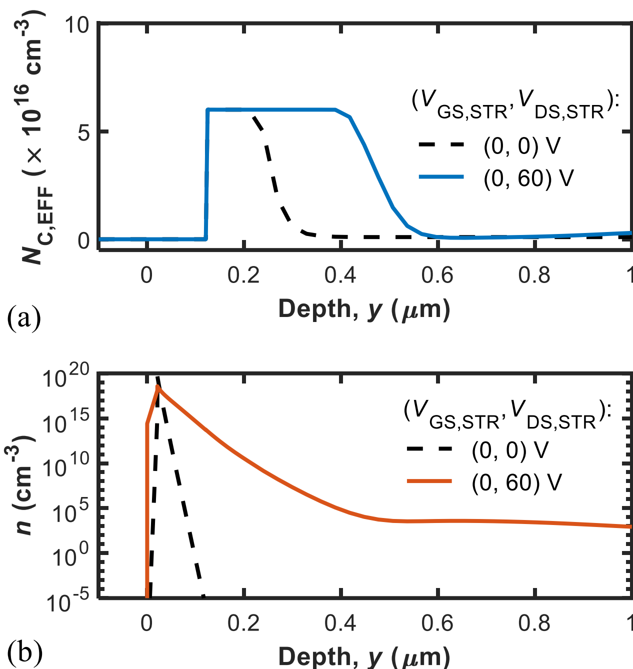

Fig. 10. Simulated (a) $N_{C,EFF}$ and (b) n along the vertical cutline B-B' (see Fig. 9) prior to and after ON-state stress. Increase of $N_{C,EFF}$ near the surface of the buffer (i.e., near the channel/buffer interface) correlates with electron injection in the same region from the 2DEG.

compared to the experimental data in Fig. 3; we attribute this discrepancy to the neglected hot electrons trapping at the device surface and in the passivation which can contribute to the total degradation [31]. Hot electrons can also be trapped in the AlGaN bulk and at AlGaN/GaN interface.

Figure 9 shows shows the contour plot of the free electron density (n) in the ON-state stress condition taken right after stress 120-s of stress at V_{DS} = 60 V. In this case, the degradation observed in Fig. 8 can be understood as being due to the injection of electrons into the buffer, as clearly shown in Fig. 9. Figure 10 further confirms the correlation between the negative charge build-up with the electron injection in the buffer during ON-state stress, by showing $N_{C,EFF}$ and n along the cutline B-B' (indicated in Fig. 9). In this case, $N_{C,EFF}$ below the gate increases during stress due to trapping of the hot electrons injected from the channel.

V. Recovery Experiments

To confirm the validity of the interpretation we carried out three types of recovery experiments on DUTs previously subjected to OFF-state or ON-state step-stress tests (described in Section III). These recovery experiments were carried out undeer the following conditions: *i)* long term (42 days) at room temperature; *ii)* short term at high-temperature (150 and 200 °C); *iii)* with UV-illumination (385, 365, and 265 nm) for 5 minutes.

Figure 11 shows the results of these analyses. After long term (42 days) storage at room temperature, DUTs subjected to OFF-state step stress showed complete recovery, see Fig. 11(a) and (b). Full recovery is consistent with the redistribution (and re-capture) of holes first emitted during stress [14]. Since full

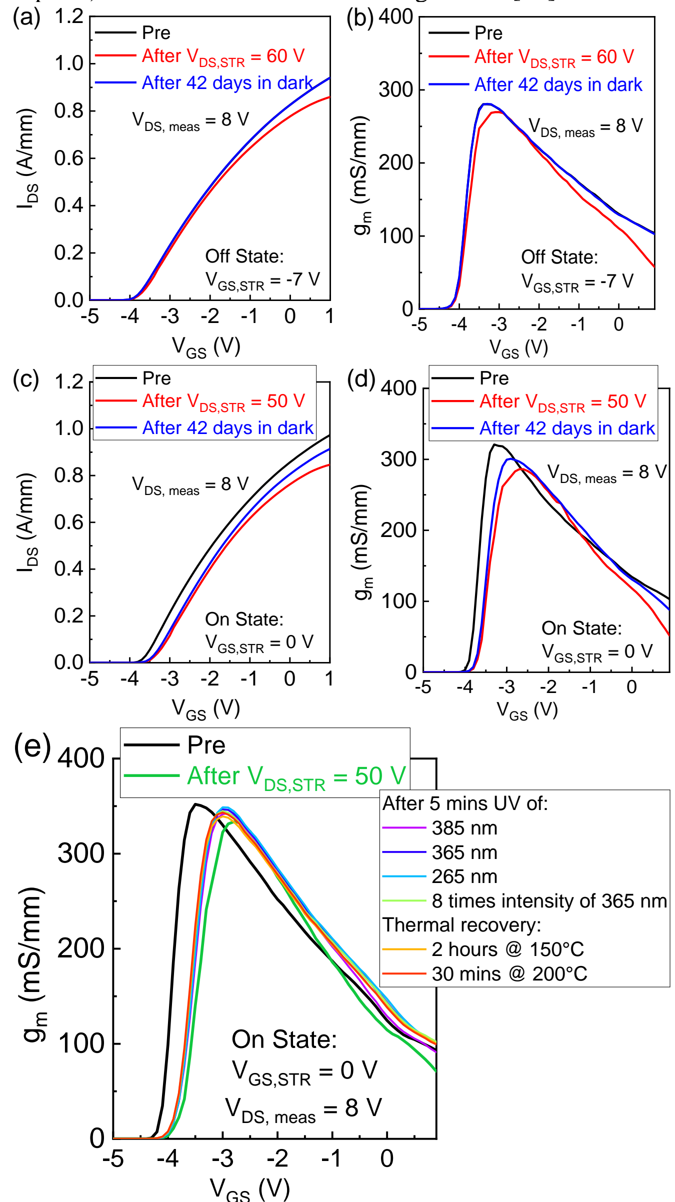

Fig. 11. (a, c) Drain-current (I_D) and (b, d) transconductance (g_m) vs gate-source-voltage (V_{GS}) curves measured after long term (42 days) recovery at room temperature on DUTs subjected to OFF-state (a, b) and ON-state (c, d) step-stress. (e) Short term, high temperature and with UV-illumination recovery of g_m–V_{GS} carried out on DUTs subjected to ON-state step stress.

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recovery was achieved at room temperature, experiments of type *ii)* and *iii)* were not carried out on devices stressed under OFF-state.

Conversely, DUTs subjected to ON-state step stress showed, after long term (42 days) room temperature storage, only partial recovery that mainly involved $g_{m,max}$ and high-current g_m, whereas V_T did not recover, see Fig. 11(c), (d). The partial recovery can be attributed to electron de-trapping from traps located at the device surface and/or in the passivation [31], whereas the remaning g_m degradation and lack of V_T recovery can be attributed to the hot electrons trapped in the C-related buffer traps.

Figure 11(e) shows the results of the recovery experiments corresponding to cases *ii)* and *iii)*, explained in the following. The short-term high temperature storage induces an almost complete $g_{m,max}$ recovery, due to a combination of thermal de-trapping of electrons from surface traps and accelerated redistribution of holes within the buffer [14]. The recovery experiments with UV-illumination led to complete $g_{m,max}$ recovery but no V_T recovery. This can be explained by the fact that the region under the gate contact is shielded from the photon flux by the gate and field plate metal, and as such the UV-illumination is not effective in assisting electron de-trapping from C_N traps located in this region. In other words, the C-related buffer traps under the gate remain negatively charged causing a non-recoverable positive V_T shift even under UV illumination.

VI. Conclusions

We presented results from drain step stress tests on 0.15-μm AlGaN/GaN HEMTs fabricated on wafers with C-doped buffer layers. Both OFF- and ON-state stress conditions were applied, finding a small g_m drop in the first case, whereas an enhanced g_m drop and positive V_T shift in the second one. Two-dimensional hydrodynamic device simulations were carried out as an aid in the interpretation of the results. Recovery experiments were also carried out at room-temperature, high temperature and under UV illumination.

Based on both stress and recovery experiments as well as on simulations, we conclude that:

1) The g_m drop under OFF-state stress conditions can be interpreted with the 'hole-redistribution' model as being due to hole emission from the C_N acceptor traps leading to increased negative charge stored in the gate-drain access region. The latter can accumulate during the step stress experiment as a result of the long time constants involved. Room-temperature storage of the DUT was found to induce a total recovery of stress effects, which is compatible with the 'hole-redistribution' model.

2) Both g_m and V_T degradation under ON-state stress conditions can be attributed to capture of CHEs by C_N traps in the buffer and by surface traps, inducing negative charge buildup in the buffer under the gate and within the gate-drain access region both in the buffer and at the surface. Long-term, room-temperature storage caused small recovery from g_m degradation, which can be attributed to electron de-trapping from surface traps. High-temperature and UV-illumination recovery experiments instead allowed almost complete recovery of g_m but not of V_T. Surface electron traps can effectively be depleted by the high-temperature storage, while C_N buffer acceptor traps in the gate-drain access region emit the trapped electrons with the aid of UV-illumination. Conversely, the region under the gate is shielded by the metal and UV-illumination is not effective in depleting the negative charge build-up due to electron trapping in C_N buffer states, explaining the permanent degradation of V_T.

Owing to the peculiarity of C doping, when C_N acceptors, that "naturally" behave as hole traps, are forced to capture electrons, as it can happen under ON-state conditions because of CHE injection into the buffer, the resulting negative charge buildup can appear permanent and be misinterpreted as a structural damage. This phenomenon should be characterized during the device-technology development and specifically taken into consideration, especially in short-gate HEMTs for high-frequency applications, for the optimization of C doping or the selection of the most suitable epitaxy, in order to properly trade off breakdown-voltage increase with tolerable, overall trapping effects.

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