A CMOS Pixelated Nanocapacitor Biosensor Platform for High-Frequency Impedance Spectroscopy and Imaging

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***Abstract*—We describe the realization of a fully-electronic label-free temperature-controlled biosensing platform aimed to overcome the Debye screening limit over a wide range of electrolyte salt concentrations. It is based on an improved version of a 90 nm CMOS integrated circuit featuring a nanocapacitor array, readout and A/D conversion circuitry, and an FPGA-based interface board with NIOS II soft processor. We describe the chip's processing, the mounting, the microfluidics, the temperature control system, as well as the calibration and compensation procedures to reduce systematic errors, which altogether make up a complete quantitative sensor platform. Capacitance spectra recorded up to 70 MHz are shown and successfully compared to predictions by FEM numerical simulations in the Poisson-Drift-Diffusion formalism. They demonstrate the ability of the chip to reach high upper frequency of operation, thus overcoming the low-frequency Debye screening limit at nearly physiological salt concentrations in the electrolyte, and allowing for detection of events occurring beyond the extent of the electrical double layer. Furthermore, calibrated multi-frequency measurements enable quantitative recording of capacitance spectra, whose features can reveal new properties of the analytes. The scalability of the electrode dimensions, inter-electrode pitch and size of the array make this sensing approach of quite general applicability, even in a non-bio context (e.g. gas sensing).**

***Index Terms*—biosensors, CMOS, high-frequency, imaging, impedance spectroscopy, nanoelectrodes**

I. Introduction

ELECTROCHEMICAL impedance spectroscopy (EIS) is a popular sensing technique, thanks to its capability to investigate different sample properties at different frequencies [1]. Miniaturization and monolithic integration of EIS sensors in CMOS technology is possible, enabling highly parallel sensing and readout [2][3][4][5][6][7] and recording and stimulation of cellular activity [8][9][10][11][12][13]. Within the field of capacitance biosensors [14], high sensitivity realizations have been presented, that enable the implementation of CMOS DNA sensor arrays [4][15], and even to reach zepto-Farad resolution [16][17].

In this context of integrated impedance biosensors, high frequencies of operation is a noted obstacle [18][19][20][21], which impedes overcoming the screening by the electrical double layer (EDL) and probing analytes far beyond one Debye length from the surface [22]. As a result of operation at relatively low frequencies, the response of existing systems is mostly sensitive to surface chemical processes and analytes in close proximity to the sensor's surface, that is within the EDL. Increasing the Debye length by lowering the electrolyte ionic strength is not a solution, because it can alter the biomolecule properties, or even denature them.

At physiological salt concentrations, high frequency operation can be achieved only by substantial reduction of parasitic impedance as enabled by advanced CMOS processes [23][24]. On top of that, also electrodes and electronics co-design is essential to implement successful high-resolution integrated biosensors [25]. Until now, very few platforms revealed the capability to operate at frequencies above 1MHz or as high as 50 MHz [2][23][26][27], combined with high-resolution real-time imaging of particles, cells, and emulsions.

Following the early demonstrations in [1], [2], [3], this work describes in detail the operating principle, key circuitry, advanced processing and improved system implementation, of a CMOS pixelated capacitance (bio)sensor platform aimed to enable massively-parallel (256x256 pixels) label-free imaging and high-frequency impedance spectroscopy (HFIS) beyond the dielectric relaxation cut-off frequency of the electrolyte up to nearly physiological salt concentrations.

Firstly, the principle of operation and circuitry and the chip and nanoelectrode fabrication process are described (Sections II and III, respectively). Chip assembly in an ad-hoc microfluidic setup is presented next in Section IV, including the realization of an appropriate chip socket. Then, the board and system assembly, including a controller to dynamically adapt/control the working temperature is discussed in Section V. Calibration and compensation procedures are applied (Sections VI and VII), to enable not merely qualitative but also reliable

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quantitative measurements verified by numerical simulations. Spectroscopic measurements in uniform environments (air, milliQ, electrolytes) and array statistics are discussed in Section VIII, and imaging properties are demonstrated in Section IX. Conclusions and outlook in Section X complete the paper.

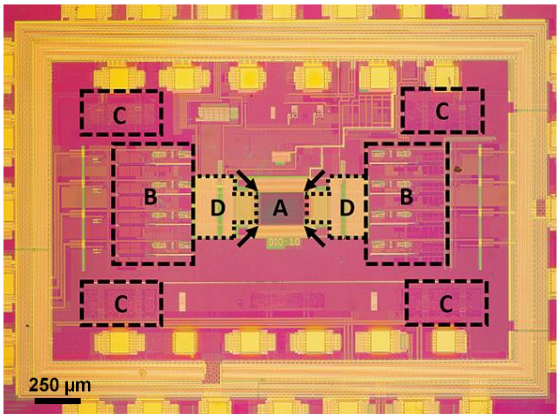

Fig. 1. Chip photo, showing the matrix of 256×256 nanoelectrodes (A), 4 temperature sensors (arrows), 8 A/D converters (B), 4×64 data accumulation registers (C), and 2×128 column read-out circuits (D). The chip size is 3.2×2.1 mm^2; the area in the image is 2.95×2.20 mm^2.

II. Concept and Chip Implementation

The core of the chip consists of 65,536 individualy addressable gold-copper nanoelectrodes of 90 nm nominal radius, arranged in a 256×256 array with 550nm×720nm, 600nm×720nm or 600nm×890nm column/row pitch (different chip versions). The chip has been designed for Charge Based Capacitance Measurements (CBCM) [28] at switching frequencies up to 300 MHz. Fig. 1 shows a chip photo, highlighting the main features. Fig. 2 shows the basic schematic of a sensor cell, a column read-out circuit, and the array architecture.

CBCM is implemented with two minimum-size (W/L = 200nm/90nm) switch transistors S_T and S_D per sensor cell, that repetitively charge and discharge the capacitance of a nanoelectrode, connected to the switching node, to the potentials V_T and V_D, respectively. S_T and S_D are controlled by off-chip generated non-overlapping clocks (Φ_T, Φ_D) with programmable frequency and pulse shapes. To avoid interference in ground return paths on the chip, Φ_T and Φ_D are imported on the chip as 2 differential clock pairs, that are routed differentially all the way to the row selection circuitry alongside the array, where the non-inverted clock signals are passed on to a selected row of sensor cells. The clock waveforms for measurements at 50 MHz switching frequency have 1 ns rise and fall times, 7 ns high times, and 10 ns delay between the Φ_T and Φ_D pulses.

A full row of 256 sensor cells is selected (e.g. row 2 in Fig. 2) by passing the clock signals Φ_T and Φ_D, and the discharge potential V_D, to the row's $\Phi_{T,m}$, $\Phi_{D,m}$ and $V_{D,k}$ terminals ($k = \lfloor m/2 \rfloor$, where $\lfloor \cdot \rfloor$ rounds down to the nearest integer; i.e. $\Phi_{T,2}$, $\Phi_{D,2}$ and $V_{D,1}$ in the example) via on-chip analog switches,

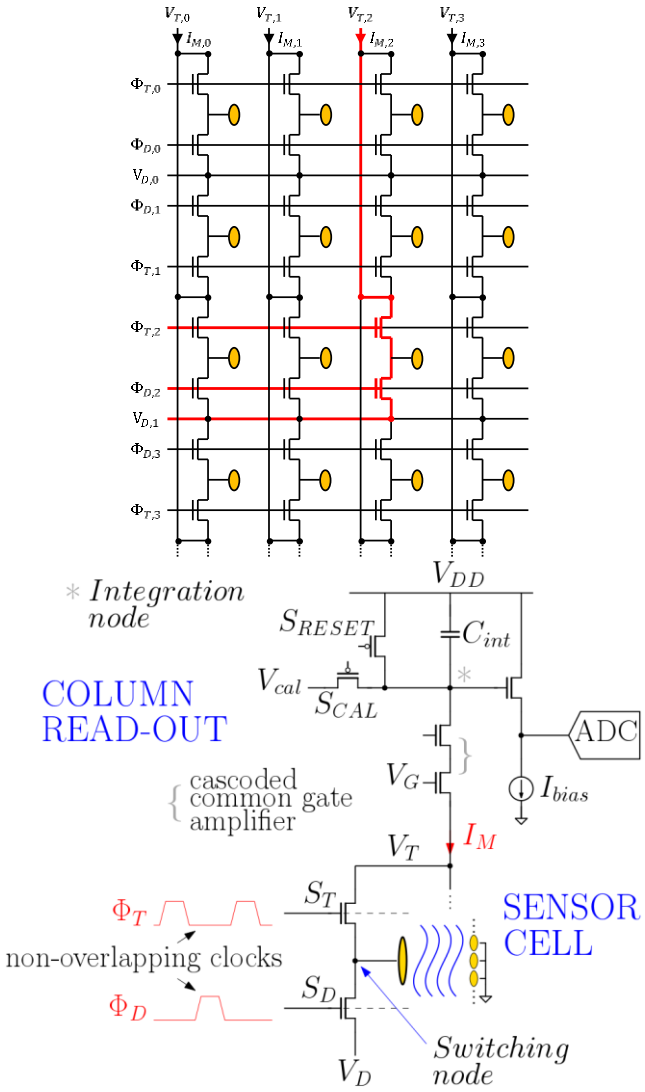

Fig. 2. Top: Array architecture, with a single sensor cell highlighted in red. Bottom: Schematic of a selected sensor cell, coupled to its column read-out circuit. Gold disks represent the nanoelectrodes. The cascoded common gate amplifier controls the column voltage V_T, and passes the column current I_M to the integration capacitor C_{int} (480 fF). I_M is equal to the average sensor cell current (averaged by the column's parasitic capacitance). At the end of a charge integration period (started by opening switch S_{RESET}), the ADC samples the voltage on the integration node (labeled *). Immediately after, it samples the calibration voltage V_{cal} (800 mV), passed to the integration node via switch S_{CAL}, and converts the difference of the 2 samples. This Correlated Double Sampling (CDS) scheme suppresses 1/f noise and drift in the A/D conversion path.

controlled by an on-chip row decoder. All other rows (i.e. rows 0, 1, 3, 4,… in the example) are disabled with a logic low DC potential on their respective $\Phi_{T,m}$ terminals.

The nanoelectrodes of the adjacent row, that shares the same $V_{D,k}$ line with the selected row (i.e., row 3 and line $V_{D,1}$ in the example), are made floating with a logic low DC potential on that row's $\Phi_{D,m'}$ terminal ($m' = 4\lfloor m/2 \rfloor - m + 1$; i.e. $\Phi_{D,3}$ in the example). This insulates these nanoelectrodes from the discharge potential V_D.

A "fluid" DC potential V_{FL} is put on the $V_{D,k'}$ lines of all other non-selected rows ($k' \neq k$; i.e. $V_{D,0}$, $V_{D,2}$, $V_{D,3}$,… in the example), and passed on to the nanoelectrodes by putting a logic high DC potential on the respective $\Phi_{D,m''}$ terminals

($\lfloor m''/2 \rfloor \neq k$; i.e. $\Phi_{D,0}$, $\Phi_{D,1}$, $\Phi_{D,4}$, $\Phi_{D,5}$,… in the example). These electrodes provide an AC return path for the modulation signal on the selected nanoelectrodes.

This selection scheme effectively constitutes a single large reconfigurable on-chip counter electrode, at a DC voltage V_{FL}, that is typically set to the time-averaged DC level of the modulation signal on the selected nanoelectrodes. With this row selection scheme and V_{FL} potential, the long-term net DC charge transport throught all nanoelectrode surfaces, mediated e.g. by redox-active species in the fluid, is always averaged out to zero, preventing unwanted electrochemical modifications of the electrode surfaces. This is an important prerequisite for long-term stable measurements in electrolytes.

The array and row-selection electronics of the chip version with 890nm row pitch are slightly modified: each row of nanoelectrodes has its own selectable discharge line, so that the nanoelectrodes of both non-selected rows adjacent to the selected row can be connected to V_{FL}. This way, the selected nanoelectrodes are surrounded by a fully symmetrical AC return path, at the expense of a slightly larger sensor cell area.

In the array of the chip version with 550nm column pitch, odd and even columns are placed mirror-imaged with respect to each other. This way, groups of 2×2 sensors cells can share a single discharge line contact. This gives the smallest sensor cell area, at the expense of non-identical misalignment sensitivity of the odd and even sensor cells of a selected row.

This combination of small-radius actively modulated on-chip nanoelectrodes with a much larger reconfigurable counter electrode at micrometer proximity is a critical enabler for CBCM at MHz – GHz switching frequencies, without being limited by the electrolyte series resistance. To be able to reach a similar high-frequency operation with off-chip modulation, the electrolyte series resistance, loaded by the parasitic capacitive coupling to the entire wetted chip surface (including disabled nanoelectrodes) surrounding the selected nanoeletrodes, would require placing a large external counter electrode plate at few-micrometer distance above the chip surface. Apart from the fact that such a system cannot be manufactured without drastically modifying a mature CMOS flow, the narrow gap between the counter electrode and the chip surface would constitute a huge resistance for the fluid flow. Such a system, if reliably manufactrable at all, would be very impractical.

The capacitance of a nanoelectrode in (row, column) = (i,j) is determined by selecting row i, and measuring the average charge/discharge DC current I_M of column j (see Fig. 2). Therefore, the *measurement capacitance* (C_M) can be expressed as:

$$C_M = \frac{Q_S}{\Delta V} = \frac{I_M}{f_S \Delta V} \quad (1)$$

where f_s is the switching frequency, $\Delta V = V_T - V_D$ is the charge/discharge modulation amplitude, and Q_s is the charge transferred through the sensor cell per charge/discharge cycle.

Typical values of V_D and V_T are in the ranges of 80 – 160 mV and 280 – 360 mV, respectively, with a maximum $V_T - V_D$ of 200 mV. For typical values of C_M in the range 0.6 – 4 fF, the maximum column current I_M at f_s = 70 MHz is 56 nA. Therefore, the input transistor (W/L = 600nm/300nm) of the common-gate amplifier in Fig. 2 is always biased in the sub-threshold regime.

The voltages of the charge-integration nodes (* in Fig. 2) of the 256 column read-out circuits are digitized by 8 ADCs, running in parallel.

The 13-bit ADCs have a cyclic "1.5 bit/cycle" architecture, with built-in noise suppression (by Correlated Double Sampling (CDS), see caption of Fig. 2), similar to the ADC described in section 3B of [29] (same architecture but different component values). They run at clock frequencies of 1 – 45 MHz, that can be derived from the non-overlapping clocks with an on-chip clock recovery circuit and an optional clock divider (divide-by-2; required for non-overlapping clock frequencies of 45 – 90 MHz). For non-overlapping clock frequencies above 90 MHz, the ADC can be clocked with an external clock. In practice, we always use the clock recovery circuit combined with the clock divider, to guarantee a 50% duty cycle for the ADC clock.

Although the ADCs have been designed for 13 bits resolution, their actual resolution is limited to 9 – 10 effective number of bits. The root cause of this limitation is still not fully understood, but it involves a correlated noise or cross-talk component that cannot be averaged out. Although this limits the sensitivity of single-electrode capacitance measurements to 0.5 – 1 aF (1-sigma noise level; see Fig. 16b), it does not block the use of the chip for many interesting single-particle detection and imaging applications (see section IX), or applications where signals of multiple nanoelectrodes can be averaged (e.g. for protein or DNA/RNA detection).

Each ADC processes a group of 32 consecutive odd or even columns in time-division multiplexing mode (MUX not shown in Fig. 2). With the clocks Φ_T and Φ_D of the selected row running continuously, the charge integrators of the 32 columns are started one after another at integer multiples of the number of clock cycles required for 1 A/D conversion (this number depends on the settings of the ADCs). After integration for a programmable number of non-overlapping clock cycles (which determines the integration time), the voltage on the charge-integration node of a column is sampled by the A/D converter, applying CDS, and subsequently reset and restarted, while the other 31 charge integrators continue integrating. Then the next column is processed. This sequence through 32 consecutive columns is repeated 1 – 127 times (programmable), where the ADC ouputs are column-demultiplexed, and accumulated in 256 on-chip data accumulation registers (the 4 blocks labeled "C" in Fig. 1).

After data accumulation is completed for all columns, the contents of the 256 registers are exported via a serial output bus. Then the next row is selected and processed (to avoid cross-talk from the serial output bus, charge integration is postponed during serial output).

On-chip accumulating the ADC outputs of a full row of 256 selected sensor cells can be used for increasing the signal/noise ratio and decreasing the serial-out duty cycle (during which the sensor does not measure).

On a dedicated test board, with clock signals generated by a multi-channel high-frequency pulse generator, connected to the

chip by 50-Ohm terminated rigid coax cables, the chip's CBCM circuitry was verified to work properly up to 320 MHz (using externally clocked ADCs). However, for use in biochemical laboratories, the chip is operated in a self-contained system with on-board pulse generation circuitry that can support a maximum non-overlapping clock frequency of 70 MHz (see section V).

The lower frequency limit is determined by the leakage currents of the non-selected switching transistors. For switching frequencies below 1 MHz, I_M drops to a level that approaches the total leakage current of all non-selected cells of the same column. This results in non-negligible offset errors in the measured capacitance. First-order corrections for leakage currents could not fully remove the errors, suggesting additional effects being involved as well (e.g., the ADCs require a minimum clock frequency to prevent leakage of the charges stored on their capacitors). This issue is subject to ongoing investigation. Pending the results, we limit the lowest frequency to 1 MHz.

The number of switching cycles is typically set to 1408 for most measurements at higher frequencies, but can be reduced if larger values of C_M are expected (e.g. at lower switching frequencies and/or high-salt electrolytes) to keep the voltages on the charge integration nodes within the linear input range of the ADCs. Under nominal operating conditions, the chip produces 4.5 frames/s at 50 MHz switching frequency and 9 on-chip data accumulations per row. With ADC clocks derived on-chip from the switching clock, the frame rate is proportional to the switching frequency. Therefore, at 1.6 MHz it takes about 7 seconds to acquire a complete frame. At a lower number of data accumulations, the frame rate becomes limited by the data transfer time over the serial output bus, with a maximum of about 10 frames/s at 50 MHz. Measurement capacitance images are available in real time. The supply voltage is 1.2 V. With nominal settings, the chip consumes 15 mW at 50 MHz switching frequency (80% by the 8 ADCs).

III. Chip Fabrication and Nanoelectrode Processing

Manufacturing of the wafers consisted of two main parts: an (almost) standard CMOS part, done by TSMC in a mature production fab (Hsinchu, Taiwan), followed by a post-processing part, done in the cleanrooms of IMEC (Leuven, Belgium) and Philips Innovation Services (Eindhoven, Netherlands).

The initial part starts with a TSMC default 90nm LP CMOS flow, processed up to and including the metal-4 Chemical Mechanical Planarization (CMP) step. Next, a 75nm/300nm/150nm (bottom up) nitride/oxide/nitride stack was deposited, which serves as a moisture barrier to protect the underlying CMOS. Via-4 holes (exposed 130nm×130nm), arranged in 256×256 arrays with column/row pitches of 550nm×720nm, 600nm×720nm or 600nm×890nm (on different chip versions), were exposed and etched in the moisture barrier (the etching widens the holes' apexes somewhat). The via-4 holes land on patterned minimum-area metal-4 pads, vertically connected to the common source/drain regions of underlying pairs of switch transistors (the switching nodes in Fig. 2) by minimum-area contact/metal-1/via-1/metal-2/via-2/metal-3/via-3 pillars (see Fig. 4 of [2]). Next, 100µm×100µm bond pad openings were exposed and etched in the moisture barrier, using a TSMC-proprietary method that protects the already formed via-4 holes. Then, a Ta/TaN diffusion barrier was deposited conformally over the patterned moisture barrier, also covering the sidewalls and bottom regions of the via-4 holes and bond pad openings. Finally, the high aspect-ratio via-4 holes and bond pad openings were filled simultaneously with a copper layer that extends 1µm above the surface of the moisture barrier (about 0.5µm in the bond pad regions), as needed to be able to planarize the copper with a copper-CMP step in advanced CMOS copper processes. Here the (almost) standard CMOS processing part ends.

The post-processing part starts with transferring the wafers to the IMEC 300mm cleanroom. Here, the copper layers on the wafers were planarized and thinned with a copper-CMP tool, equipped with an eddy current sensor that monitors the remaining copper thickness during polishing. The CMP was stopped at a target thickness of 120nm, to preserve the underlying Ta/TaN diffusion barrier (see next paragraph).

Next, the wafers were cut into 45mm×45mm squares for further post-processing in the pilot cleanroom of Philips Innovation Services. The actual copper thickness was measured on wafer residues. Gold was sputtered on the thinned copper, and annealed to inter-diffuse with the copper into a uniform gold-copper alloy. The deposited gold thickness was tuned to end at cubic $Au_{0.66}Cu_{0.34}$ and $Au_{0.3}Cu_{0.7}$ phases on the array and bond pad regions, respectively. Cubic phases were chosen to avoid build-up of microscopic stress and defects in the alloy, caused by phase transformations during cooling-down. The gold fractions of the alloys are determined by the average local thickness of the thinned copper layer in the array and bond pad regions. During the anneal, the preserved Ta/TaN double layer acts as a diffusion barrier for copper and gold atoms, to prevent the metals from diffusing into the underlying CMOS layers. In addition, the Ta/TaN is a good adhesion layer for the formed gold-copper alloy, required to prevent delamination from the moisture barrier during subsequent gold-copper polishing (delamination of gold-copper flakes during polishing can rip nanoelectrodes out of the via-4 holes; this was the main defect mechanism in a previous gold-copper manufacturing process that didn't preserve the Ta/TaN double layer).

The gold-copper alloy was patterned with a damascene-like polishing step that stops selectively on the underlying Ta/TaN diffusion barrier. Then the barrier was removed with a conventional barrier-removal polish step, to electrically separate the nanoelectrodes (Fig. 3) and bond pads.

Because, with this approach, all critical geometrical features were defined with state-of-the-art CMOS equipment (193-nm lithography, dry etching) in a production cleanroom with nearly perfect process control, and the gold-copper post-processing flow is essentially like a state-of-the-art copper damascene flow, fully functional sensor chips were made with high yield and low spread. This clearly proves the advantage of staying close to state-of-the-art CMOS processing.

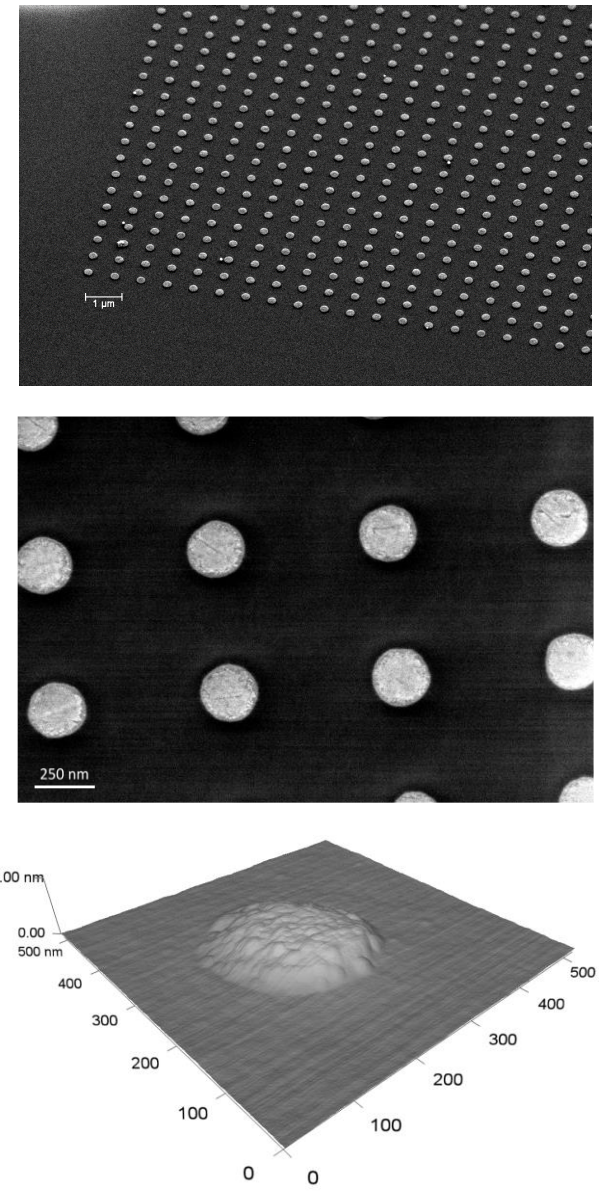

Fig. 3. Tilted overview (top) and perpendicular zoomed-in (middle) SEM images of nanoelectrodes on a 600nm×720nm pitch (white spots in the top picture are polishing slurry particles, left behind because of insufficient post-CMP cleaning). Bottom: contact-mode AFM image of a nanoelectrode protruding 11 nm above the chip surface (the similar-looking hemispherical structures are an AFM tip convolution artifact).

Sensor chips were separated from full-thickness wafers (no backside grinding) by first cutting 100µm wide V-grooves in the saw lanes with a 45° tapered blade, and then cutting though the wafers with a 50µm thick blade. The thick bare dice with 45° beveled front-side edges can be handled conveniently with tweezers, and inserted easily upside-down in a compression spring probe (CSP) socket (section IV).

IV. Socket and Microfluidics

Disposable bare sensor dice are mounted upside down in an ARIES Electronics CSP (Compression Spring Probes) socket (PEEK material) with gold-plated heat-treated BeCu contacts [30][31]. The sockets are modified with 2 drilled fluidic ports (500-µm diameter) and an optional milled microfluidic channel

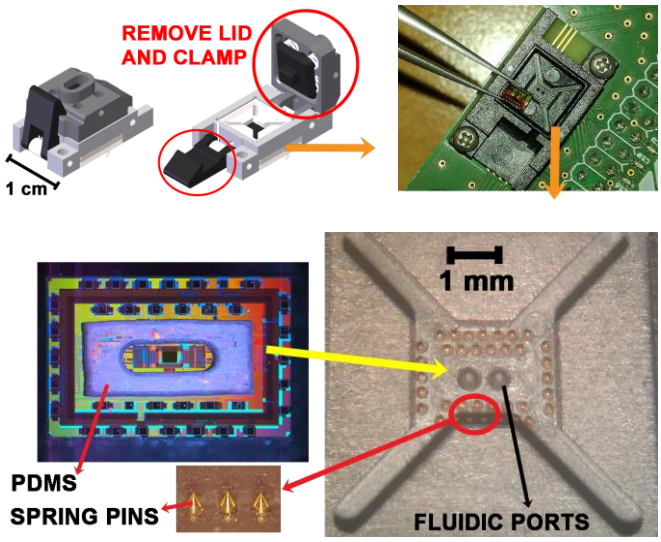

Fig. 4. Drawings and photos of the socket and its mounting. Top left: 3D rendering of the socket assembly [31]. The lid and clamp are removed before connecting the socket to the PCB. Top right: photo of the socket mounted on the PCB, together with a chip held with tweezers. Bottom right: detail of the contact spring pins and fluidic ports in the socket. Bottom left: photo of the chip with a PDMS seal ring (the opening, at the center of the seal, is the fluidic chamber that is filled with electrolyte), and optical microscope photo of the spring pins. The chip is inserted upside-down in the socket.

(150-µm deep and 500-µm wide) in the bottom (part no. A1924-314-23-2 and A3592-314-23_1, respectively). Fig. 4 (bottom-right) shows the version without milled microfluidic channel.

A laser-cut PDMS guard ring defines and seals the microfluidic chamber, and protects the chip's bond pad ring from the liquids. A PDMS sheet (250 µm thick) was cut at 1000 mm/s speed and 13 W power with a commercial CO_2 laser cutter machine. In a socket without milled microfluidic, this seal creates a fluidic chamber with a volume of about 50 nL. In a socket with milled microfluidic channel, a similar volume can be realized with a thinner PDMS ring (typically 100-µm or less). Fig. 4 (bottom-left) shows the PDMS ring placed on the chip.

Closing the lid and clamp of the socket presses the chip on the PDMS ring, with its bond pads against the spring pins. As an alternative mounting approach, a metal finger (Fig. 5 inset) can be pressed on the backside of the chip (instead of the standard lid), thereby creating a good thermal connection to an external temperature control system (section V). Liquids are pumped through the fluidic chamber via PEEK tubes (510-µm outer diameter, 255-µm inner-diameter), press-fitted into the fluidic ports. The biocompatible PEEK material of the socket and the tubes provides high chemical resistance to almost all fluids of interest for biosensing.

V. Board and System Assembly

As shown in Fig. 4 (top right) and Fig. 5, the socket is mounted on a dual-layer PCB, connected with a 40-core flat-cable to a control system, based on an Altera Cyclone III FPGA, partially used to run a NIOS II soft processor. Programmable non-overlapping clock generators are built around an AD9959

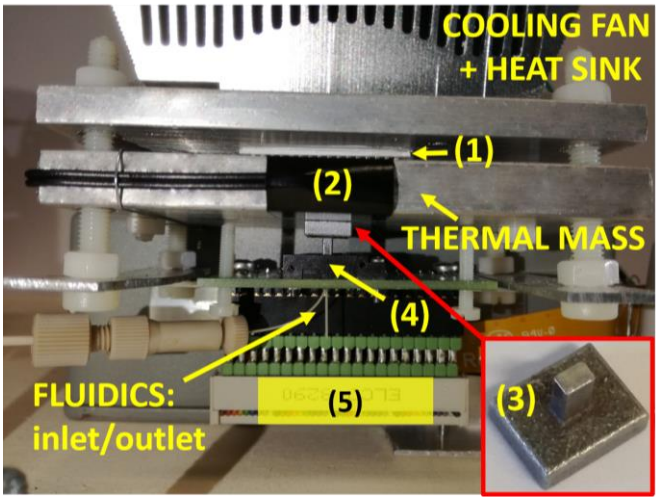

Fig. 5. Chip/controller and indication of the various parts. A Peltier element (1) thermally connects the heat sink to an aluminum thermal mass. An NTC temperature sensor (2) is mounted in a small hole in the thermal mass. Thermal contact to the backside of the chip is created via a 3D printed $Al_{0.94}Si_{0.06}$ alloy heat finger (3, inset). The socket (4) is used without lid and clamp. A 40-pin connector (5) and 40-core flat cable provide the electrical connection to the FPGA-based control system.

direct digital synthesizer (DDS) chip and 2 AD5390 16-channel 14-bit DAC chips, both from Analog Devices. The DAC outputs set clipping and offset voltages, and control current sources of a high-frequency analog circuit that transforms the DDS sinewave outputs into non-overlapping clock pulses with programmable high and low levels, and rise, fall and high times. The details of these circuits are beyond the scope of the current article.

The non-overlapping clocks are exported as differential pairs, and routed through signal-ground-signal wire triples over a 5-cm long 40-core flat cable to the sensor chip outside the control system's enclosure. The clock wires are driven by 118 Ω source impedances, that minimize ringing in the clock signals at the sensor chip terminals. To keep the system compact and simple, all other control signals and voltages are routed through adjacent wires of the same flat cable. Residual ringing in the clock signals, caused by the non-ideal transmission line properties of this construction, limits the maximum useful switching frequency to 70 MHz.

Fig. 5 shows a zoom of the board/socket/temperature control parts. Automatic syringe pumps deliver the liquids to the chip at controlled rates (typically, a few µL/min). The backside of the chip is pressed by a narrow metal finger, in thermal contact to a thermal mass. The finger was 3D printed in $Al_{0.94}Si_{0.06}$ alloy to ensure low surface roughness and high surface parallelism. A temperature control system made of a Peltier cell (model ET-127-10-13), thermal masses, and a heat sink with cooling fan were designed to dynamically regulate the chip temperature over a temperature range from 10 to 75 °C (at 22 °C room temperature). The control algorithm is either a simple on-off sequence or a PID function, where we use an NTC thermistor inserted inside of the thermal mass (label 2 in Fig. 5) to provide a reference temperature for the Peltier controller (LairdTech PR-59).

Fig. 6 (top) shows the chip/thermal mass temperature (T_{chip}, $T_{thermal\ mass}$) and measurement capacitance (C_M) waveforms corresponding to a piecewise-constant change of the temperature setpoint (dashed black curve). Measurements are done in air at 50 MHz switching frequency. Here the temperature is intentionally regulated with a coarse on-off algorithm, generating small rapid temperature ripples around the setpoint, to highlight the strong correlation between the chip temperature and the measured capacitance (mainly via the temperature-sensitivity of the gate-source voltages of the sub-threshold-biased bottom transistors of the cascoded common gate amplifiers in the column read-out circuits; see Fig. 2). Fig. 6 (bottom) demonstrates a strong correlation between T_{chip} and C_M, as expected, with a temperature coefficient of approximately 2.7 aF/degree. With the signals from the 4 on-chip temperature sensors, this coefficient can be used to compensate for temperature variations during measurements.

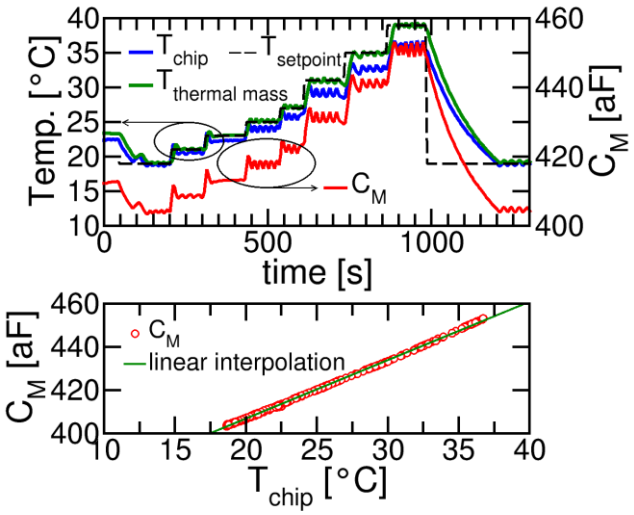

Fig. 6. Top: Measurement capacitance (C_M) in air at 50 MHz while dynamically changing the temperature controller set point ($T_{setpoint}$). On-chip and thermal mass temperature sensor readings (T_{chip}, $T_{thermal\ mass}$) are also shown. Bottom: A strong correlation is observed between C_M and the on-chip measured temperature.

VI. Numerical Modeling and Simulation

The signal transduction mechanisms of the nanoelectrode cells has been explored in detail by means of 3D finite element numerical simulations based on the CVFEM discretization method [32]. The ENBIOS simulator (which is also partly available via the nanohub.org portal [33][34]) solves self-consistently the Poisson-Boltzmann equation in steady state and the coupled Poisson-Drift-Diffusion equations in the time harmonic linearized small signal regime for all ion species in the electrolyte. We simulate arrays of 7×7 to 13×17 nanoelectrodes. The size of the simulation domain is chosen large enough to render effects of the domain boundaries on the results negligible. To mimic the parallel operating principle of the chip, we apply the time-harmonic small signal AC excitation to all nanoelectrodes of the central row of the array and calculate the impedance of the central electrode of that row

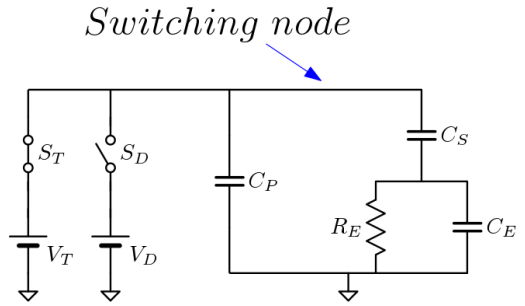

Fig. 7. Equivalent circuit of the switching model. C_P is the parasitic capacitance, C_S is the surface capacitance (the SAM, if present, in series with the double layer), R_E and C_E are the spreading resistance and spreading capacitance of the electrode to the electrolyte. The switches (S_T and S_D) connect the switching node to the charging or discharging voltages (V_T and V_D), as in Fig. 2.

as a function of the AC modulation frequency. Small-signal AC models and numerical simulations produce a complex electrode admittance that can be formally interpreted as a conductance in parallel with a capacitance $Y_A = G_A + j\omega C_A$. In general, G_A and C_A are frequency-dependent real numbers, related to each other via the Kramers-Kronig relations.

Because of the switching operation of the sensor cells, the measurement capacitance C_M (Eq. 1) is not directly comparable to C_A, obtained from small-signal AC models or simulations at $\omega = 2\pi f_s$. Therefore, we developed a switching model, based on a simplified equivalent circuit of a sensor cell with a nanoelectrode in contact with an electrolyte (Fig. 7). The circuit has 4 constant (frequency-independent) components. R_E and C_E are the spreading resistance and spreading capacitance of the nanoelectrode to the electrolyte, C_S is the surface capacitance of a self-assembled monolayer (SAM) on the nanoelectrode surface (if present) in series with the electrical double layer (EDL) capacitance at the electrolyte/electrode interface, and C_P is the parasitic capacitance of the switching node. Combined with the timing parameters of the non-overlapping clocks Φ_T and Φ_D (Fig. 2), the average current $f_s C_{SW}(V_T - V_D)$, pumped through the sensor cell from source V_T to source V_D, can be derived, where the *switching capacitance* is given by [35] (see Appendix A for the derivation of the expression and all its parameters):

$$C_{SW} = (C_S + C_P)(1 - p_b p_a E) \qquad (2)$$

The values of R_E, C_E and C_S can be estimated by fitting the AC admittance $Y = \frac{j\omega C_S(1+j\omega R_E C_E)}{1+j\omega R_E(C_E+C_S)}$ of the right branch of Fig. 7 to the AC admittance Y_A, modeled or simulated with or without analyte on, or near the nanoelectrode surface [36]. The value of C_P can be extracted from experiments (in dry experiments $|Y| \ll \omega C_P$, so the measured capacitance in air is very close to C_P). In the following, we will rely on the switching capacitance model for the theoretical predictions (that is, we extract the AC admittance from ENBIOS simulations, fit the lumped-element model of Fig. 7 to this admittance, and compute C_{SW} according to Eq. 2).

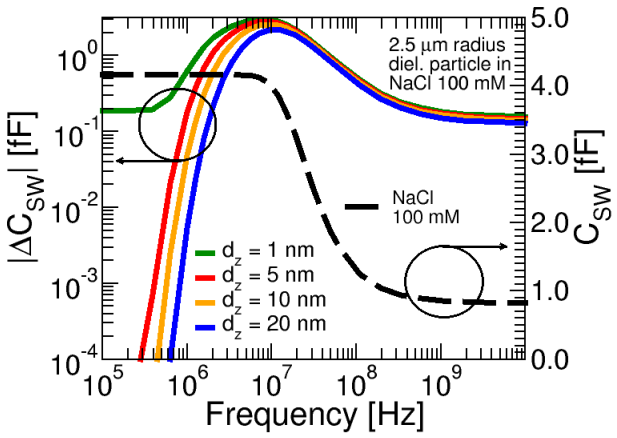

Fig. 8. Theoretical switching capacitance spectrum of a bare nanoelectrode (no SAM) in 100 mM NaCl electrolyte (black), and *switching* capacitance variation spectrum due to inserting a 2.5 µm radius microparticle at a vertical distance of 1, 5, 10, or 20 nm from the surface of the (central) nanoelectrode. The equivalent circuit model parameters in 100 mM without particle are C_S=3.5 fF, C_E=0.173 fF, R_E=2.6 MΩ, C_P=0.65 fF. For each particle location, R_E, C_E and C_S were fitted to numerical AC simulations over a frequency range of 1 kHz to 10 GHz. Detecting analytes beyond the Debye screening length requires high frequencies.

In Fig. 8 (black dashed curve), we show a typical switching capacitance spectrum in electrolyte, where the low frequency part of the response is essentially governed by the surface capacitance C_S, as per the EDL screening theory.

If an analyte (e.g., a microparticle) is present in the electrolyte, the capacitance spectrum is perturbed. We call $\Delta C_{SW} = C_{SW_{w/\ analyte}} - C_{SW_{w/o\ analyte}}$ the *switching capacitance* variation, induced by the presence of the analyte, i.e. the difference between the switching capacitance response with and without analyte. In Fig. 8 (green/red/blue curves) we show the switching capacitance variation spectra due to a 2.5 µm radius dielectric microparticle (ε = 2.6), inserted at vertical distances of 1, 5, 10 and 20 nm above the center of the central nanoelectrode, in a 100 mM NaCl electrolyte. When the particle is located beyond one Debye length from the electrode, the response at low frequency is extremely small. The peak of the curve, around 10 MHz, identifies the frequency of optimum sensitivity.

VII. Calibration and Compensation Strategy

As explained, under intended operating conditions, the 2 transistors of the cascoded common gate amplifier in Fig. 2 are biased in sub-threshold. Therefore, their gate-source voltages (and consequently, V_T) depend logarithmically on the average column current I_M, which, in turn, depends on the switching frequency f_S. Without further measures, this would cause frequency-dependent deviations of the charge/discharge modulation peak-peak amplitude $\Delta V = V_T - V_D$ and the average nanoelectrode DC potential from their setpoints. The latter, in turn, can cause unintended electrochemical disturbances at the nanoelectrode surface, and/or of the nanoelectrode admittance (via the voltage-dependence of the EDL capacitance).

From Eq. 1 it follows that, at constant C_M and ΔV, I_M should depend linearly on f_s: $I_M = C_M f_s \Delta V$. Under these conditions, we can keep V_T constant by correcting V_G:

$$V_G = V_{G,r} + \frac{nk_BT}{q}\ln\left(\frac{I_M}{I_{M,r}}\right) = V_{G,r} + \frac{nk_BT}{q}\ln\left(\frac{f_s}{f_{s,r}}\right) \quad (3)$$

where $V_{G,r}$ and $I_{M,r}$ are values at a reference frequency $f_{s,r}$, k_B is Boltzmann's constant, T is the absolute temperature, q is the elementary charge unit, and n is a non-ideality factor. The latter is calibrated on a frequency sweep with dry nanoelectrodes: n is set to the value that makes C_M, calculated from the measured $I_M(f_s)$ response, frequency-independent. This correction is applied during subsequent frequency sweeps with nanoelectrodes exposed to electrolyte (the same correction is applied to the gate voltage of the upper cascoded common gate transistor). Fig. 9 shows that this "pre-calibration" indeed yields a frequency independent capacitance C_M for dry nanoelectrodes, as expected.

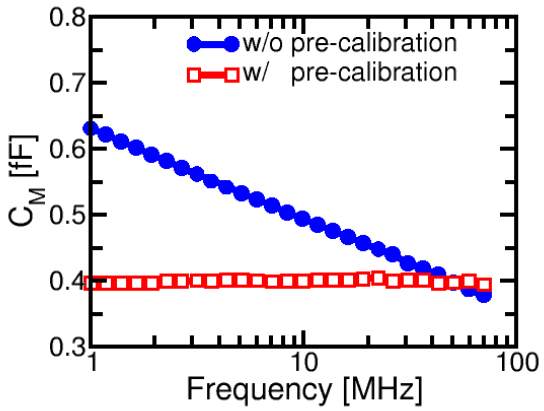

Fig. 9. Uncalibrated and pre-calibrated capacitance spectra for dry nanoelectrodes at 1-70 MHz (the capacitance of dry nanoelectrodes is almost equal to the parasitic capacitance C_P in Fig. 7).

For more complicated cases, where C_M is inherently frequency-dependent, more advanced models can be used to estimate the expected relation $I_M(f_s)$, e.g. based on numerical simulations, or on experimental results from other measurements. However, for brevity, in the current article, we don't go into this detail, and only consider cases described by the logarithmic frequency-dependence in equation 3.

Pre-calibration works fine for constant-capacitance cases. However, dielectric properties of electrolytes in general deviate from purely capacitive behavior. This introduces additional sources of frequency-dependent variations of V_T that are not compensated for. But, because pre-calibration compensates for the most dominant source of variation (frequency sweeps over almost 2 decades), and remaining variations usually are significantly smaller, it still helps keeping the nanoelectrodes biased close to the intended DC setpoint. After the measurement, once I_M is known, we calculate a post-calibration correction for V_T:

$$V_T = V_{T,r} - \frac{nk_BT}{q}\ln\left(\frac{I_M}{I_{M,r}}\frac{f_{s,r}}{f_s}\right) \quad (4)$$

This value is used in Eq. 1 to calculate, off-line via MATLAB scripts, the final C_M, which we refer to as C_{post} in the following. For more complicated pre-calibration estimations of the relation $I_M(f_s)$, equation 4 can be adjusted accordingly.

VIII. Measurements in Uniform Environments and Frequency Spectra

Figure 10 (top) shows a measurement capacitance (C_M) map of the array in air. Striped patterns are visible, which can be attributed partly to lithography effects, which make even and odd rows systematically slightly different from each other,

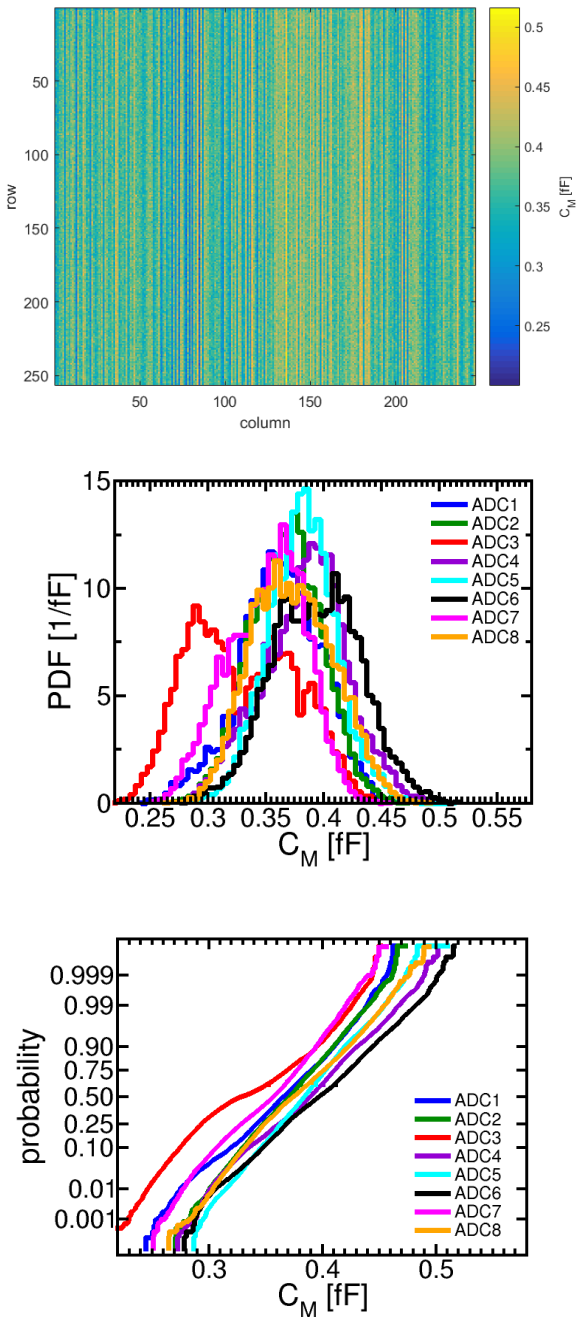

Fig. 10. Measurement capacitance in air at 50 MHz. Top: array map. Middle: histograms of the measurement capacitances, obtained from the 8 ADCs (each one showing a different mean value). Bottom: normal probability plots.

partly to statistical variations and RTN noise in the column readout circuitry, and partly to the fact that odd and even columns are processed by different ADCs, in groups of 32 columns per ADC. In Fig. 10 (middle) the capacitance distribution of the nanoelectrodes, obtained from different ADCs, are shown; Fig. 10 (bottom) shows the corresponding normal probability plots. For each A/D converter, the distribution has a different mean value. These offsets from the full matrix mean value can easily be corrected.

If applied to each column independently, the post-calibration correction of Eq. 4 reduces significantly the column-striped pattern (Fig. 11, top) for both the current-generation chips with novel nanoelectrode processing (this work, left) and the previous-generation chips ([3], right). In the latter case a few regions still can be seen (e.g., in the top left part of the array)

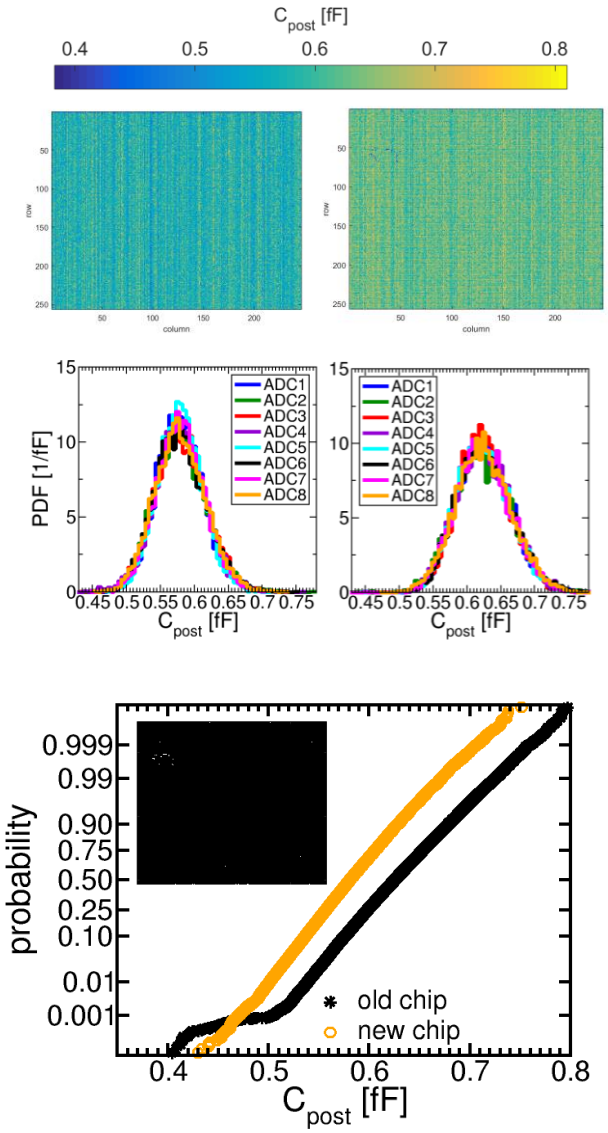

Fig. 11. Top and middle graphs: same as Fig. 10 for the post-calibrated capacitance C_{post}, also corrected for the ADC offsets, both for new (left, this work) and old (right, [3]) nanoelectrode processing. The resulting standard deviation is 0.04 fF and 0.05 fF, respectively; the std/mean ratio is 6.5% for both. Bottom: normal probability plot of all the nanoelectrodes, for old (black) and new (orange) nanoelectrode processing. Inset: 2D binary map that identifies the location of the outliers for the old chip (white spots over black background).

where faulty or dirty electrodes can be identified. The source of the residual column-striped patterns is still under investigation.

Fig. 11 (middle) shows the post-calibrated capacitance distributions for the 8 ADCs after offset compensation. All curves are now on top of each other, as expected. The normal probability plot of the capacitance distribution of all the nanoelectrodes (Fig. 11, bottom) allows for easy identification of outliers, which cause a major deviation of the curve from the expected approximately straight-line trend. The numerous outliers of the old-generation chip (black line in Fig. 11, bottom) are easily located on a binary 2D map (inset), and require to be pruned before further analyses with that chip. They visually match the "bad nanoelectrodes", visible in the top-right color map of Fig. 11. Instead, the improved new nanoelectrode process, described in section III, does not show outliers.

In Fig. 12 we compare the theoretical response, as computed

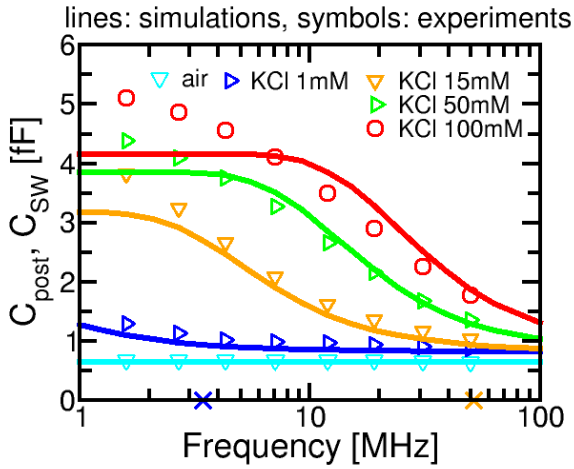

Fig. 12. Comparison of simulations (C_{SW}) and experimental post-calibrated capacitance spectra (C_{post}) in air, and in KCl electrolytes of different salt concentrations. Pre-calibration was applied to the measurements. Crosses on the frequency axis indicate the dielectric relaxation cut-off frequencies of the 1.5 mM and 15 mM electrolytes (3.4 MHz and 51.7 MHz, respectively). The cut-off frequencies of the 50 mM and 100 mM electrolytes (174 MHz and 352 MHz, respectively) are outside the shown frequency range.

with the switching capacitance model of Eq. 2, to experiments in air, and in KCl electrolytes of different salt concentrations. The symbols are array-averages of post-calibrated (C_{post}) capacitances, obtained with pre-calibrated measurements. The main qualitative features are essentially well reproduced, and a good quantitative agreement is obtained up to 50 mM concentrations and frequencies above 2 MHz. Compared to C_M, the C_{post} capacitance trace in air is increased to about 0.6 fF (see also Fig. 11, middle, and Fig. 13), which is close to the value of C_P obtained from parasitic extraction on the physical layout of the sensor cells. In fact, C_P is essentially equal to the sum of the gate-source and gate-drain overlap capacitances of the transistor junctions connected to the switching node (Fig. 2), and the parasitic capacitance of the metals involved in connecting the nanoelectrode.

The frequency sweeps exceed the dielectric relaxation cut-off frequencies $f_E = (2\pi R_E C_E)^{-1}$ of the 1.5 mM and 15 mM

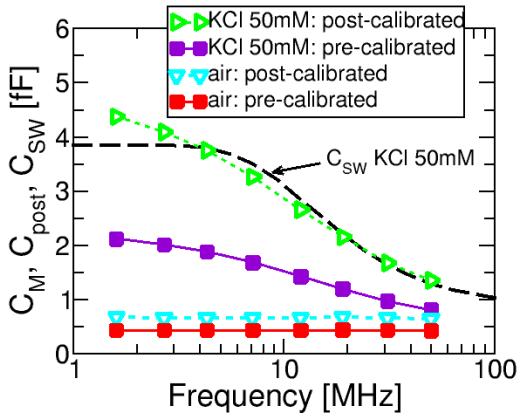

Fig. 13. Comparison between pre-calibrated (C_M) and post-calibrated (C_{post}) capacitance measurements in air and 50 mM electrolyte. The post-calibration increases the baseline value in air to about 0.6 fF. The impact on the spectrum in electrolyte is even more evident. For comparison, the simulated switching capacitance for the 50 mM electrolyte is also included (black dashed curve).

electrolytes (marked on the abscissa in Fig. 12), and approach them for 50 mM and 100mM. Exceeding f_E is important, because only above f_E the nanoelectrode admittance change is constant and insensitive to to the salt concentration and the particle's surface charge, and only depends on the praticle's size and conductivity type (insulating or conducting) [36]. Therefore, the response above f_E serves as a reference level for assessing additional partcile properties like surface charge and overlapping with the EDL, using data recorded below f_E.

Fig. 13 shows a direct comparison between pre-calibrated and post-calibrated capacitance for air, and for a KCl 50mM electrolyte. A large variation of the capacitance is visible in electrolyte, especially at low frequency; this highlights the quantitative importance and impact of the post-calibration.

We speculate that the residual discrepancy between simulations and experiments at low frequencies is mainly caused by surface roughness of the nanoelectrodes. At high frequencies and/or low salt concentrations, the EDL capacitance is less dominant, and the nanoelectrode capacitance is governed, via the much lower spreading capacitance C_E, by its geometrical shape (section VI). However, at low frequencies and/or high salt concentrations, the EDL capacitance becomes dominant (because C_E is short-circuited by the spreading resistance R_E). Then, the EDL capacitance, and therefore also the nanoelectrode capacitance, is governed by the effective electrode area (including nm-scale roughness on a scale larger than the Debye screening length). Because the effective area is larger than the geometrical area, the low-frequency capacitance is higher than expected. This effect, which increases with decreasing frequency, explains the positive offset of C_{post} from C_{SW} in Fig. 12. However, because the chip was designed and optimized for sensing beyond the EDL at high-frequencies, larger discrepancies and spread at low frequencies are less relevant for the intended applications. Identifying the root cause of the discrepancies and larger variations at lower frequencies will be the subject of further investigations.

IX. Imaging and Detection of Particles

All the measurement protocols involving the detection of particles include some preliminary steps to gradually fill the fluidic chamber with the appropriate electrolyte. The first step usually consists in flushing with high-purity isopropyl alcohol (IPA, 99.5%), followed by degassed milliQ water. Thanks to IPA's good wetting properties, compared to directly injecting milliQ, these steps help in filling the whole fluidic chamber with liquid, without stagnant air bubbles. As successive steps, appropriate electrolytes can be flushed to replace the milliQ in the chamber.

During all these steps, avoiding accidentally injecting air bubbles is also of critical importance. In fact, introduction of air bubbles in the fluidic chamber can result in local depressions of the measurement capacitance, thus affecting the measurements. To demonstrate the imaging capabilities of the platform, in Fig. 14 we show 2D capacitance maps of a sequence of air-milliQ transitions (here, intentionally without intermediate IPA flushing), recorded at 50 MHz. The 4 different time frames show the progressive displacement of the air in the fluidic

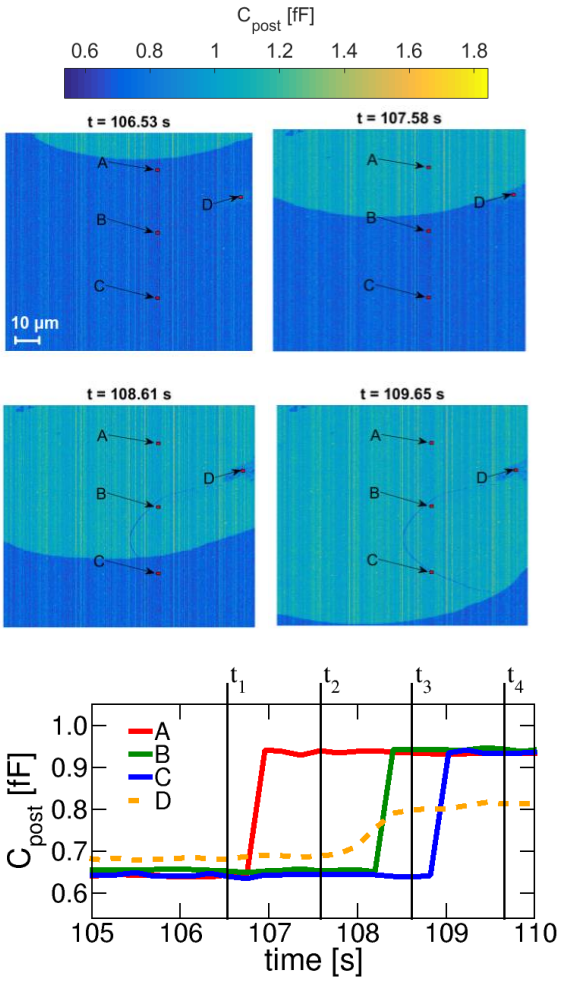

Fig. 14. Imaging sequence of direct air-milliQ transition at 50 MHz at four different time frames, showing the transient response of three nanoelectrodes along a column (A, B, C). The 2D maps are single frames, captured with 512 charge/discharge cycles and 8 on-chip data accumulations. Skipping the intermediate IPA flushing step can result in an imperfect wetting. Contaminated areas (nanoelectrode D) are also evident.

chamber by milliQ. Three nanoelectrodes (A, B, C) are selected along the same column, and in Fig. 14 (bottom) their capacitance time traces are shown, highlighting the steps in their responses upon wetting. Fractions of the surface not suited for analysis (e.g. electrode D, in the stained region near the right edge of the maps, probably due to surface contamination) can be identified a-priori and excluded from the analysis. Indeed,

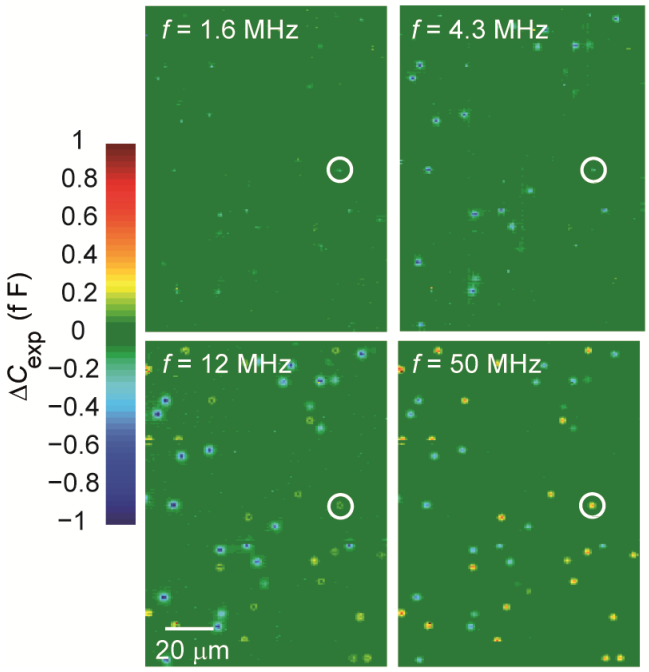

Fig. 15. Pre-calibrated 2D capacitance maps for 200×100 nanoelectrodes resulting from the sedimentation of dielectric and conducting microspheres at different frequencies. The capacitance before microparticle deposition has been subtracted from each pixel (green = no change). Dielectric particles exhibit a decrease in capacitance (cyan/blue) at all frequencies while metallic particles (e.g. in white circle) transition from a decrease to an increase (yellow/red) with increasing frequency. The 2D maps are single frames, captured with 512 charge/discharge cycles and 16 on-chip data accumulations.

the much smaller capacitance increase upon wetting of nanoelectrode D indicates that its surface is not perfectly wetted by water.

During wetting of the array, the measured capacitance change is induced by an increase of the permittivity of the medium in direct contact with the nanoelectrode surface. To demonstrate the ability to also detect changes originating from entities located further from the surface – and in particular beyond the electrical double layer as predicted in Fig. 8 – we performed sedimentation experiments in which microspheres landed on the array while the capacitance was recorded at several frequencies. Fig. 15 shows the outcome of such an experiment in which a mixture of 5 μm radius insulating (latex) and conducting (gold-coated polystyrene) particles were immobilized on the chip surface. The surrounding solution consists of phosphate buffered saline with an ionic strength of 0.1 M, corresponding to a Debye length of approximately 1 nm. The resulting 2D capacitance maps for four different frequencies ranging from 1.6 MHz to 50 MHz are shown in the figure.

By virtue of their radius being larger than the pitch of the array, the footprint of each microparticle spans a number of nanocapacitors, yet it can only be in near contact with a single one. Indeed, at the lowest measured frequency of 1.6 MHz, essentially only single nanocapacitors exhibit a significant response to microparticle sedimentation, corresponding to particles located in close vicinity to that electrode. As the frequency increases the signals become gradually stronger, however, and the spatial extent over which the particle is detected grows in size, such that above 10 MHz the particles exhibit a footprint on the array which can be related via simulations to the real size of the particles themselves.

A striking feature of the data of Fig. 15 is the qualitative difference in response between the two types of particles. While dielectric microspheres cause a decrease of the capacitance, conducting particles cause an increase at high frequencies. This behavior can be understood by noting that, whereas dielectric particles block access of the ionic and displacement currents to the electrode, conducting particles instead provide a capacitor-like high-frequency short-circuit through the surrounding dissipative medium [37]. This picture is further corroborated by the observation that, as predicted by the compact model in [36], at lower frequencies, conducting particles also behave as high-impedance pathways and yield a suppression of the charging response, much like the dielectric particles. This behavior (see highlighted particle in Fig. 15) was verified and confirmed by numerical simulations, whose detailed description is well beyond the scope of this paper.

The high-frequency impedance response of nanocapacitors is largest to objects located in the region of greatest electric field strength [36], namely, the hemispherical volume located directly above the electrode. To exploit this capability, we performed detection experiments using nanometer-scale spherical particles. In this case the analyte is much smaller than

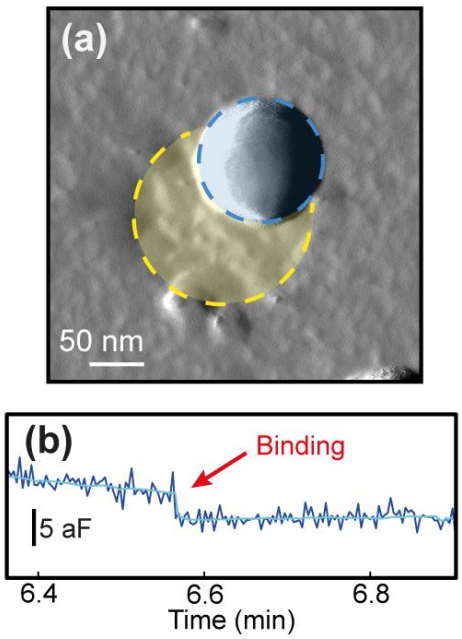

Fig. 16. (a) Tapping-mode AFM amplitude image of a nanocapacitor (yellow) with a single dielectric 40 nm diameter particle attached (blue). The particle diameter appears larger due to tip convolution. (b) Capacitive response of the same electrode exhibiting a single step attributed to binding of the nanoparticle. The measurement frequency is 50 MHz.

TABLE I
COMPARISONS WITH PRIOR ART

Ref.	CMOS Tech.	Sensor Site	# sens.	Sensors /mm^2	Meas. quantity	Meas. principle[e]	Freq. range	P_{diss} [mW]	Imaging
[20]	180 nm	MEA (Au) 22×22 µm	9,216	1,111	|Impedance|	EIS	100 Hz-1 MHz	N/A	
[23]	350 nm	MEA (Au) 40×40 µm	100	204	Admittance	I/Q	10 Hz-50 MHz	84.8	
[39]	130 nm	MEA (Au) 28×28 µm + PDA	5,120[a]	297	|Impedance|, ExC pot., OD	I/Q	100 kHz-2 MHz	N/A	Yes (optical)
[40]	130 nm	4-WE (+ CE, RE) (Au) 2×2 µm[b]	64[c]	17	Admittance	I/Q	0.1 Hz-10 kHz	1.8	
[41]	130 nm	MEA	16,384	4,4	Impedance, ExC pot., InC pot.	SW mod/dem	1 Hz-10 MHz[d]	95	Yes
[27]	250 nm	IMEA (Al/Al_2O_3) 100×100 µm	5	500	capacitance	C2f	8 kHz-291 MHz	29	
[5]	180 nm	MEA (Pt) 7.5×3 µm	59,760	5,487	Impedance	Lock-in	1 Hz-1 MHz	86	Yes
This work	90 nm	NEA (AuCu) radius=90 nm	65,536	2,525,253	Switched capacitance	CBCM	1 MHz-70 MHz	15	Yes

a. grouped in 1 electrode + 4 photodiodes per sensing site; b. one WE sized 55×55 µm, one WE sized 5×5 µm, two WE sized 2×2 µm; c. 16-channels, each one with 4-WE; d. range for HFIS, e. for impedance analysis
C2f: capacitance-to-frequency, CBCM: Charge-based capacitance measurement, CE: counter electrode, ExC pot.: extra-cellular potentials, f_{max}: maximum frequency, IMEA: interdigitated MEA, InC pot.: intra-cellular potentials, MEA: micro-electrode array, NEA: nano-electrode array, OD: optical detection, PDA: photodiodes array, P_{diss}: dissipated power, RE: reference electrode, SW mod/dem: square-wave modulation/demodulation, WE: working electrode

the pitch of the array, and a response to a nanoparticle is only expected at a single electrode, even at high frequencies. Immobilization of the analyte to the surface of the array is absolutely necessary since the diffusion time of a nanoparticle past the electrode is much shorter than the inverse of the image capture rate of 4.5 frames/second. We employed bovine serum albumin (BSA) to immobilize polystyrene nanoparticles on the array; Fig. 16a shows an AFM image of such a 40 nm diameter particle overlapping a nanocapacitor. The corresponding capacitance signal for the same electrode is shown in Fig. 16b, exhibiting a single step with a capacitance change <5 aF upon binding. The cyan curve is obtained applying the filtering method defined in [38] to the capacitance waveform. Detection of such a small capacitance with as good a time-resolution would be essentially impossible with a macro- or microelectrode.

The time trace in Fig. 16 also shows the noise level of a single electrode: about 0.5 – 1 aF (1 standard deviation).

X. DISCUSSION AND CONCLUSIONS

To benchmark our work with existing literature, Table I compares key features and performance indicators of our chip with published planar micro and nanoelectrode arrays. Our chip has the largest number and surface density of working electrodes. The small size and density of sensors is a fundamental prerequisite for enabling detection and HFIS of small nanoscale analytes, as those shown, for instance, in Fig. 16. On top of that, the chip exhibits high maximum frequency of operation and small consumed power at that frequency. Chips as in [27] were reported to operate at even higher frequencies, but with much smaller spatial resolution and larger dissipated power. The Table demonstrates the opportunities offered by state-of-the-art CMOS process technology.

The chip is placed in a custom socket and microfluidics setup, connected to a temperature control system capable to operate over broad temperature ranges. This enables to inspect physico-chemical phenomena and analytes which are of interest at specific operating temperatures, like for instance imaging of tumor cells (at human body temperature) or DNA hybridization/melting processes (from 50 °C and above). Capacitance spectra up to 70 MHz allow to identify the relevant cut-off frequencies and demonstrate the ability of the chip to overcome Debye screening limits over a broad range of electrolyte salt concentrations, nearly approaching physiological limits. *A-priori* and *a-posteriori* compensation of systematic errors (pre- and post-calibration) allows to achieve a good quantitative agreement between experimental and simulated capacitance spectra, especially in the intended high frequency domain. While not being identical to a true amplitude/phase impedance measurement, the proposed frequency-swept CBCM measurements enable much higher nanoelectrode surface density and lower power consumption at high modulation frequency. This concept thus represents a valid alternative, especially for the envisioned (bio)sensing applications, where the measured impedance can be modelled as the combination of resistive and capacitive lumped elements.

On top of HFIS applications, the imaging capabilities have also been illustrated. The platform allows to identify upfront regions of the array with contamination and excluding them from analyses. The imaging capability make it a useful alternative to expensive optical systems, that require optical components and CMOS image sensors. The real-time detection enables, for instance, to estimate deposition times of analytes. The combination of frequency sweeps and imaging enables spectroscopic investigations of living cells and cell walls, e.g. in cell-based high-throughput drug screening, etc.

In general, the chip allows massive parallel capacitive imaging systems with tens to hundreds (maybe even thousands) of chips running in parallel. Fields like high-throughput drug discovery could benefit big time from this.

The system is enabled by advanced CMOS technology processes, and the approach is actually quite general. In fact, it is applicable also to different (non-*bio*) applications (e.g., gas or airborne particles sensing).

APPENDIX A

Here, we briefly describe the steps that lead to Eq. 2. The equivalent circuit of the switching model (Fig. 7) is cycled repetitively through 4 successive phases. During phase 1, of duration t_1, with $(S_T, S_D) = (OFF, ON)$, the switching node is discharged to V_D. During phase 2, of duration t_2, with $(S_T, S_D) = (OFF, OFF)$, charge redistribution takes place. During phase 3, of duration t_3, with $(S_T, S_D) = (ON, OFF)$, the switching node is charged to V_T. During phase 4, of duration t_4, with $(S_T, S_D) = (OFF, OFF)$, charge redistribution takes place again. Because of the stationary repetitive cycling with switching frequency $f_s = \frac{1}{t_1+t_2+t_3+t_4}$, the initial state of phase 1 is equal to the final state of phase 4.

The switching events cause transient currents through C_S, characterized by 2 ratios $p_a = \frac{C_S}{C_S+C_E}$ and $p_b = \frac{C_S}{C_S+C_P}$, 2 time constants $\tau_a = R_E(C_S + C_E)$ and $\tau_b = R_E\left(\frac{C_S C_P}{C_S+C_P} + C_E\right)$, and 4 decay factors $e_{1/3} = \exp\left(-\frac{t_{1/3}}{\tau_a}\right)$, $e_{2/4} = \exp\left(-\frac{t_{2/4}}{\tau_b}\right)$.

During each cycle, a charge $Q_s = \Delta V(C_S + C_P)(1 - p_b p_a E)$ is transferred from the charge source V_T to the discharge source V_D, where

$$E = \frac{e_1\big(1 - e_3(e_4 - (1 - e_4)p_a p_b)\big)}{D} + \frac{e_3\big(1 - e_1(e_2 - (1 - e_2)p_a p_b)\big)}{D}$$

$$D = 1 - e_1(e_2 - (1 - e_2)p_a p_b)e_3(e_4 - (1 - e_4)p_a p_b)$$

The switching capacitance is defined as $C_{SW} = \frac{Q_s}{\Delta V}$. Substitution of Q_s leads to Eq. 2.

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