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Temperature Impact on the Reset Operation in HfO_2 RRAM

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***Abstract*—In this letter we report about the impact of temperature on the reset operation in HfO_2 RRAM devices. Standard I-V DC characterization (voltage sweeps) is exploited to separately assess the different temperature impact on Reset and High Resistance State (HRS) Verify stages in real operating conditions. The temperature dependence of the processes involved in the two stages is obtained by extracting the effective activation energy of the charge transport in HRS Verify, and exploiting a compact model for the Reset stage. The compact model links I-V DC measurements to the physical properties of the dielectric barrier defining the HRS in the RRAM. A linear relation is found between barrier thickness and Reset temperature. Results suggest that Reset may be optimized w.r.t. the operating temperature to improve cycling variability, especially at ultra-low reset voltages.**

***Index Terms*—RRAM; I-V; Temperature; Reset; Variability; Resistive Switching.**

I. Introduction

RESISTIVE Random Access Memory (RRAM) based on HfO_2 allows fast low-power operations, and high-density [1-2], becoming a promising alternative non-volatile memory. Unfortunately, stochastic features inborn in this technology, e.g. randomness in the switching mechanism and variability [3-8], are hampering the device scaling and multi-bit storage implementation. This is delaying the full scale industrial exploitation of the RRAM concept which requires further investigations. To this purpose, a full characterization in real operating conditions would require pulsed experiments to investigate the actual device behavior and to improve its performance and reliability. On the other hand, pulsed characterization can be challenging, making the standard DC characterization a more attractive option due to its feasibility, if its limitations are correctly considered. In this study, we exploit a simple DC characterization to investigate the impact of temperature by estimating the physical properties of the device at the end of the Reset stage and at HRS Verify. Experimental data are evaluated using a compact model [9] linking the device physical properties to its electrical features. A different temperature dependence of the Reset and HRS Verify stages is detected and described in a compact fashion. This analysis provides insights into the physics of the reset operation and can be used for its optimization.

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II. Device and Experiments

Measurements are performed on scaled 200x200nm^2 TiN/Ti/HfO_2/TiN cross-bar RRAMs in 1T1R configuration. The access transistor is used to prevent current overshoot during forming and set operations, which could degrade the switching characteristics [10]. The transistor gate is biased to limit the maximum current (i.e. to enforce a current compliance, I_C) through the cell. Devices with 3.4 nm ALD HfO_2 and a 5 nm Ti layer are analyzed. The forming operation is performed with I_C=100μA by applying a slow voltage ramp (10mV/s). In these conditions, the transition to the Low Resistive State (LRS) during the forming operation happens at a typical forming voltage of ~2.5V (not shown). After forming, we performed 50 switching DC cycles by means of bipolar voltage sweeps on every device in different operating conditions. The switching is described in the literature as the formation and subsequent partial oxidation of a conductive filament (CF) during set and reset operations [5-6], driving the device in LRS and HRS, respectively. I-V curves are measured at each cycle to determine HRS and LRS resistances at read voltage, V_{READ}=50mV, except when differently reported.

III. Results and Discussion

Figure 1a) shows the I-V curve of an RRAM device during the application of a DC voltage sweep from 0V to -V_{RESET} and back to 0V, which is used to drive the device from LRS to HRS and to detect the I-V characteristic of HRS. For clarity, this operation is divided in two parts, identified by the blue circles in Fig. 1a). Part 1 (namely, *Reset stage*) corresponds to the DC voltage sweep from 0V to -V_{RESET}, while part 2 (namely, *HRS Verify stage*) corresponds to the voltage sweep from -V_{RESET} to 0V. Since the two parts are associated with different physical mechanisms we may expect they have different temperature dependence. Indeed, the *Reset stage* is driven by the applied electric field leading to the creation of a dielectric barrier [4-9] which determines the HRS. The mechanism has been described as the diffusion of oxygen ions around the CF towards the bottom end and their recombination with the oxygen vacancies in the CF itself. In this work we neglect the impact of the CF local temperature since its influence on the diffusion of the O ions, which are in the surroundings of the CF and not within the CF, is negligible [11]. Experimental evidences and simulations [5-6] suggest that the barrier is formed during the *Reset stage* (part 1), and

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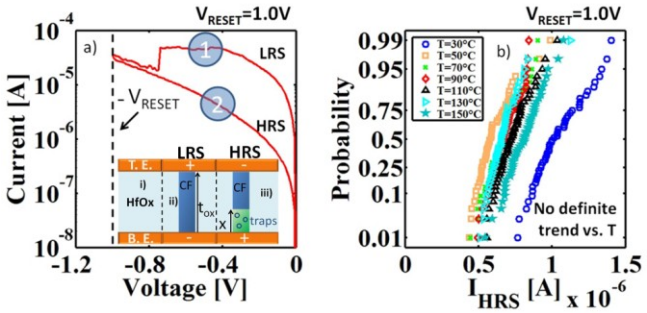

Figure 1. (a) I-V curve of the reset operation at V_{RESET}=1.0V. The reset I-V curve is schematically divided in part 1 and 2, identified by the two blue circles. In the inset, the schematic of an RRAM in different states: (i) The cell in pristine state. The top and bottom electrodes are highlighted. (ii) A conductive filament (blue cylinder) is formed, driving the device in LRS. The polarity of the applied voltage during the set operation is reported. (iii) Reset process: partial oxidation of the conductive filament creating a dielectric barrier (green section of the cylinder), with thickness *x*. The polarity of the applied voltage during the reset operation is indicated. (b) Statistical I_{HRS} distribution over 50 cycles at V_{READ}=50mV after reset operations at different temperatures. The temperature of the two stages (parts 1 and 2) is the same.

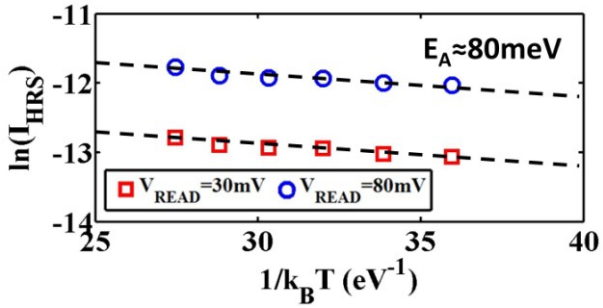

Figure 2. Arrhenius plot of the HRS current in reading conditions at two different V_{READ} (symbols). The effective activation energy E_A≈80meV is extracted. All the symbols collected at the same reading voltage are related to the same bit, which is read at different temperatures. The goodness of fitting is >95% in both cases.

that is kept unaltered during the *HRS verify stage* (part 2), since the absolute value of the applied voltage decreases after having reached its maximum, V_{RESET}, at the end of part 1. Hence, the characteristics of the HRS resulting from the reset operation are mostly determined during part 1. The shape of the *HRS Verify stage* I-V curve is characteristic of the trap-assisted tunneling (TAT) charge transport through the dielectric barrier resulting from the previous *Reset stage* [12].

We performed 50 switching cycles at room temperature (RT) and repeated the whole experiment at different temperatures. The probability distributions of the experimental read current in HRS at V_{READ}=50mV after every switching cycle at different temperatures are shown in Fig. 1b). It is important to notice that: (i) the temperature of the two stages of the reset operation is the same; (ii) the confidence in the results obtained by this simple DC set-up is very high. Fig. 1b) shows no clear trend of the reading current with temperature, hiding the actual temperature dependence of both part 1 and part 2.

To clear this point, we exploit the model in [9] which provides an estimation of the barrier thickness associated with the HRS resistance measured at low voltages, typically $|V_{READ}|$<300mV [9], and extracted from the RT *HRS Verify stage* I-V curve. This allows linking the structural properties of the dielectric barrier to the electrical characteristics of the device at low voltages (i.e. V_{READ}) and RT, see the inset in Fig. 1a). To exploit the same model at different temperatures and obtain the correct estimation of the barrier thickness, we need to disassociate the temperature dependences of the two stages. This could be achieved by performing the *Reset stage* at different temperatures and the *HRS Verify stage* always at RT: this results in a dramatically time-consuming experiment due to the continuous heating and cooling of the wafer. Conversely, we characterize the temperature dependence of the *HRS Verify stage* only, and then include the results in the compact model. Hence, we considered a device driven in HRS at RT and performed reading operations at different reading voltages and temperatures. This was repeated for different reset conditions and on devices formed with different current compliances. In all cases, the temperature dependence of the current is exponential, so we can represent the complex temperature dependence of the TAT charge transport [12] through the effective activation energy, by considering the Arrhenius law, Fig. 2. The extracted effective activation energy is nearly E_A≈80meV, in agreement with the values reported in the literature [4-5].

Having identified the temperature dependence of the read current, we can now use the compact model to estimate the

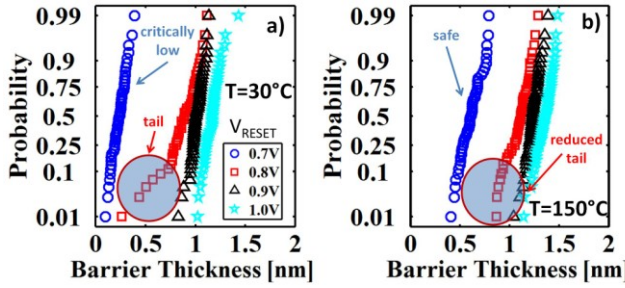

Figure 3. (a) Probability distribution of the barrier thickness over cycling at 30°C for a device in different reset conditions. Cycling variability issues arise at ultra-low reset voltage. (b) Probability distribution of the barrier thickness over cycling at 150°C for a device in different reset conditions. Cycling variability and reset fail issues in (a) are now less critical. Same legend as in (a) applies.

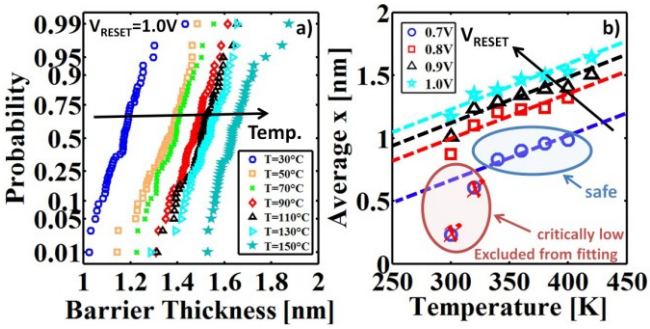

Figure 4. (a) Probability distribution of the barrier thickness over cycling at different temperatures (from 30°C to 150°C) for a device reset at V_{RESET}=1.0V. A monotonic increasing trend of the barrier thickness with the reset temperature is found. (b) The average values of the distribution in (a) are reported as a function of temperature for different reset conditions. Linear fittings are reported for every reset voltage. The points marked with a red cross and reported as "critically low" have been excluded from the fitting since they correspond to unreliable reset conditions (low temperature and ultra-low reset voltage).

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correct barrier thickness from data at different temperatures following this algorithm: (i) measure read current at given temperatures; (ii) estimate read current at RT using E_A; (iii) feed the compact model with the read current at RT to extrapolate the actual barrier thickness at given temperatures. This allows characterizing the effect of temperature on the *Reset stage* (i.e. how the reset temperature affects the barrier thickness).

Fig. 3a) shows the probability plots of the barrier thickness over cycling at RT for a device in different HRS conditions (V_{RESET}=0.7V to 1.0V). The normal distribution of the barrier thickness arises from the intrinsic randomness of the switching mechanism, determining cycling variability [3-4]. The distribution shifts towards higher values for higher V_{RESET}, in agreement with the trends reported in the literature [5-9]. However, the condition V_{RESET}=0.7V results in a critically thin barrier, determining poor performances. Actually, these reset conditions are insufficient to reliably switch the device. Reset at V_{RESET}=0.8V becomes more reliable, even though a tail appears in the distribution. This is due to the intrinsic randomness in the reset operation: these reset conditions are barely sufficient to obtain a reliable switching, which is not always attained. Satisfactory performances are reached using higher V_{RESET}.

Results at higher temperature are shown in Fig. 3b). The reset operation at given V_{RESET} is found to be associated with a thicker barrier at higher reset temperatures, enhancing the reliability of the reset condition V_{RESET}=0.7V w.r.t. RT, which now results in the formation of a thicker barrier. Furthermore, a better control of the cycling variability is attained; see tail reductions in Fig. 3b). Again, this is due to the fact that a higher temperature implies a thicker barrier, hence a more reliable switching.

The statistical characterization of the temperature impact on the *Reset stage* is summarized in Fig. 4a), where we report the barrier thickness distributions over cycling at different reset temperatures for the reset condition V_{RESET}=1.0V. The trends of the average values of the distributions are reported in Fig. 4b), showing a linear trend between the barrier thickness and the reset temperature in every reset condition. This finding is consistent with the enhanced oxygen ions diffusivity at higher temperature, leading to a more efficient recombination with oxygen vacancies, producing thicker barriers at the same reset voltage [5-6].

The overall picture suggests that V_{RESET} might be controlled according to the temperature used in the qualification procedure of an RRAM device. In fact, for high temperatures, we can reduce V_{RESET} and thus target low-power operation at the same variability. Moreover, the read margin constraints due to variability can be relaxed due to the positive influence of typical operating temperature, which is higher than RT.

IV. Conclusions

We investigated the effect of temperature on the *Reset stage* in HfO_2 RRAM devices. The extraction of the *HRS Verify stage* activation energy, E_A≈80meV, together with the exploitation of a compact model, allows estimating the physical properties characterizing the HRS (i.e. barrier thickness). A statistical analysis over cycling in different reset conditions confirms that a higher temperature leads to the re-oxidation of a larger portion of the CF. The relation between the reset temperature and the barrier thickness is linear in all the experimental range. These results can be exploited to optimize the *Reset stage* w.r.t. cycling variability and power consumption.

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