IET Renewable Power Generation

Review Article

IET Journals
The Institution of Engineering and Technology

Recent advances in single-phase transformerless photovoltaic inverters

ISSN 1752-1416
Received on 11th March 2015
Revised on 17th July 2015
Accepted on 24th August 2015
doi: 10.1049/iet-rpg.2015.0101
www.ietdl.org

Davide Barater[1] ✉, Emilio Lorenzani[2], Carlo Concari[1], Giovanni Franceschini[1], Giampaolo Buticchi[3]

[1]*Department of Information Engineering, University of Parma, Parma, Italy*
[2]*Department of Science and Methods for Engineering, University of Modena and Reggio Emilia, Reggio Emilia, Italy*
[3]*Chair of Power Electronics, University of Kiel, Kiel, Germany*
✉ *E-mail: davide.barater@unipr.it*

Abstract: Photovoltaic (PV) power systems have been in the spotlight of scientific research for years. However, this technology is still undergoing developments, and several new architectures are proposed each year. This study describes the main challenges facing grid-connected PV systems without galvanic isolation, then carries out a review of the state-of-the-art of single-phase systems. The converter topology review is focused on the match between the different types of converters and the different PV panel technologies, determined by the common-mode voltage between the PV string terminals and the ground. The ground leakage current, due to time variations of this voltage, is a source of electric safety and electromagnetic interference (EMI)-related problems, and its amplitude is constrained by international standards. The basic principles of operation of the different solutions are described, along with their strengths and drawbacks. Conversion efficiency is evaluated qualitatively comparing the semiconductor power losses. Finally, the future trends regarding semiconductor devices, PV panels and international regulations for single-phase grid-connected equipment are discussed, and indications on how these might steer future research efforts in PV converters are inferred.

1 Introduction

Recent years have witnessed a steady increase of energy production from renewable resources. In particular, the greatest increment has been registered for household-size grid-connected photovoltaic (PV) energy production, due to the possibility to install low power plants easily integrated into the urban environment, the so-called domestic PV.

Following this trend, in recent years there has been a remarkable proliferation of academic and industrial research on new solutions for single-phase grid-connected inverters, designed to maximise efficiency and reliability; many innovations have already started trickling down to the market.

Initially, grid-connected inverters were designed around a line frequency transformer, which facilitated the design by establishing a galvanic isolation between the PV source and the grid. Nevertheless, a line transformer is a bulky component, and the source of additional cost and power losses. The typical efficiency of this kind of systems is below 97%. An intermediate solution is represented by inverters that use a high-frequency transformer, which, keeping the advantages of galvanic isolation, mitigates the problem of the reduced power density, due to the reduced size of the magnetic core. Anyway, the use of high-frequency transformers inevitably increases the number of power stages, since the DC power from the panels has to be modulated at high frequency and, then, converted to line frequency, increasing the total complexity of the inverter. The number of power stages, and the size constraints of the high-frequency transformer (that inevitably limit the wire sections, consequently increasing the resistance) have a great impact on the maximum efficiency that these topologies can achieve.

For all the reasons above, transformers have been almost universally phased out of domestic size PV plants. Nowadays, transformerless inverters are the most efficient grid-connected converters on the market, with some companies claiming efficiencies higher than 98% for their products.

Nevertheless, the use of transformerless inverters in grid-connected systems is not straightforward. New problems arise due the absence of galvanic isolation, such as ground leakage currents and the possibility to inject DC current into the grid.

During the last years, several classifications for transformerless single-phase inverters were proposed.

In [1], Meneses *et al.* identified three categories of step-up transformerless topologies: two-stage topologies, pseudo-DC link topologies, and single-stage topologies, shown, respectively in Figs. 1*a–c*.

The former are those that employ a DC/DC stage for boosting the voltage from the PV source while performing a maximum power point tracking (MPPT) algorithm, and a DC/AC stage to inject current into the grid. Between the two stages a DC-link capacitor bank ensures power decoupling between the DC source and the AC load. The DC link capacitor bank must usually be very large in order to reduce the amplitude of the voltage ripple at twice the grid frequency; thus, electrolytic capacitors are usually employed, affecting the life span of the entire system.

The pseudo-DC-link topologies consist of two power stages as well, but in this case the DC/DC converter generates a rectified sinusoidal current. This current is then unfolded in phase with the grid voltage by means of a line-switched bridge.

The last category includes converters where the functionalities of stepping-up the voltage from the PV source, executing the MPPT algorithm, and controlling the quality of the injected grid current are performed by a single power stage. These solutions aim at simplifying the converter structure and increasing the power density, but often they fail at improving the efficiency as well, due to increased semiconductor stress.

In [2], Kjaer *et al.* classified the converters for PV applications into transformer and transformerless. Furthermore, a more accurate subdivision was developed on the base of the number of power stages, the position of the power decoupling capacitor, and the grid interface stage.

All the above categorisations were developed focusing on an inverter-centric point of view.

In recent years, many new types of PV panels were developed and marketed, with different basic technologies. Each one of them presents peculiar characteristics and requires specific precautions for the connection. From a practical point of view, the choice of the appropriate inverter for a PV plant is made by the designers

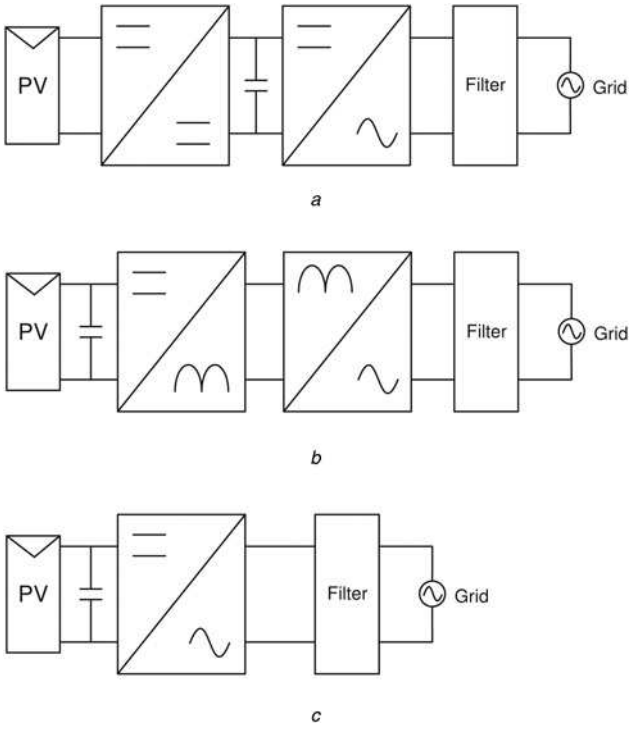

Fig. 1 *Classification of step-up transformerless topologies [1]*

a Two-stage
b Pseudo DC-Link
c Single-stage

depending on the PV technology installed. For these reasons, an alternative classification for grid-connected transformerless PV inverters is adopted, already used by some inverters manufacturers, in this work, correlating the characteristics of the converters with the needs of the different PV technologies.

Since PV panels and converters are so tightly tied, an overview of the major types of PV panels is carried on in the next section. Sections 3–6 represent the core of the paper with a review of the state-of-the-art of the different types of PV converters, while Section 7 compares their power losses. Finally, Section 8 outlines the future trends, and Section 9 reports the concluding remarks.

2 PV panel technologies and their peculiarities

This section reports a brief overview of the existing PV panel technologies. The motivation is that the PV panel technology can affect the design of the power converter. In particular, it will be explained in the following that some panels have particular grounding requirements that only some topologies can fulfil.

Monocrystalline and polycrystalline panels have been dominating the PV market for years. Nevertheless, new technologies, such as thin film modules, amorphous panels, and tandem (two-junction) solar cells, offer high performances and, in some cases, reduced production costs. However, some of these technologies may be employed only in restricted circumstances where proper precautions are taken. The major issues for PV panel technologies are

- ground leakage current;
- potential induced degradation (PID);
- transparent conductive oxide (TCO) corrosion.

2.1 Ground leakage current

Monocrystalline and polycrystalline panels present a stray capacitance between the PV cells and the metal support frame of the modules, which is usually grounded for safety reasons. Since the neutral cable of the grid is connected to ground in correspondence of the medium voltage (MV) to low voltage (LV) mains transformer, the output of the grid-connected converter results grounded as well. In this scenario, it is possible for a leakage current to circulate in the path that connects the PV cells to the ground through the panel parasitic capacitance C_p (Fig. 2*b*). The value of the capacitance depends, among other factors, on the geometrical structure of the PV plant and on the weather conditions.

A PV plant can thus be seen as an array of stray capacitances, connected in series or in parallel according to the structure of the PV field. Nevertheless, the phenomenon can be effectively described adding two concentrated capacitors to the schematic of a grid-connected inverter, between the ground reference and both the positive and negative terminals of the PV source, as shown in Fig. 2*b*. The value of the stray capacitor can typically vary from 10 to 100 nF for each kW installed for mono- and polycrystalline panels, while for thin film panels it can be an order of magnitude higher [3].

If no precautions are taken, the leakage current can be very high. Ground leakage currents are particularly detrimental not only because they can damage the PV panels, but also because, being in the same path as a possible fault current, they make it difficult to detect the presence of ground faults.

To limit the ground leakage current, the voltage across the parasitic capacitance C_p must be limited in both frequency and amplitude. Describing the circuit of Fig. 2*b* in terms of differential- and common-mode (CM) components, as shown in Fig. 2*a*, the voltage v_n can be expressed as

$$v_n = -v_{cm} - \frac{v_d(L_{f_2} - L_{f_1})}{2(L_{f_2} + L_{f_1})} + v_{grid_{cm}} - \frac{V_{DC}}{2} \quad (1)$$

where v_d and v_{cm} are the differential-mode and CM components of

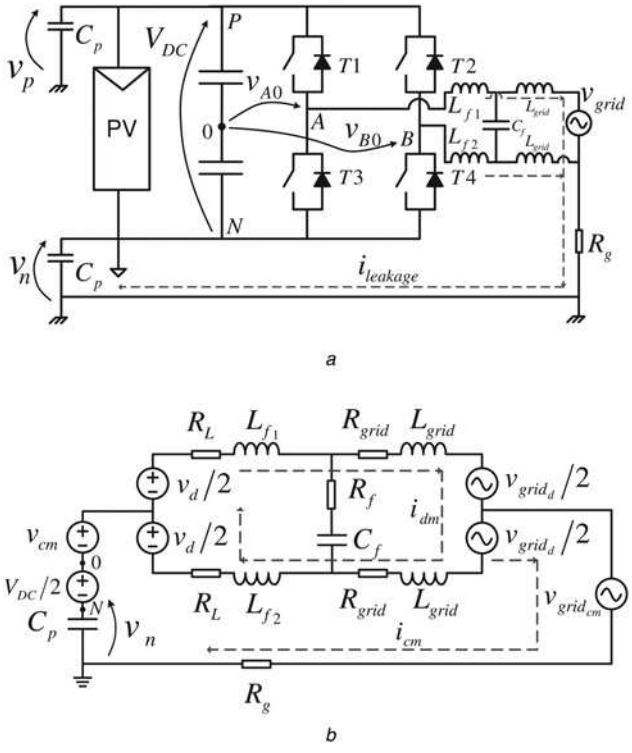

Fig. 2 *CM issue description*

a Grid-connected transformerless inverter with stray capacitance C_p
b Equivalent CM and differential-mode circuits for a grid-connected transformerless inverter

the voltage at the output of the converter, defined as

$$v_{\mathrm{cm}} = \frac{v_{A0} + v_{B0}}{2}, \quad v_{\mathrm{d}} = v_{A0} - v_{B0}, \quad v_{\mathrm{grid_{cm}}} = \frac{v_{\mathrm{grid}}}{2} \tag{2}$$

The first term in (1) is the CM voltage at the output of the converter. The second term is due to the mismatch between the value of the inductors of the inverter output filter and it is expected to be low in case of a good converter design, whereas the third is the CM component of the grid voltage. The last term of (1) is present because the reference point 0 in Fig. 2*b* is at $V_{\mathrm{DC}}/2$ with respect to the negative rail of the DC link. (If the positive pole of the DC link was considered instead, this component would appear with a plus sign). In the derivation of (1), the ground resistance is neglected, since its impedance is much lower compared to the other elements in the circuit. Since V_{DC} is constant, it cannot generate current flowing through C_{p}. Nevertheless, while the inverter is operating, the DC link is affected by a voltage ripple at twice the mains frequency. The amplitude of the ripple depends on the DC-link capacitor, which is usually designed to have small voltage oscillations.

The most influential term of (1) is usually v_{cm}, since it carries high-frequency harmonic content at the converter switching frequency. The contribution of $v_{\mathrm{grid_{cm}}}$, conversely, is typically low, because of the high value of the stray capacitive impedance at grid frequency. The resulting sinusoidal leakage current is usually below the limits imposed by standards [4, 5], unless thin film PV modules (that typically have higher stray capacitance) are used.

To summarise, the ground leakage current is caused by the CM voltages of the system, for this reason it is often referred to as the CM current.

2.2 Potential induced degradation

A degradation of the panels performance after a period of operation was already noticed in the earliest PV plants. Where panels were connected in strings, this phenomenon was particularly observed in the modules nearest to the negative terminal of the PV array. The degradation was discovered not to be related to the natural aging of the material, but to the Coulomb effect [6].

The degradation process is associated with the soda lime glass that is commonly used as the cover or as both the cover and back glass in PV solar modules. In the presence of an electric field, Na+ ions may migrate in large quantities from the glass substrate into the solar cell structure. The potentials of the positive and negative terminals of PV modules are biased with respect to the metal frame, which is grounded for safety standards. This voltage bias induces an electric field that originates the degradation process.

This phenomenon results in a progressive decrease of the maximum available power from the module. However, competing processes make the effect non-linear and history-dependent [7]. Tests have revealed the relationship of mobility to temperature and humidity, with the degradation being accelerated by increases in temperature and/or relative humidity. The PID process was initially attributed only to certain types of solar cells. For instance, the SunPower company indicates the grounding of the positive pole of the PV string as a remedy for its products. Nevertheless, cases where it is the negative pole that has to be grounded have been recorded as well.

In [8], the authors proposed an analytical transient model describing the PID effect for standard crystalline silicon PV cells. The PID mechanism is compared with transistor aging concepts, since both PV cells and metal–oxide–semiconductor field-effect transistors (MOSFETs) have an insulating film within the leakage current path. Arrhenius's law was also considered in the model for including temperature dependencies with specific activation energies for each humidity range, increased risk during rainy events, full/partial recovery, thermal annealing, climate-dependency and history dependency. The voltage bias leads to accumulation of trapped charge over the active layer. This charge can influence the surface field of the semiconductor active layer. In severe cases, accumulation of mobile ions, such as Na^+, leads to delamination when the active layer is biased negatively. The use of Na-free or low Na content glass substrates has been observed to enhance the resiliency to potential-induced degradation, if compared with glass substrates with high Na content. Several models were also proposed to devise accelerated life test procedures to obtain reliable forecasts for the behaviour the different PV technologies [9, 10].

2.3 Transparent conductive oxide (TCO) corrosion

A widely adopted method for fabricating PV panels involves the creation of a thin layer of oxide doped with fluorine (NO_2:F). This transparent conductive oxide layer is an electrically conductive layer employed in thin film PV panels and is housed on the inside surface of the cover glass, see Fig. 3. It serves as a front side electrode, and is very important for thin film panels, as they require, besides a high transparency and conductivity, also the ability to scatter the light under large angles, to improve the panel efficiency.

It was shown in the literature that this layer is subject to corrosion [11–14]; in particular, humidity and temperature accelerate the process. The voltage is then responsible for the damage, whereas the NO_2:F loses adhesion to the glass, as it delaminates. Only negative voltages seem to cause this sort of damage, while positively biased panels do not show this effect.

Researchers still do not agree on the exact chemical reaction responsible for this kind of damage; however, considering the strong dependence on the voltage polarity, several have hypothesised that the sodium ions may migrate from the glass to the TCO, causing a reaction with the fluorine [11]. In particular, in [14] the authors developed a laboratory set-up to test TCO corrosion, where heated up panels were subjected to a positive bias between the metal frame and the cell in order to intentionally drive the sodium ions to the TCO-glass interface.

Since corrosion is directly related to the leakage currents and to the potential of the PV array against the ground, the damages can be prevented by grounding the negative pole of the PV array.

3 Transformerless grid-connected topologies

In the previous section, it has been discussed how different PV panel technologies suffer from different types of degradation, but in the majority of cases all the problems can be attributed to the presence of a potential difference between the PV cells and the ground.

To limit the degradation of PV panels, the potential of the positive and negative terminals of the PV array against the ground must be controlled.

Therefore, it is possible to subdivide single-stage grid-connected transformerless inverters in:

- sinusoidal pole voltages (SPVs), mostly full-bridge-based topologies used in PV systems;
- constant pole voltages (CPVs), mostly half-bridge or neutral point clamped (NPC) topologies;
- grounded pole (GP), also known as doubly grounded topologies.

Fig. 4 shows the ideal voltage waveforms between the positive (v_{p}) and negative (v_{n}) terminals of the PV source and the ground

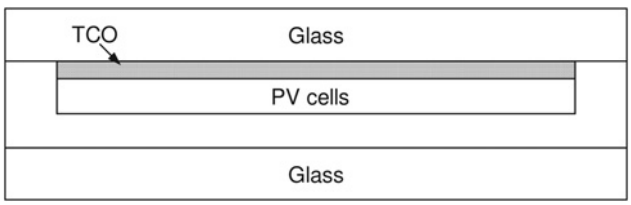

Fig. 3 *Structure of a PV panel with the TCO highlighted*

for each of the above categories. In actual PV systems the presence of parasitic inductances in all the wires and undesired voltage ripple across DC capacitors determines an increased harmonic content, in particular at the converter switching frequency.

In ideal conditions, the full-bridge based topologies present sinusoidal waveforms that are symmetrical with respect to the ground potential. The oscillation at the grid frequency is due to the CM component of the grid voltage that is intrinsically present in v_p and v_n for this family of inverters.

In half-bridge based inverters the sinusoidal component in v_p and v_n is totally eliminated, since the neutral wire of the grid, which is grounded in correspondence of the MV/LV transformer of the mains, is directly connected to the mid-point of the DC voltage source. Nevertheless, a symmetrical DC bias equal to half the DC voltage is still present.

The doubly grounded topologies are those where the negative terminal of the PV source is directly connected to the ground. Their name derives from the fact that the output of the inverter is also grounded, since the neutral wire of the grid is connected to the ground at the mains transformer. Therefore, both the input and output stages of the converter are clamped to the ground potential, and special architectures are required to prevent short-circuits during the inverter operation.

It is important to put in evidence that some topologies of this last class can be modified in order to ground the positive pole of the PV string instead of the negative one. This feature could be very important in case of some kind of PV modules, such as high efficiency SunPower panels or certain thin-film cells.

The grid-connected inverters of the CPV and GP classes allow, ideally, to manage PV generators characterised by large parasitic capacitances to the ground (thin-film cells), while the topologies of SPV class allow to manage only traditional mono- and polycrystalline panels. Despite this fact, most commercial inverters still fall into the SPV category. So far the SPV class has been preferred by manufacturers for three reasons:

- it can reach high efficiencies;
- it needs a DC input voltage only slightly higher than the grid voltage amplitude;
- most of the PV panels currently installed in actual plants are built with traditional silicon technology presenting parasitic capacitances up to 100 nF/kWp, one order of magnitude below the 1 F/kWp typical of thin-film cells.

The inverters of the other two classes present several drawbacks with respect to SPV. For example, CPV inverters need a doubled DC voltage input, while the inverters of the GP class present a lower conversion efficiency because of high voltage and current stress of the power switches. The three classes of inverter topologies will be analysed in detail in the following sections.

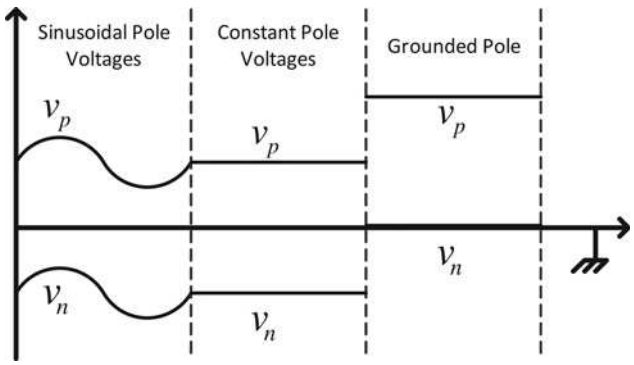

Fig. 4 *Voltages of the positive and negative poles of the PV source against ground during converter operation for different families of grid-connected transformerless inverters*

4 SPV class of transformerless inverters

According to what was reported in Section 2.1, the voltages of the positive and negative rails of the DC source against the ground for full-bridge based topologies (v_p and v_n) can be expressed by the following formula

$$v_n = -v_{cm} - \frac{v_d(L_{f_2} - L_{f_1})}{2(L_{f_2} + L_{f_1})} + v_{grid_{cm}} - \frac{V_{DC}}{2}$$
$$v_p = -v_{cm} - \frac{v_d(L_{f_2} - L_{f_1})}{2(L_{f_2} + L_{f_1})} + v_{grid_{cm}} + \frac{V_{DC}}{2} \quad (3)$$

The sinusoidal component is the CM component of the grid voltage, with amplitude equal to half of the grid voltage's. The v_{cm} term represents the CM output voltage generated by the converter during the operation. Ideally, were v_{cm} constant, no CM currents due to the contribution of the converter would arise, and the ground leakage current would be at grid frequency [(4) can be used to calculate the amplitude of the ground leakage current]. As reported in Section 2, the high impedance of the parasitic capacitance at grid frequency usually renders this component negligible, unless particular types of panels (i.e. thin film) or plants of significant size are considered

$$I = \omega C_p \frac{V_{grid}}{2} \quad (4)$$

The following subsections describe some of the most interesting SPV class topologies.

4.1 Pure full-bridge topologies

Fig. 5 shows the schematic of a simple full-bridge topology with a passive CM filter added in order to accomplish EMI goals and to reduce the harmonic content of ground leakage current at the switching frequency [15]. It is possible to use a small CM filter if the full-bridge is driven by a bipolar pulse-width modulation (PWM), but the required filter can result significantly larger if a more efficient PWM is chosen. A hybrid full-bridge is often used in commercial PV inverters where the two low side power switches T3, T4 are high frequency MOSFETs (in some case two or three in parallel connection to reduce conduction losses) and the two high side switches T1 and T2 are line-frequency insulated-gate bipolar transistors (IGBTs). This solution allows to obtain very high efficiencies at the expense of a v_{cm} variation of $V_{DC}/2$ at the switching frequency. In this case, the ground leakage current can be kept at acceptable levels only with heavy passive CM filtering. Moreover, only unity power factor operation is possible for this topology.

Another recently proposed solution is based on the use of an active CM filter, which compensates in feed-forward the v_{cm} variation of the full-bridge topology driven by the unipolar PWM [16]. Fig. 6

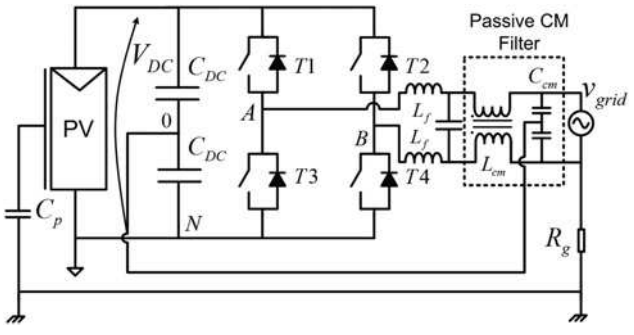

Fig. 5 *Full-bridge inverter with passive CM filter for ground leakage current reduction*

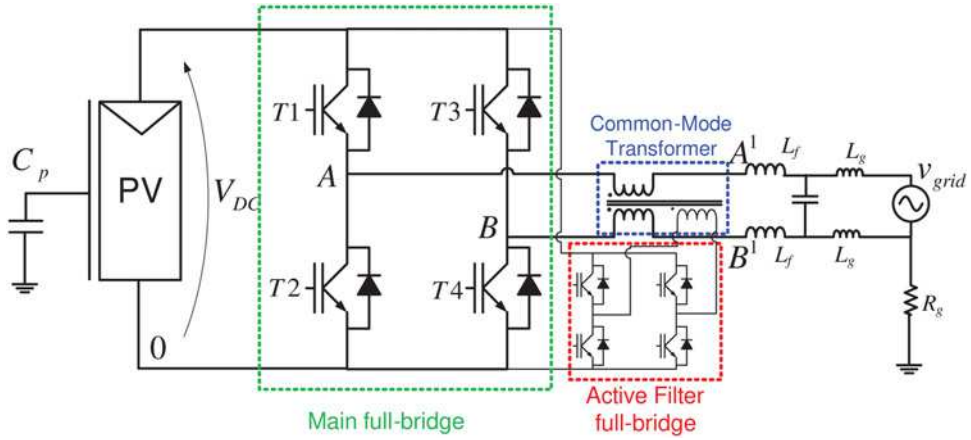

Fig. 6 *Full-bridge driven by unipolar modulation with active CM filter [16]*

shows the CM transformer which operates the CM voltage compensation. It is driven by a low power additional full-bridge which provides only the magnetising current to the CM transformer. The solution allows to use the simple and effective unipolar modulation, which presents a current ripple at twice the switching frequency and the possibility to operate with any power factor. The evident drawback is the use of four additional power switches and an additional magnetic component (more complicated than the traditional CM inductor used only for EMI), although the additional components only need very low power ratings. Due to the need for freewheeling paths in the full-bridge, traditional IGBTs have to be used in this solution. This is because MOSFETs have exhibited high failure probability when used in hard-switching power converters due to the poor dynamic performance of the intrinsic body diode. As shown in [17], it is possible that the parasitic BJT of the MOSFET structure is activated due to the reverse recovery of the internal diode.

4.2 Full-bridge-based topologies

High frequency CM voltage variations happen in full-bridge-based inverters during the freewheeling intervals of the PWM cycle. This subsection presents inverter topologies that can keep the CM voltage constant, a feature that is generally implemented in one of two ways:

- with the disconnection of the grid from the PV source during the freewheeling intervals of the output current; this is obtained by means of additional power switches;
- by actively clamping the CM voltage to the mid-point of the DC link.

The latter technique ensures better performance, because the voltage waveforms of v_{A0} and v_{B0} do not depend on the parasitic components or on the perfect match of power switch parameters as in the first case [18]. The drawback is usually an increased component count and the possibility to unbalance the DC-link capacitor divider.

Fig. 7*a* depicts two solutions that disconnect the grid from the DC source. The two additional dotted blocks are used alternatively: one is inserted in the DC side of the converter, the other in the AC side [19–21]. These solutions ensure good performances only when the inverter operates at unity power factor. This is becoming a heavy limitation for these solutions as more and more countries worldwide adopt standards for the connection of grid-connected inverters that enforce the injection of a certain amount of reactive power when required.

The use of DC or AC decoupling allows the disconnection of the grid voltage from the PV plant during the grid current freewheeling intervals. The AC decoupling block is employed in the Sunways inverter named highly efficient reliable inverter concept (HERIC),

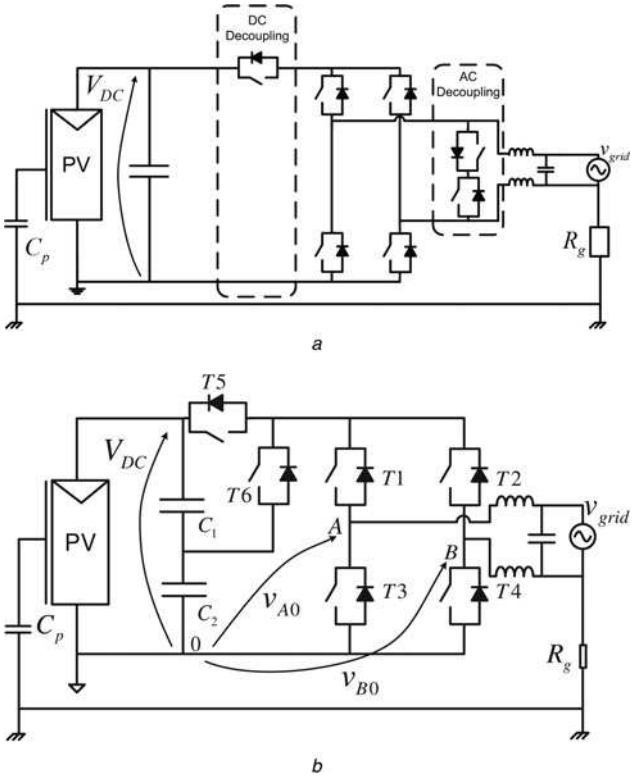

Fig. 7 *Full-bridge with AC or DC decoupling blocks*

a HERIC and H5 topologies
b Topology proposed in [22]

whereas the DC decoupling is used in the SMA H5 converter. In both cases, the output voltage is a three-level waveform with the fundamental component at the switching frequency of the converter. Therefore, in the output filter design, a current ripple at said frequency has to be taken into account.

The efficiency of the two above converters is up to 98%. To maximise the efficiency, these solutions can employ MOSFETs for some of the power devices. For instance, the H5 topology can use MOSFETs in the low side of the full-bridge. However, it is important to evidence that silicon MOSFETs can be used only at unity power factor operation. If the converter needs to manage reactive power as well, IGBTs or SiC MOSFETs must be used instead.

It is also important to note that a significant v_{cm} variation can occur in case of asymmetric commutations of the power switches [18].

IET Renew. Power Gener., 2016, Vol. 10, Iss. 2, pp. 260–273

A simple approach to fix the v_{cm} during the freewheeling intervals is to modify the H5 topology by adding a device connected between the mid-point of the DC link and the high-side of the full-bridge. This topology was proposed in [22] and is shown in Fig. 7*b*.

The main drawback of this solution is that the DC-link voltage must be equally divided between the capacitors C_1 and C_2 in order to obtain the minimum leakage current. As a matter of fact, if a diode is added to the mid-point, the unidirectional current flow will cause the mid-point voltage to drift unless countermeasures are employed, i.e. a resistive divider or additional switches to balance the mid-point. Moreover, an uncontrolled drift of the mid-point voltage poses a serious safety threat, as unbalanced series-connected capacitors might exceed their individual voltage rating. These solutions obviously deteriorate the efficiency of the converter and add complexity.

Another solution based on a modification of an existing topology was proposed in [23] (Fig. 8). In this topology, a bidirectional switch (BDS) in addition to the full-bridge was implemented using a diode bridge rectifier together with an additional device, hence the name HB-ZVR (H-bridge zero voltage rectifier).

The modulation strategy is very similar to HERIC's. Considering the positive half cycle, T1 and T4 commutate at high frequency supplying the DC-link voltage to the output, while T5 switches complementarily to supply the zero voltage.

By connecting the source of the additional device to the mid-point, it is ensured that v_{A0} and v_{B0} are clamped to $V_{DC}/2$ when supplying the zero voltage. An additional diode is inserted in the current path to prevent short-circuiting the capacitors.

As in the previous case, it is extremely important to control the mid-point voltage, otherwise ground leakage current will increase. This task is complicated by the presence of the diode, which presents the same problem as in [22]. The balancing of the voltage across the DC-link capacitors was not addressed in [23].

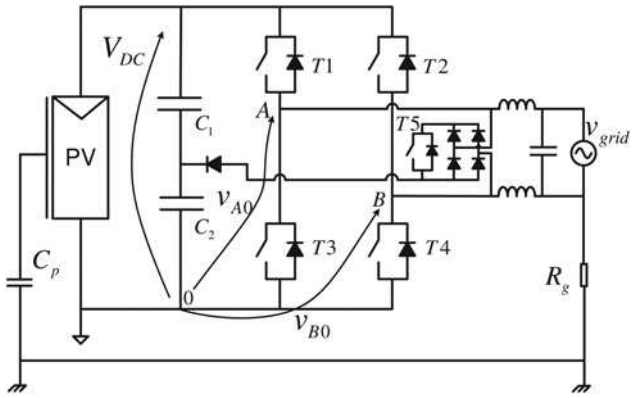

Fig. 8 *Topology proposed in [23]*

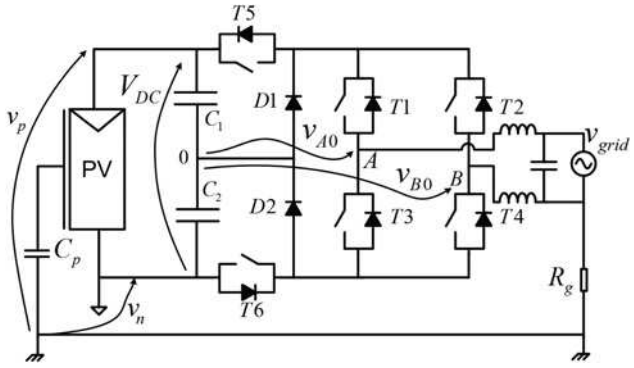

Fig. 9 *Topology proposed in [24, 25]*

4.3 H6-based topologies

The solution proposed in [24] comprises six power switches and two diodes. The inverter is named H6 and, as can be seen in Fig. 9, in addition to the H-bridge structure, two switches are inserted in the DC rails, while two diodes are connected between the DC rails and the mid-point of the DC source.

This topology is driven by a particular modulation strategy. A diagonal of the full-bridge is kept on during a whole grid voltage half-wave (for instance T1 and T4 while the grid voltage is positive), whereas the DC decoupling transistors, T5 and T6, commutate simultaneously at the switching frequency. During the output current freewheeling interval, when T5 and T6 are off, all the four full-bridge switches are on; the grid current then splits across the two paths constituted by the transistor T1 and the freewheeling diode of T3, and the transistor T4 and the freewheeling diode of T2. The additional diodes D1 and D2 fix the CM voltage to $V_{DC}/2$.

In [25], the same architecture is driven by a different modulation strategy. In this case, the four switches of the H-bridge are driven as in the case of unipolar PWM, whereas the two DC devices T5 and T6 do not commutate simultaneously, but switch off alternatively when the current freewheels, respectively, in the upper and lower sections of the H-bridge. The additional diodes do not continuously conduct current, but clamp the load potential at $V_{DC}/2$ during the freewheeling intervals. Both solutions allow to fix v_{cm} to the desired voltage during the freewheeling intervals. The drawback of the topology is the presence of four power devices in series during the on state of the diagonals of the full-bridge. This determines higher conduction losses for H6-based topologies with respect to the other ones.

Differently from [24], in [25], the ripple of the output current is at twice the switching frequency. Therefore, for a given switching frequency of the converter, the size of the filter inductor can be divided by two.

The H6-basic topology can be also employed to generate five output voltage levels, since the DC-link capacitor divider offers an additional voltage level. This was described in [26]. This work presents an in-depth analysis of the balancing strategy of the mid-point DC-link voltage. However, the output CM voltage of this topology is not constant, determining a poor performance in terms of ground leakage current.

4.4 Full MOSFET topologies

Using MOSFETs for all the transistors allow to obtain a very high efficiency, especially in terms of conduction power losses when the PV source provides only a fraction of the rated power.

Some inverters manufactured by STECA Elektronik GmbH adopt a full MOSFET topology (see Fig. 10) which merges the output and CM filters of the inverter.

The full-bridge commutates at line frequency, while the rectified sinusoidal current is realised by a buck-type converter connected at the output of the PV source [27]. The commutation of T5 and

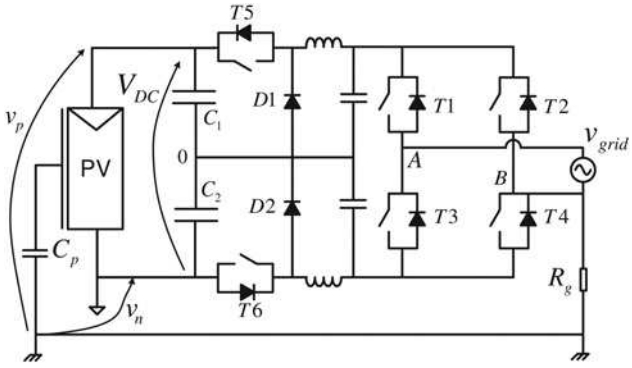

Fig. 10 *STECA topology*

T6 allow to obtain three voltage levels (V_{DC}, $V_{DC}/2$ and 0) while the inductors and capacitors work a differential-mode and CM filter.

An effective solution presenting the same number of switches and diodes was proposed in [28]. Fig. 11*a* illustrates the scheme for this inverter. The top device in one leg and the bottom device in the other leg are switched simultaneously during the PWM cycle and the middle device operates as a polarity selection switch depending on the grid half cycle. During the positive half cycle, for example T4 remains on, whereas T3 is off. When T1, T6 and T4 are on, the converter feeds positive voltage to the load, and when T1 and T6 turn off the current freewheels through diode D1. Again, the current ripple is at the switching frequency of the converter.

Furthermore, like many other topologies in the literature, the solution in [28] was designed for MOSFET devices, in order to achieve very high efficiency. The modulation strategy was studied in order to avoid the conduction of the MOSFET antiparallel body diode; in fact, the freewheeling interval happens with the conduction of unidirectional devices, i.e. diodes D1, D2. Thus, this converter can operate only with unity power factor and the capability of managing reactive power, as mandated by recent regulations, is not present.

A novel topology was recently presented in [29], its architecture is shown in Fig. 11*b*. This topology was developed in order to avoid the conduction of the antiparallel diodes of the devices.

For example, during the positive half cycle two configurations are possible:

(i) T1 and T3 on (T5 off): $v_{A0} = V_{DC}$, $v_{B0} = 0$, $v_{cm} = V_{DC}/2$.
(ii) T1 and T3 off (T5 on): $v_{A0} = v_{B0} = V_{DC}/2$, $v_{cm} = V_{DC}/2$.

Since a DC source capacitor divider is not employed in this architecture, the negative terminal of the PV source is taken as reference in the v_{cm} formula. The drawback of this topology is the increased number of devices and the need for two inductors.

The three full MOSFET topologies described above have as their main drawback the inability to handle reactive power, as required by many recent international standards. However, as MOSFETs with slow body diodes can be employed, these solutions can lead to very high efficiencies.

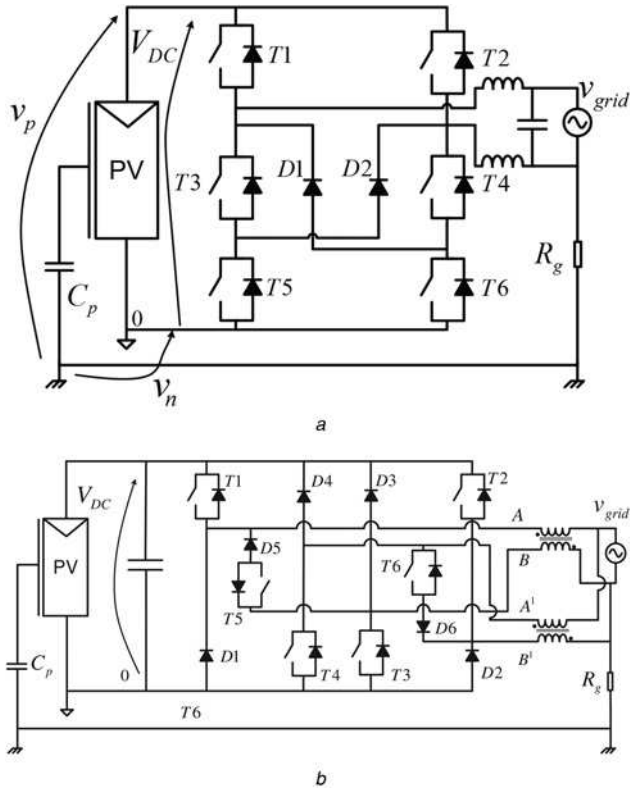

Fig. 11 *Topologies that avoid body-diode conduction*
a H6-type topology proposed in [28]
b Topology proposed in [29]

4.5 Quasi-sinusoidal terminal voltages

In [30], a particular structure of parallel buck converters is employed to ensure that, during each half cycle of the grid voltage, the neutral conductor is connected either to the high or to the low side of the DC link (Fig. 12). While this can greatly reduce the ground leakage current, special care must be taken at the zero-crossing of the grid voltage.

In this last case, the ground voltage is equal to the full-grid voltage during the positive half cycle, while it corresponds to the DC-link voltage during the negative half cycle. No discontinuities are present, so the ground leakage current is low. Hence the PV terminal to ground voltages presents a grid frequency first harmonic, for our purposes, this topology is presented together with the full-bridge-based ones.

Since all these architectures aim at reducing the high-frequency CM voltage, they are intrinsically very robust to variations of the grid impedance and of the ground return path impedance. However, due to the presence of the sinusoidal CM voltage across the parasitic capacitance, only Si panels can be adopted, as thin-film presents a very high parasitic capacitance. If these latter panels were adopted, the grid frequency component of the leakage current alone would be sufficient to cause the residual current devices to trip.

5 CPV class of transformerless inverters

In CPV topologies the neutral wire of the grid is directly connected to the mid-point of the DC source, whereas the phase wire is connected to the PWM output of the converter through the output filter. In this way, the voltage across the parasitic capacitance is clamped to a constant value and, from (5), only the voltage ripple of the DC source affects the leakage current, and its contribution is negligible

$$v_n = -\frac{V_{DC}}{2} - \frac{v_{DCripple}}{2}$$
$$v_p = \frac{V_{DC}}{2} + \frac{v_{DCripple}}{2} \quad (5)$$

Thin-film panels that do not require grounding can be employed with these architectures; however, since for their proper operation they require the neutral conductor to be effectively connected to the earth potential with a low-impedance path, high impedance of the grid or of the ground return path can negatively affect the performance of these topologies in a very marked way. This issue is seldom considered in the literature, where the experimental test beds are usually built with very low ground return path impedance.

The best known topology of this family is the NPC inverter. It was first proposed in [31] for a three-phase application and subsequently employed also in single-phase solutions [32].

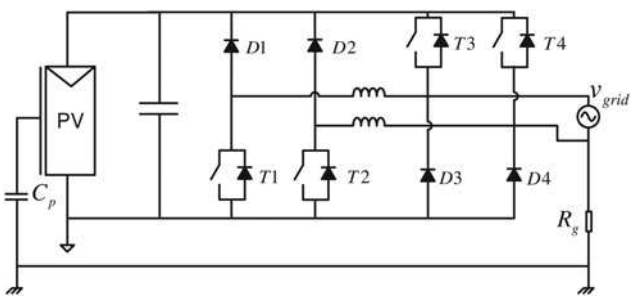

Fig. 12 *Topology proposed in [30]*

The topology is shown in Fig. 13*a*. The DC link is composed of two series capacitors with equal voltage, with $V_{DC} = V_{C_1} + V_{C_2}$. The neutral wire of the grid is connected to the mid-point of the DC voltage source. The NPC inverter comprises four switches (T1–T4) and two clamping diodes (D1 and D2).

During the positive half-wave, T2 is kept on while T1 commutates at the switching frequency, whereas, for the negative half-wave, T3 is kept on while T4 commutates at the switching frequency. During the freewheeling intervals, the output current circulates through the on-state IGBT and the D1 or D2 diode depending on the sign of the grid voltage. The three-level output voltage presents a ripple at the same frequency as the PMW carrier.

Despite the intrinsic high efficiency and the virtual absence of switching frequency ground leakage current, the basic NPC topology suffers from a number of limitations. It needs a doubled DC bus voltage to obtain the same output voltage as full-bridge-based topologies and it distributes power losses unevenly among its power devices. Despite these limitations, if having a potentially higher DC-link voltage does not represent a problem for the application, NPC is a simple and cost-effective solutions that allows to realise a transformerless power system with high current controllability (reactive power injection is possible), good efficiency and a simple modulation.

By replacing the clamping diodes D1 and D2 with active switches (Fig. 13*b*), the active NPC (ANPC) topology is obtained [33]. ANPC inverters can deliver reactive power and have higher efficiency than the basic NPC. Moreover, different PWM strategies can be implemented, considering the added degrees of freedom that this topology offers with respect to the traditional NPC. In [34], three different modulations for the ANPC topology were proposed. Among them, an interesting solution permits to double the apparent switching frequency of the converter output voltage without greatly affecting the power losses, thus enabling the use of a smaller filter inductor.

Conergy AG patented an NPC topology [35] in which the output of a half-bridge is clamped to the neutral via a series BDS (Fig. 14).

During the positive half-wave of the grid voltage T1 and T3 commutate at the switching frequency, whereas T2 is kept on. On the contrary, during the negative half-wave T2 and T4 switch at high frequency while T3 is kept on. This solution provides very high efficiency since during the active stage, when the inverter output voltage is positive or negative, only one device is conducting, whereas when the output voltage is zero, the current flows through two devices. The only disadvantage with respect to NPC is that, in this case, the voltage that the devices have to withstand when they are off is equal to the DC voltage source, whereas in NPC converters it's only $V_{DC}/2$. Therefore, devices with a much higher breakdown voltage have to be used.

The Conergy topology can provide reactive power. It was further improved in [36] by having only one active switch in the BDS.

Another recent patent, filed by Vincotech GmbH, deals with the poor recovery performance of body diodes by providing alternative conduction paths for the current [37]. The alternative conduction paths are represented in Fig. 15 by diodes D3, D4 and inductances L_{fi}. T1 and T2 operate at the switching frequency, while T3 and T4 switch at the grid frequency. The claimed efficiency is very high (98.59%), and the inverter can handle reactive power.

The use of advanced power devices can further improve efficiency and reduce the output filter size by increasing the switching frequency. PV inverter market leader SMA has recently unveiled an inverter based on the Conergy topology that employs SiC MOSFETs, while in [38], the authors propose an NPC-based architecture that integrates CoolMOS devices by Infineon, also helping to evenly distribute losses among the power devices. The problem of uneven switching losses distribution can also be tackled by employing suitable modulation strategies in ANPC converters [39].

The efficiency can be improved by employing soft switching as well, as proposed in [40].

Moreover, the concept of a stacked NPC (SNPC) converter was introduced in [41], in which an additional branch, comprising two anti-series devices, is added to the NPC structure and inserted between the converter output and the mid-point of the DC source (Fig. 16*a*). The concept was enhanced with the active SNPC (ASNPC) [42], enabling a better loss distribution by substituting power switches for diodes (Fig. 16*b*).

The need for a doubled DC bus voltage can be advantageously exploited in multistring PV fields by connecting two strings in series. This arrangement is proposed in [43], in which two independent boost converters are used to elevate the string voltages. One drawback is represented by the need to keep the two halves of the DC-link balanced, even in case of power mismatch between the strings supplying them (e.g. in case of partial shading). In [43], a specially programmed controller is used to keep the DC-link balanced; [44] balances the DC link by injecting even harmonics, that electric utilities subject to less stringent regulations than the DC component.

Another solution to the need for the augmented DC-link voltage is proposed in [45] through an NPC with a quasi-impedance-source (QZS) input stage that can boost the voltage. Moreover, the QZS has an excellent shoot-through immunity, which ensures enhanced reliability. Similar shoot-through protection is achieved by the split-inductor NPC converter [46].

Zhang *et al.* [47] present a systematic construction of NPC-based topologies starting from elementary 3-device building blocks, yielding a deeper insight into this type of converter architecture.

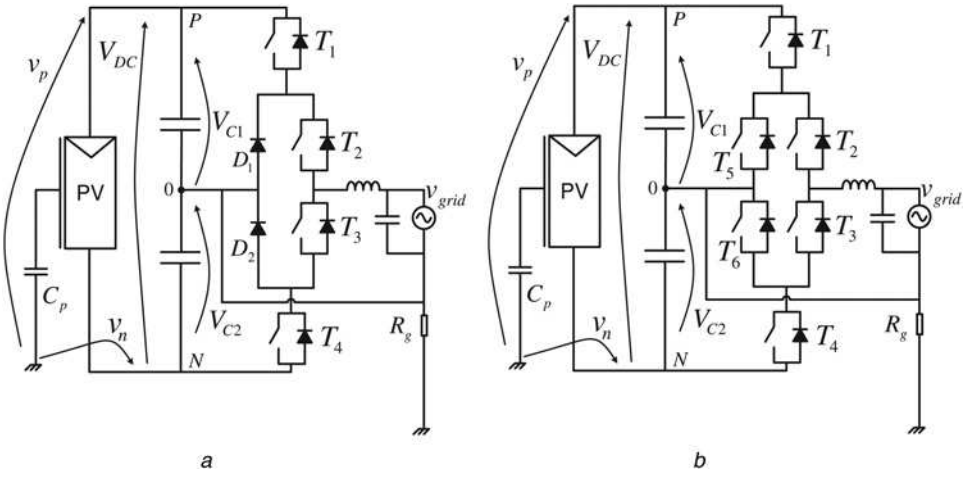

Fig. 13 *NPC converters*

a Standard NPC topology
b ANPC topology

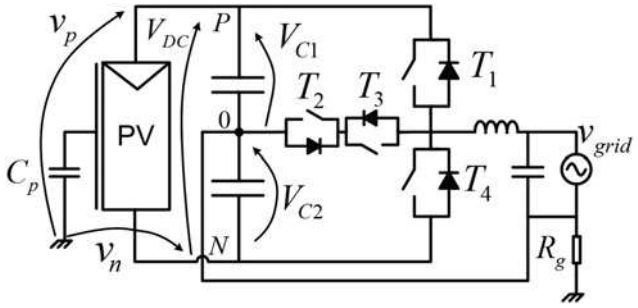

Fig. 14 *Clamped half-bridge topology patented by Conergy*

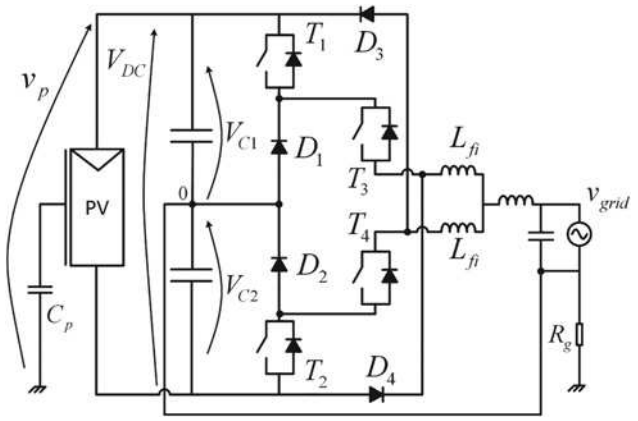

Fig. 15 *Topology patented by Vincotech*

A comprehensive comparison of several H-bridge-based and NPC-based PV converters is carried out in [33]. Design parameters of the various topologies are optimised in terms of efficiency and reliability, considering lifetime cost versus energy production and geographical location. NPC-based architectures often end up among the best in terms of efficiency and cost-effectiveness.

6 GP class of transformerless inverters

The GP inverter family comprises the doubly grounded inverters, in which the negative pole of the PV source is grounded. The voltage v_n is zero, whereas v_p is equal to the DC source voltage (6). In this category, several topologies have been proposed, and in [1] they fall under the category of single-stage step up transformerless topologies. Most of them are variations of the boost or buck–boost converter, like the one presented in [48]. For this reason, in this work only the most relevant solutions in terms of topology will be reported.

$$\begin{aligned} v_n &= 0 \\ v_p &= V_{DC} + v_{DCripple} \end{aligned} \tag{6}$$

Since the output of the converter is also grounded through the neutral wire of the grid, particular inverter configurations have to be considered to avoid short-circuit conditions.

The topology proposed in [49] is presented in Fig. 17. During the positive half-wave T1 and T3 are on, while T4 and T5 switch complementarily at PWM frequency to synthesise the correct output voltage. The flying capacitor is connected in parallel with the DC link, and it is charged at the full DC source voltage. During the negative half wave T5 is kept on, while T1 and T3 switch synchronously and T2 in complement to them in order to generate the negative output voltage.

When T1 and T3 are on the inverter outputs the zero voltage level, and the flying capacitor is charged. When T2 switches on, T1 and T3 turn off, and the output voltage equals the opposite of the DC voltage, supplied by the flying capacitor C2.

However, the stresses on the devices are not balanced, in fact T3 is subject not only to the output current but also to the flying capacitor charging current. Since the size of the capacitor must be large in order to effectively decouple the AC load power from the DC source, the charging current of the flying capacitor can present high surge peaks, increasing the conduction power losses.

An alternative solution was proposed in [50] and is shown in Fig. 18*a*. It belongs to the category of the so-called flying-inductor converters. The basic inverter topology is composed of a buck–boost converter that can be shifted according to the positive and negative outputs of the grid.

During the positive half-wave of the grid voltage T4 and T5 are on, T3 is off, while T1 and T2 switch simultaneously at high frequency. When T1 and T2 are on the inductor L is charged, and when they turn off the current can flow through T4, T5 and the diodes D1 and D2. During the negative half-wave behaviour is similar: T2 and T3 are on, T4 and T5 are off, whereas T1 switches at high frequency.

The drawback of such solution is the discontinuous waveform of the output current that requires large filter capacitors. To address this problem, a new circuit, as illustrated in Fig. 18*b*, was proposed in [51], though the increased amount of switches negatively affects the efficiency and robustness of the total system.

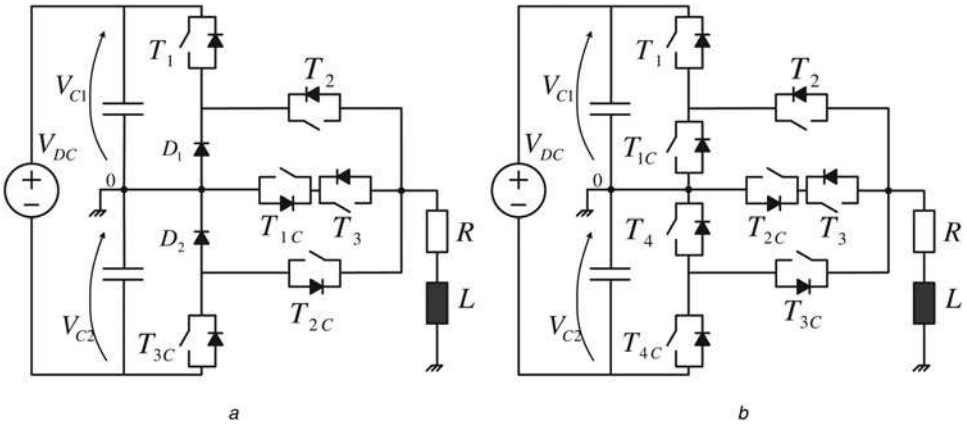

Fig. 16 *Stacked NPC converters*

a SNPC topology
b ASNPC topology

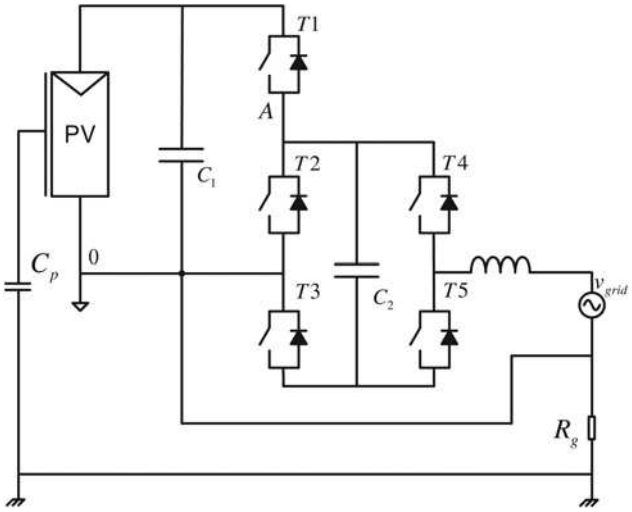

Fig. 17 *Topology proposed in [49]*

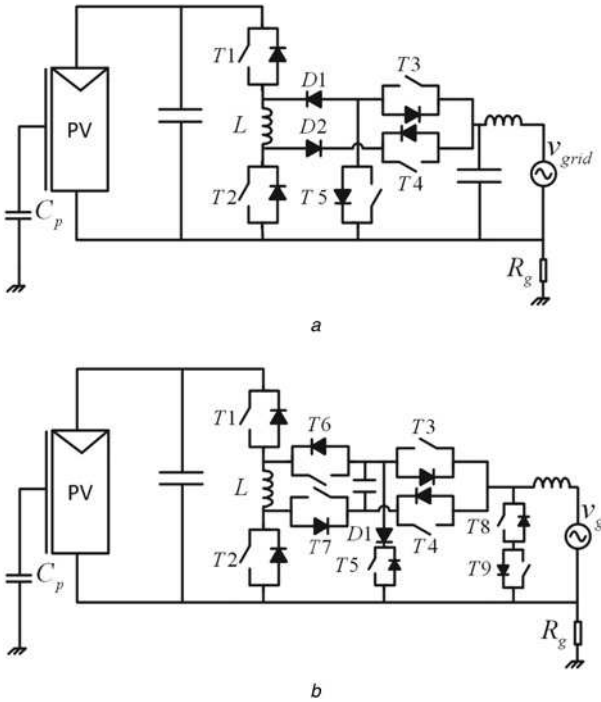

Fig. 18 *Topologies proposed in*

a Topology [50]
b Topology [51]

In the doubly grounded scenario, there is also another topology derived by the Z-source inverter (ZSI): it is called the semi-quasi-Z-source inverter. Fig. 19*a* shows the basic architecture proposed in [52]. In this work, the experimental validation was conducted only for stand-alone applications, but the converter can be used in grid-connected systems as well. The topology presents only two power switches controlled complementarily. However, these two devices are highly stressed and the conduction and switching power losses can result very high. In fact, with an optimal design and during the worst time interval of the sinusoid output voltage/current, the peak voltage across the power switches is three times the input DC voltage, while the peak current is three times the amplitude of the output current. For these reasons, this solution needs high performance power switches, such as high voltage SiC MOSFETs, and is effective only in case of low power PV systems or microinverter applications.

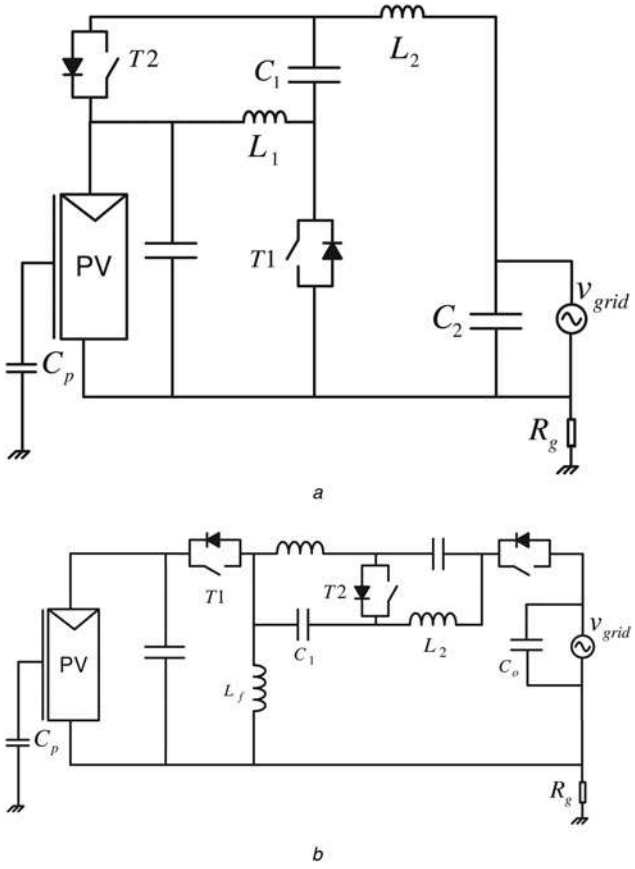

Fig. 19 *Z-source-based topologies*

a Semi-quasi- ZSI proposed in [52]
b Boost-based-TSTS-ZSI [53]

A family of topologies based on the ZSI concept is proposed in [53] featuring three switches and three states (TSTS). In particular, the buck–boost-based TSTS-ZSI is reported in Fig. 19*b*. This topology, with respect to the semi-ZSI and semi-quasi-ZSI presents the advantage of a linear characteristic, and a reduced voltage stress among the switches and the capacitors.

7 Topology comparison: operation and qualitative power loss analysis

To obtain a fair, albeit qualitative, comparison of the semiconductor power losses, a base switching frequency of f_s will be considered. Considering the same output passive filter for every topology, each one will operate at a multiple of this base frequency in order to obtain the same value of the maximum ripple of the injected grid current. The unipolar full-bridge topology is considered in this analysis as a reference case. For instance, if a PWM frequency of f_s is considered for the unipolar full-bridge, the HERIC and H5 topologies will be driven by a PWM at $2f_s$.

Table 1 shows, for several previously described topologies, the conduction power losses during the active and freewheeling intervals, the number of transistor commutations (with the switching voltage) for every switching period $T_s = 1/f_s$ and the number of the needed transistors and diodes with their breakdown voltage. It is interesting to see that the Steca topology, despite the high number of transistors, presents theoretically the lower switching power losses and since it can use MOSFETs for all the transistors, the European efficiency of this converter can result very high.

The Vincotech topology is also very efficient, and can provide reactive power as well.

Topology [53] does not present a clear zero state, so it is not included in the table. This topology, despite representing a very

Table 1 Semiconductor power loss comparison (qualitative)

Topology	Power losses in a switching cycle T_{PWM}		Transistors (+diodes) × breakdown voltage
	Conduction path	Number of commutations (switching voltage)	
unipolar full-bridge	2 transistors 1 transistor + 1 diode	2 turn on (V_{DC}) 2 turn off (V_{DC})	$4 \times V_{DC}$
HERIC	2 transistors	4 turn on $\left(\frac{V_{DC}}{2}\right)$	$4 \times V_{DC}$
	1 transistor + 1 diode	4 turn off $\left(\frac{V_{DC}}{2}\right)$	
H5	3 transistors	2 turn on $\left(\frac{V_{DC}}{2}\right)$	$4 \times V_{DC}$
	1 transistor + 1 diode	2 turn off $\left(\frac{V_{DC}}{2}\right)$	$1 \times \frac{V_{DC}}{2}$
H6/UniTL	4 transistors	2 turn on $\left(\frac{V_{DC}}{2}\right)$	$4 \times V_{DC}$
	1 transistor + 1 diode	2 turn off $\left(\frac{V_{DC}}{2}\right)$	$2(+2) \times \frac{V_{DC}}{2}$
Steca	4 transistors	1 turn on $\left(\frac{V_{DC}}{2}\right)$	$2(+2) \times \frac{V_{DC}}{2}$
	3 transistors + 1 diode 2 transistors + 2 diodes	1 turn off $\left(\frac{V_{DC}}{2}\right)$	$4 \times V_{DC}$ (low frequency)
Topology [28]	3 transistors	2 turn on $\left(\frac{V_{DC}}{2}\right)$	$4(+2) \times V_{DC}$
	1 transistor + 1 diode	2 turn off $\left(\frac{V_{DC}}{2}\right)$	$2 \times \frac{V_{DC}}{2}$
Topology [30]	2 transistors	2 turn on $\left(\frac{V_{DC}}{2}\right)$	$4(+4) \times V_{DC}$
	1 transistor + 1 diode	2 turn off $\left(\frac{V_{DC}}{2}\right)$	
NPC	2 transistors	1 turn on $\left(\frac{V_{DC}}{2}\right)$	$4(+2) \times \frac{V_{DC}}{2}$
	1 transistor + 1 diode	1 turn off $\left(\frac{V_{DC}}{2}\right)$	
ANPC	2 transistors	2 turn on $\left(\frac{V_{DC}}{2}\right)$	$6 \times \frac{V_{DC}}{2}$
	2 transistors	2 turn off $\left(\frac{V_{DC}}{2}\right)$	
Conergy	1 transistor	2 turn on $\left(\frac{V_{DC}}{2}\right)$	$2 \times V_{DC}$
	1 transistor + 1 diode	2 turn off $\left(\frac{V_{DC}}{2}\right)$	$2 \times \frac{V_{DC}}{2}$
Vincotech	2 transistor	1 turn on $\left(\frac{V_{DC}}{2}\right)$	$(2) \times V_{DC}$
	1 transistor + 1 diode	1 turn off $\left(\frac{V_{DC}}{2}\right)$	$4(+2) \times \frac{V_{DC}}{2}$
Topology [50]	2 transistors 2 transistors + 2 diodes	4 turn on (V_{DC}) 4 turn off (V_{DC})	$4(+2) \times V_{DC}$
Topology [52]	1 transistor + 1 diode 1 transistor + 1 diode	2 turn on (V_{DC}) 2 turn off (V_{DC})	$2 \times 2V_{DC}$

good and simple single-stage solution, implies double voltage and current stress, when compared with a full-bridge topology, i.e. when it is operating with unity voltage gain for a fair comparison.

The performances of the different topologies analysed in the previous sections are compared in Table 2 where strengths and weaknesses of each topology are summarised.

The Steca and Vincotech topologies are the best in terms of efficiency, but Steca is unable to provide reactive power. Topologies [28, 30] and plain NPC as well cannot provide reactive power; therefore, all these topologies are not suitable for complying with the new regulations.

Concerning the ground leakage current, all the CPV architectures perform very well, but they all need a doubled DC bus voltage. H6/UniTL and the Steca topology have very good efficiency as well, together with the full MOSFET architectures, which conversely cannot provide reactive power.

8 Selected simulations

To show some characteristic waveforms of the different topologies, one example for each classification was chosen. Basic requirements are the possibility to handle reactive power and representing a good trade-off between complexity and efficiency. In particular, the selected topologies are HERIC for the SPV category, the standard NPC for CPV, and the topology presented in [53] among the GP converters.

Simulations are carried on considering the parameters are shown in Table 3. To make a fair comparison and show the peculiarities of each choice, similar output THD waveforms were considered. As can be seen from the required DC voltage, the NPC has a doubled DC-link level with respect to a full-bridge solution, while topology [53] exhibits boost capabilities, and for this reason a halved voltage is sufficient.

The simulation results are reported in Figs. 20*a*–*c*. HERIC shows the characteristic sinusoidal pole voltages, meaning that a sinusoidal leakage current appears even in the ideal simulation conditions, thus limiting the application of this solution to poly-crystalline panel technology. NPC is virtually free from leakage current, due to the constant pole voltage. Solution [53] performs well, although, with the chosen voltage and current level, a high value of output capacitance is needed.

9 Future trends

The earliest PV inverter designs used a line frequency transformer to couple the converter to the mains providing galvanic isolation. The transformer eliminated the problems of ground leakage current and DC current injection, and the expertise gained in designing AC power supplies could be employed to realise grid-connected inverters without significant changes.

The pursuit of the maximum efficiency together with cost and weight reduction has stirred, in recent years, a flourishing research activity in transformerless grid-connected inverter topologies. The first designs

Table 2 Topologies comparison

Topology	Efficiency	Reactive power	Leakage current	Pro	Cons
HERIC	++	+	+	high efficiency	residual line frequency leakage current
H5	+	+	+	low component count	uneven device stress
H6/UniTL	+	+	++	very low leakage current	lower efficiency
Steca	+++	–	++	very high efficiency	leakage current
Topology [28]	++	–	+	high efficiency	no reactive power
Topology [30]	++	–	+	high efficiency	no reactive power
NPC	+	+	++	3-level with few components	uneven device stress
ANPC	++	+	++	improved NPC	increased complexity
Conergy	+	+	++	reduced component count	high devices stress
Cincotech	+++	+	++	very high efficiency	additional devices needed
Topology [50]	+	+	+	boost capability	high devices stress
Topology [52]	++	+	+	boost capability	high devices stress
Topology [53]	++	+	+	boost capability	high devices stress

IET Renew. Power Gener., 2016, Vol. 10, Iss. 2, pp. 260–273

Table 3 Simulation parameters

Parameter	Value	Unit
grid voltage	230	Vrms
grid frequency	50	Hz
grid current	13	Arms
switching frequency	20	kHz
total output inductance	2	mH
filter capacitor	5	F
grid stray inductance	100	H
DC voltage (HERIC)	440	V
DC voltage NPC	880	V
DC voltage [53]	220	V
boost inductance [53]	675	H
Z-source inductance [53]	1	mH
Z-source capacitance [53]	19	F
filter capacitance [53]	100	F

were modifications of the full-bridge topology with additional switches, then newer topologies have surfaced with optimised freewheeling paths allowing the use of MOSFETs. At the same time, the work on multilevel NPC topologies was applied to transformerless inverters, due to the undeniable advantage (in terms of ground leakage current) of having constant pole voltages of the PV field.

With the increasing penetration of grid connected renewable energy systems new problems started arising in the distribution grid, initially designed for unidirectional power flow from big centralised power plants to the loads. One of the main issues is that the legacy distribution grid cannot effectively support a large amount of distributed power generation systems resulting, in extreme cases, in grid voltage/frequency instability. These mishaps can happen when the power generated by the renewable, decentralised energy sources exceeds the local load requirements.

The operators of the distribution grids are thus producing new standards in order to regulate the grid-connection of renewable energy systems. One of the main changes that are being enforced is the ability to supply pre-determined amounts of reactive power to the grid, in order to reduce the voltage rise in case of overproduction. Unfortunately, several topologies, especially the ones that employ MOSFETs to increase the efficiency [27–29], were designed with unity power factor operation in mind, and they cannot supply reactive power unless proper modifications are introduced, usually with a consequent decrease of efficiency.

In addition to the reactive power requirements, two major changes are now steering PV inverter research: the increasing availability of wide-bandgap power devices and the increasing interest in thin-film panels.

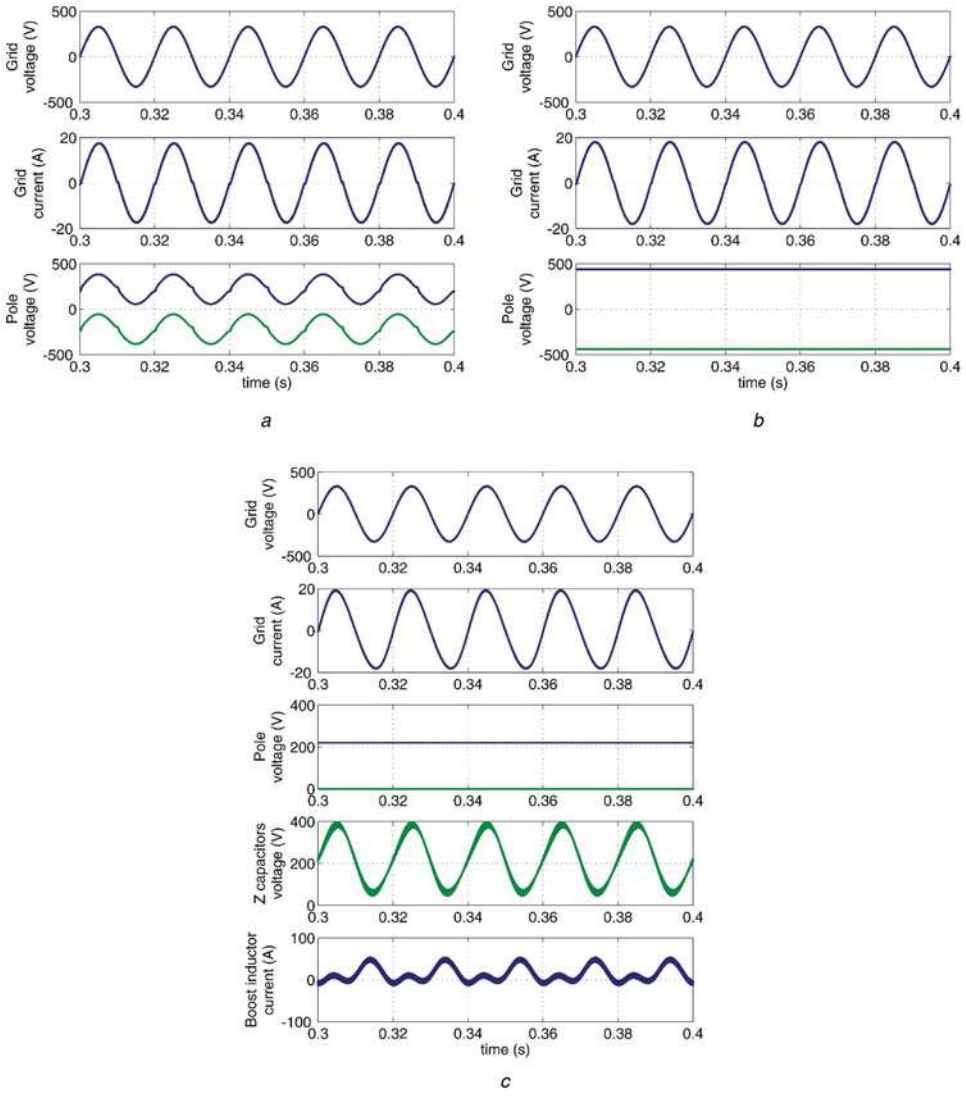

Fig. 20 *Simulation results*

a HERIC topology
b NPC topology
c Topology [53]

The main feature of wide-bandgap power devices, such as SiC and GaN, is the ability to switch at very high frequency, mainly due to unipolar current conduction (i.e. no IGBT-like current tailing) and reduced parasitic capacitances. The use of wide-bandgap FETs presents some major advantages: different from Si devices, the performances of the body diode (or equivalent body diode behaviour, for GaN devices) are sufficient to withstand hard switching operation. This, in conjunction with the very low switching losses, is likely to reduce the interest in architectures with optimised freewheeling paths in the future. The almost resistive behaviour of the FET channel will improve the weighted efficiency (such as 'European' or California Energy (CEC) efficiency) of the converters, due to the reduced losses at partial load.

On the other hand, the ongoing developments of thin-film panels and their increasing diffusion might soon reduce the adoption of sinusoidal pole voltages topologies, unless specific PWM strategies are adopted to reduce the grid frequency leakage current. As a consequence, constant pole voltage topologies will probably be reconsidered for mass commercialisation, despite the disadvantage of needing an increased DC-link voltage. It must be said that this will not constitute a problem anymore, because the new SiC devices have been heavily optimised for 1200 V breakdown ratings, and even half-bridge topologies could be interesting due to their simplicity and reduced the component count. Also, the use of new PV panels with an increased voltage maximum power point (MPP) could push towards increasing the DC-link voltage. In fact, considering a fixed rated power of the inverter, the number of parallel strings could be reduced with the aim of obtaining higher string voltages.

The development and commercialisation of thin-film PV panels or multijunction PV cells will pose more stringent constraints on inverter topologies. In particular, the voltages applied to the PV panels with respect to ground will need to be carefully considered during the design of a PV plant. Although their diffusion is limited at the moment, in the future doubly grounded topologies might become the only feasible way to realise transformerless PV systems.

10 Conclusion

This paper has covered the state of the art in transformerless PV converters. A classification of the topologies based on the voltage waveforms measured between the PV field terminals and the ground was carried out in order to match the features of the power converters with the existing panels technologies.

Several different topologies have been considered and compared in terms of ground leakage current, compatibility with the newest electrical regulations (i.e. the ability to generate reactive power) and efficiency. Since the solutions differ greatly in terms of commutation characteristics and conduction paths, the comparison has been performed on qualitative terms, based on the number of series devices during the commutation states and on the commutation voltages (Table 1).

Finally, the influence of the new trends in power semiconductors and PV technologies as well as of the new power grid regulations on converter design was considered. In particular, the emergence of thin-film PV panels and wide-bandgap devices will probably steer the research in new directions, modifying the landscape of the most effective and most widespread converter architectures.

11 References

1 Meneses, D., Blaabjerg, F., Garcia, O., *et al.*: 'Review and comparison of step-up transformerless topologies for photovoltaic ac-module application', *IEEE Trans. Power Electron.*, 2013, **28**, (6), pp. 2649–2663

2 Kjaer, S., Pedersen, J., Blaabjerg, F.: 'A review of single-phase grid-connected inverters for photovoltaic modules', *IEEE Trans. Ind. Appl.*, 2005, **41**, (5), pp. 1292–1306

3 Barater, D., Buticchi, G., Crinto, A., *et al.*: 'A new proposal for ground leakage current reduction in transformerless grid-connected converters for photovoltaic plants'. 35th Annual Conf. of IEEE Industrial Electronics, 2009, IECON'09, 2009, pp. 4531–4536

4 'Reference technical rules for the connection of active and passive users to the LV electrical Utilities', in *CEI 0-21*,: 2012-06 2012

5 'Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid', in *VDE V 0126-1-1*,: 2006-02 2006

6 Hacke, P., Terwilliger, K., Smith, R., *et al.*: 'System voltage potential-induced degradation mechanisms in pv modules and methods for test'. 37th IEEE Photovoltaic Specialists Conf. (PVSC), 2011, 2011, pp. 000 814–000 820

7 Hacke, P., Smith, R., Terwilliger, K., *et al.*: 'Testing and analysis for lifetime prediction of crystalline silicon pv modules undergoing degradation by system voltage stress', *IEEE J. Photovolt.*, 2013, **3**, (1), pp. 246–253

8 Kindyni, N., Georghiou, G.: 'Application of an analytical model based on transistor concepts for the characterization of potential-induced degradation in crystalline silicon photovoltaics'. IEEE 39th Photovoltaic Specialists Conf. (PVSC), 2013, June 2013, pp. 1559–1565

9 Hacke, P., Terwilliger, K., Smith, R., *et al.*: 'System voltage potential-induced degradation mechanisms in pv modules and methods for test'. 37th IEEE Photovoltaic Specialists Conf. (PVSC), 2011, June 2011, pp. 000 814–000 820

10 Hacke, P., Smith, R., Terwilliger, K., *et al.*: 'Acceleration factor determination for potential-induced degradation in crystalline silicon pv modules'. IEEE Int. Reliability Physics Symp. (IRPS), 2013, April 2013, pp. 4B.1.1–4B.1.5

11 Osterwald, C., McMahon, T., del Cueto, J.: 'Electrochemical corrosion of sno2:f transparent conducting layers in thin-film photovoltaic modules', *Sol. Energy Mater. Sol. Cells*, 2003, **79**, (1), pp. 21–33, Available at: http://www.sciencedirect.com/science/article/pii/S092702480200363X

12 Wen, M., Ricou, P.: 'Evaluating tco long-term performance by electrochemical corrosion test and residual film stress analysis'. 38th IEEE Photovoltaic Specialists Conf. (PVSC), 2012, 2012, pp. 001 332–001 335

13 Nghiem, B., Bellac, D.L.: 'Transparent conducting oxides superstrate for thin film solar cells: an industrial prospective', *Int. J. Nanotechnol.*, 2009, **6**, (9), pp. 870–878

14 Jansen, K., Delahoy, A.: 'A laboratory technique for the evaluation of electrochemical transparent conductive oxide delamination from glass substrates', *Thin Solid Films*, 2003, **423**, (2), pp. 153–160, Available at: http://www.sciencedirect.com/science/article/pii/S0040609002010209

15 Dong, D., Luo, F., Boroyevich, D., *et al.*: 'Leakage current reduction in a single-phase bidirectional ac-dc full-bridge inverter', *IEEE Trans. Power Electron.*, 2012, **27**, (10), pp. 4281–4291

16 Barater, D., Buticchi, G., Lorenzani, E., *et al.*: 'Active common-mode filter for ground leakage current reduction in grid connected pv converters operating with arbitrary power factor', *IEEE Trans. Ind. Electron.*, 2014, **61**, (8), pp. 3940–3950

17 Busatto, G., Persiano, G., Iannuzzo, F.: 'Experimental and numerical investigation on mosfet's failure during reverse recovery of its internal diode', *IEEE Trans. Electron. Devices*, 1999, **46**, (6), pp. 1268–1273

18 Buticchi, G., Barater, D., Lorenzani, E., *et al.*: 'Digital control of actual grid-connected converters for ground leakage current reduction in pv transformerless systems', *IEEE Trans. Ind. Inf.*, 2012, **8**, (3), pp. 563–572

19 Kerekes, T., Teodorescu, R., Borup, U.: 'Transformerless photovoltaic inverters connected to the grid'. Twenty Second Annual IEEE Applied Power Electronics Conf., APEC 2007, 2007, pp. 1733–1737

20 Ji, B., Wang, J., Zhao, J.: 'High-efficiency single-phase transformerless pv h6 inverter with hybrid modulation method', *IEEE Trans. Ind. Electron.*, 2013, **60**, (5), pp. 2104–2115

21 Wang, J., Ji, B., Zhao, J., *et al.*: 'From h4, h5 to h6 – standardization of full-bridge single phase photovoltaic inverter topologies without ground leakage current issue'. IEEE Energy Conversion Congress and Exposition (ECCE), 2012, 2012, pp. 2419–2425

22 Huafeng, X., Shaojun, X., Yang, C., *et al.*: 'An optimized transformerless photovoltaic grid-connected inverter', *IEEE Trans. Ind. Electron.*, 2011, **58**, (5), pp. 1887–1895

23 Kerekes, T., Teodorescu, R., Rodriguez, P., *et al.*: 'A new high-efficiency single-phase transformerless PV inverter topology', *IEEE Trans. Ind. Electron.*, 2011, **58**, (1), pp. 184–191

24 Gonzalez, R., Lopez, J., Sanchis, P., *et al.*: 'Transformerless inverter for single-phase photovoltaic systems', *IEEE Trans. Power Electron.*, 2007, **22**, (2), pp. 693–697

25 Barater, D., Buticchi, G., Crinto, A., *et al.*: 'Unipolar pwm strategy for transformerless pv grid-connected converters', *IEEE Trans. Energy Convers.*, 2012, **27**, (4), pp. 835–843

26 Buticchi, G., Lorenzani, E., Franceschini, G.: 'A five-level single-phase grid-connected converter for renewable distributed systems', *IEEE Trans. Ind. Electron.*, 2013, **60**, (3), pp. 906–918

27 Weissenhorn, T., Kloos, D., Winter, A., *et al.*: 'Step-down-converter, dc-ac-converter assembly and method for operating the same'. European Patent EP 2 421 135, August 2011

28 Yu, W., Lai, J.-S., Qian, H., *et al.*: 'High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated AC-module applications', *IEEE Trans. Power Electron.*, 2011, **26**, (4), pp. 1253–1260

29 Gu, B., Dominic, J., Lai, J., *et al.*: 'High reliability and efficiency single-phase transformerless inverter for grid-connected photovoltaic systems', *IEEE Trans. Power Electron.*, 2013, **57**, (9), pp. 3118–3128

30 Araujo, S.V., Zacharias, P., Mallwitz, R.: 'Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems', *IEEE Trans. Ind. Electron.*, 2010, **28**, (5), pp. 2235–2245

31 Nabae, A., Takahashi, I., Akagi, H.: 'A new neutral-point-clamped pwm inverter', *IEEE Trans. Ind. Appl.*, 1981, **IA-17**, (5), pp. 518–523

32 Lopez, O., Teodorescu, R., Doval-Gandoy, J.: 'Multilevel transformerless topologies for single-phase grid-connected converters'. 32nd Annual Conf. on IEEE Industrial Electronics, IECON 2006, 2006, pp. 5191–5196

33 Saridakis, S., Koutroulis, E., Blaabjerg, F.: 'Optimal design of modern transformerless pv inverter topologies', *IEEE Trans. Energy Convers.*, 2013, **28**, (2), pp. 394–404
34 Floricau, D., Floricau, E., Dumitrescu, M.: 'Natural doubling of the apparent switching frequency using three-level anpc converter'. Int. School on Nonsinusoidal Currents and Compensation, 2008, ISNCC 2008, June 2008, pp. 1–6
35 Knaup, P.: 'Inverter'. International Patent WO 2007/048 420 A1, May 2007
36 Hasanzadeh, A., Edrington, C., Leonard, J.: 'Reduced switch npc-based transformerless pv inverter by developed switching pattern'. Proc. IEEE APEC 2012, Orlando, FL, February 2012, pp. 359–363
37 Frisch, M., Temesi, E.: 'Inverter topologies usable with reactive power'. US Patent US20 110 013 438 A1, January 2011
38 Wang, Y., Li, R.: 'Novel high-efficiency three-level stacked-neutral-point-clamped grid-tied inverter', *IEEE Trans. Ind. Electron.*, 2013, **60**, (9), pp. 3766–3774
39 Ma, L., Jin, X., Kerekes, T., *et al.*: 'The pwm strategies of grid-connected distributed generation active npc inverters'. Proc. IEEE ECCE 2009, San Jose, CA, September 2009, pp. 920–927
40 Li, J., Liu, J., Boroyevich, D., *et al.*: 'Three-level active neutral-point-clamped zero-current-transition converter for sustainable energy systems', *IEEE Trans. Power Electron.*, 2011, **26**, (12), pp. 3680–3693
41 Floricau, D., Gateau, G., Dumitrescu, M., *et al.*: 'A new stacked npc converter: 3l-topology and control'. European Conf. on Power Electronics and Applications, 2007, September 2007, pp. 1–10
42 Floricau, D., Gateau, G., Leredde, A.: 'New active stacked npc multilevel converter: Operation and features', *IEEE Trans. Ind. Electron.*, 2010, **57**, (7), pp. 2272–2278
43 Ghoddami, H., Yazdani, A.: 'A bipolar two-stage photovoltaic system based on three-level neutral-point clamped converter'. Proc. IEEE PES 2012, San Diego, CA, July 2012, pp. 1–8
44 Petrella, R., Buonocunto, N., Revelant, A., *et al.*: 'Equalization of dc bus voltage in three-level npc half-bridge inverters for pv applications by even harmonics injection or fundamental phase modulation'. Proc. IEEE ECCE 2011, Phoenix, AZ, September 2011, pp. 3427–3434
45 Ott, S., Roasto, I., Vinnikov, D.: 'Neutral point clamped quasi-impedance-source inverter'. Proc. CPE 2011, Tallinn, Estonia, June 2011, pp. 348–353
46 Xiao, H., Xie, S.: 'Transformerless split-inductor neutral point clamped three-level pv grid-connected inverter', *IEEE Trans. Power Electron.*, 2012, **27**, (4), pp. 1799–1808
47 Zhang, L., Sun, K., Feng, L., *et al.*: 'A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters', *IEEE Trans. Power Electron.*, 2013, **28**, (2), pp. 730–739
48 Vazquez, N., Almazan, J., Alvarez, J., *et al.*: 'Analysis and experimental study of the buck, boost and buck-boost inverters'. 30th Annual IEEE Power Electronics Specialists Conf., 1999, 1999, vol. 2, pp. 801–806
49 Gu, Y., Li, W., Zhao, Y., *et al.*: 'Transformerless inverter with virtual dc bus concept for cost-effective grid-connected pv power systems', *IEEE Trans. Power Electron.*, 2013, **28**, (2), pp. 793–805
50 Karschny, D.: 'Wechselrichter'. German Patent DE19 642 522C1, April 1998
51 Schekulin, D.: 'Transformatorlose wechselrichter-schaltungsanordnung'. German Patent DE19 732 218C1, March 1999
52 Cao, D., Jiang, S., Yu, X., *et al.*: 'Low-cost semi-z-source inverter for single-phase photovoltaic systems', *IEEE Trans. Power Electron.*, 2011, **26**, (12), pp. 3514–3523
53 Huang, L., Zhang, M., Hang, L., *et al.*: 'A family of three-switch three-state single-phase z -source inverters', *IEEE Trans. Power Electron.*, 2013, **28**, (5), pp. 2317–2329