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On the VCO/Frequency Divider Interface in Cryogenic CMOS PLL for Quantum Computing Applications

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Abstract: The availability of quantum microprocessors is mandatory, to efficiently run those quantum algorithms promising a radical leap forward in computation capability. Silicon-based nanostructured qubits appear today as a very interesting approach, because of their higher information density, longer coherence times, fast operation gates, and compatibility with the actual CMOS technology. In particular, thanks to their phase noise properties, the actual CMOS RFIC Phase-Locked Loops (PLL) and Phase-Locked Oscillators (PLO) are interesting circuits to synthesize control signals for spintronic qubits. In a quantum microprocessor, these circuits should operate close to the qubits, that is, at cryogenic temperatures. The lack of commercial cryogenic Design Kits (DK) may make the interface between the Voltage Controlled Oscillator (VCO) and the Frequency Divider (FD) a serious issue. Nevertheless, currently this issue has not been systematically addressed in the literature. The aim of the present paper is to investigate the VCO/FD interface when the temperature drops from room to cryogenic. To this purpose, physical models of electronics passive/active devices and equivalent circuits of VCO and the FD were developed at room and cryogenic temperatures. The modeling activity has led to design guidelines for the VCO/FD interface, useful in the absence of cryogenic DKs.

Keywords: CMOS; PLL; VCO; qubit; design; modeling

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1. Introduction

Since ancient times, humankind has always been in need of computing; computation capability and knowledge progress have always walked arm in arm. In 1948 the discovery of the transistor triggered a revolution, paving the way for the modern microprocessors, which are at the base of the actual computation-based information society [1–3]. The microprocessor, by manipulating a huge amount of bits per second, allowed humans to face and solve problems of amazing difficulty in mathematics, physics, chemistry, and engineering. In the XXI century a new kind of microprocessor appeared, the quantum microprocessor. It manipulates bits but of a very special type: the quantum bit, or qubit. The qubit enjoys the counterintuitive properties of the quantum world, such as superposition and entanglement. For the superposition principle, a qubit can be in a superposition of states. Therefore, contrary to its classical counterpart, a qubit can assume 0 and 1 values at the same time. Generally speaking, the superposition allows for a massive parallelism, as introduced in 1985 by David Deutsch in his landmark paper [4]. Once two qubits interact, they are selectively correlated, becoming a new physical entity, not reducible to the two original single qubits. Two entangled qubits cannot be independently manipulated, even if they are far away. Superposition and entanglement allow for algorithms not pos-

sible on a classical microprocessor, promising a radical leap forward in a variety of different scientific, social, and economic contexts, spanning from finance to security and medical sectors. Nevertheless, in order to be efficient, these quantum algorithms should run on a quantum microprocessor where superposition and entanglement are physically available and not emulated, as it may be on a classical microprocessor. This calls for the fabrication of quantum microprocessors. Silicon-based spintronic qubits appear to be a very attractive alternative to the currently widely used transmon technology. From a technological point of view, they are indeed compatible with the actual CMOS microelectronics. In 1998, Kane already proposed the fabrication of quantum microprocessors by using the CMOS technology [5]. From an engineering point of view, the manipulation of silicon-based qubits requires frequencies that can be synthesized using the actual CMOS Radio Frequency Integrated Circuits (RFIC). Phase-Locked Loop (PLL) and Phase-Locked Oscillator (PLO), typically used for the frequency synthesis, offer phase noise properties that may be useful in the qubit control. When embedded in a quantum microprocessor, the RFIC should be operated at cryogenic temperatures. Currently, this poses challenges because usually the foundries do not deliver Design Kits (DK) at cryogenic temperatures. In particular, this issue may be critical for PLL/PLO, because of the frequency matching required between two of its important building blocks: the Voltage Controlled Oscillator (VCO) and the Frequency Divider. Generally speaking, as one can expect, this matching is temperature dependent, as the PLL/PLO may be prevented from correctly working when the temperature falls to cryogenic values. Nevertheless, this issue has not been systematically addressed in the literature. The aim of the present paper is to investigate the frequency mismatch that may arise between the VCO and the Frequency Divider when the temperature drops from room to cryogenic values. The paper is organized as follows. Section 2 introduces the qubit implementation with special regard for the silicon-based solution. Section 3 addresses the issues of an integrated CMOS PLL/PLO when used to synthesize frequencies for the qubit control. Section 4 is devoted to the modeling of transistors and passive components at both room and cryogenic temperature. Section 5 focuses on the design of the two critical building blocks, VCO and Frequency Divider. In particular, the effects of the temperature on the frequency behavior of these circuits are modeled. Considerations on the models lead to some design guidelines, briefly described in Section 6, for VCO and Frequency Divider useful when the cryogenic DK for the chosen technology is not available. Section 7 closes the paper by drawing some conclusions.

2. Qubit and Silicon Microelectronics

Generally speaking, every microscopic two-state quantum physical system can be exploited as a qubit. Currently, superconductor and trapped ions are the technologies at the heart of the first generation of commercially pre-competitive quantum microprocessors. Semiconductor nanostructures, neutral ions, and photons provide a valid alternative to achieve comparable results in the medium term. In particular, silicon technology, despite a delay in terms of maturity with respect to the two more cutting-edge technologies (superconductors and trapped ions), is definitely in strong competition with them for several reasons.

First, under a solid-state physics point of view, the confinement of electron and nuclear spins in host semiconducting materials represents a versatile platform for the realization of qubit. The electron confinement into a quantum dot is achievable following different approaches, from electrostatically and self-assembled quantum dots to donor spins in solid matrices or a combination of them [6]. Several qubit realizations are presented in the literature where the logical states $|0\rangle$ and $|1\rangle$ are encoded in single-electron spin in a quantum dot, singlet-triplet spin states in double quantum dot, three electrons spin states in triple quantum dot, or an all-electrical realization of quantum dot qubit, where three

electrons are confined in a double quantum dot, called hybrid qubit [7]. Analogous qubit realizations are achieved for the donor scenario [8].

The fabrication of a complete silicon fault-tolerant architecture is an ambitious task rewarded with the possibility of using the well assessed CMOS technology semiconductor manufacturing. Semiconductor nanostructured qubits offer, therefore, the exciting potentiality of paving the way towards the large-scale quantum computation era based on the same silicon chip technology of the current information age.

Moreover, silicon qubits outperform other competitors in terms of quantum information density, i.e., the number of physical qubits per unit area. For silicon qubits this quantity goes from 830 to 10^5 Mqubit/cm^2, which is significantly larger than superconductors and trapped ions qubits, for which it lies in the 10^{-4}–10^{-5} Mqubit/cm^2 range. In addition, the chip area, i.e., the area covered by 2 billion physical qubits, goes from 10–10^2 mm^2 for semiconducting qubits to 10^7–10^{10} mm^2 for superconductors and trapped ions qubits [9].

Semiconductor nanostructured qubits are attractive also for their relatively long coherence times, which allows for the execution of a higher number of quantum gate operations. The silicon crystal, once made free from its 29-isotope, is a relatively noise-free environment for spintronic qubits.

Easy manipulation and fast gate operations are other benefits offered by the qubits on silicon. Regarding the qubit manipulation, for single-electron spin qubits in a quantum dot, the microwave frequency useful for its control, that corresponds to the energy difference between the two spin states, is in the 13–40 GHz frequency range. The frequency grows for the single-electron spin qubits in a donor for which lies in the 30–50 GHz range. These control frequency ranges are very attractive, because in the last two decades, the microelectronics industry for telecom applications demonstrated that such kind of signals can be generated and manipulated by using CMOS RFICs. Therefore, again, the CMOS technology seems to be an interesting option for the fabrication of quantum microprocessor.

In short, on the basis of the previous discussion, one can conclude that silicon-based qubits sound very appealing, because of higher versatility, higher information density, longer coherence times, and compatibility with CMOS technology and RFIC microelectronics.

3. PLL/PLO and Quantum Microprocessors

The typical circuit frequency synthesizer used in CMOS RFIC is the PLL/PLO, the typical building block diagram of which is shown in Figure 1. In a PLL, the Frequency Divider in the feedback loop is programmable, while in a PLO it is not. The PLL/PLO constitutes a feedback loop, the goal of which is to control the frequency generated by the VCO. When locked, the PLL/PLO sets the VCO to oscillate at a frequency N times the reference frequency, where N is the division modulus of the Frequency Divider. Overall, the PLL/PLO therefore works as a frequency multiplier. A very interesting property of the PLL/PLO is the shaping effect of the feedback loop on the phase noise when the PLL/PLO is locked. On the right, Figure 1 shows that close to the carrier, the PLL/PLO phase noise is lower with respect to the free running VCO. The integral phase noise therefore decreases when the PLL/PLO instead of the VCO is used for the frequency synthesis. In telecom applications this property is useful because it helps with keeping low the Bit Error Rate (BER) at the receiver side. Interestingly, this property turns out to be useful also for the control of a qubit. The signal controlling the qubit in a quantum microprocessor should exhibit indeed an integral phase noise as low as possible, because a too large integral phase noise may jeopardize the quantum gate fidelity [10], a sort of BER for the qubit. The PLL/PLO therefore appears to be an interesting candidate radiofrequency source for a quantum microprocessor [10,11]. A survey of the recent literature reveals that, under the

pressure of packing together a large number of qubits, being the estimated goal for the quantum supremacy in the range of tens of millions, the actual envisage solution is moving the classical CMOS circuitry closer to the qubits by levering on the actual microelectronics technology [12–26]. The design of cryogenic CMOS circuitry for a quantum microprocessor is a real multi-faceted activity covering RFIC [12,17,22,24,26], DAC [16,24,26], readout circuits [22,25], and more general aspects related to the microprocessor architecture [15,23,25] and to the cryogenic system, as well. This makes a quantum microprocessor closer to a mixed-signal than a pure digital circuit. The CMOS circuit design depends, moreover, also on the qubit implementation (transmonic, spintronic, single, double, triplet) [13,14].

Therefore, an integrated CMOS PLL appears to be a very interesting electronic cell for the design of the measure-and-control layer of a quantum microprocessor. It is worth noting that classical microprocessors also currently embed several PLLs.

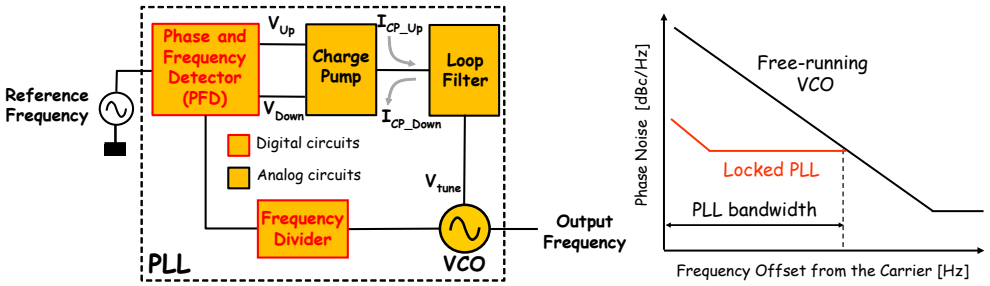

Figure 1. Typical building block diagram of a PLL (on the **left**) and phase noise shaping under locked conditions (on the **right**).

The interface between the VCO and the digital Frequency Divider is a very challenging issue in the design of a PLL/PLO. The Frequency Divider exhibits indeed an optimal frequency f_{OPT}, at which the required level of the input signal is minimum, making easier the design of the VCO. The larger the offset from f_{OPT} is, the higher the amplitude of the VCO signal should be. If the frequency offset is too large, the PLL/PLO cannot achieve the locking condition. In this case, the VCO runs free, and its frequency goes out of control. As in a quantum microprocessor, the integrated CMOS PLL/PLO is placed close to the qubits, and it should operate at cryogenic temperature. In reality, this involves a practical issue for the microelectronics designer: the lack of commercial Design Kits (DK) available at cryogenic temperatures [11]. Currently, the silicon foundries usually release DK in the −50 °C to +80 °C temperature range. The actual praxis is therefore designing the RFICs at room temperature by using a standard process and then cooling down the prototypes to cryogenic temperatures for its characterization [27,28]. As the cooling down from 300 K to a cryogenic temperature may induce a frequency mismatch between the VCO and the Frequency Divider, the RFICs are designed with generous tolerances and tuning capabilities, entailing a sub-optimized design. In the worst cases, these tolerances may not be enough to prevent the PLL to achieve the locking condition. In this frame, the investigation of the critical interface between the VCO and the Frequency Divider when the temperature changes from room to cryogenic is of large interest. Nevertheless, in spite of that, this issue has not been systematically investigated in the literature. The present paper intends to investigate the frequency mismatch between the VCO and the Frequency Divider that may arise when the temperature drops from room to cryogenic values.

4. Cryogenic Models

In the present work, the first step was to address the cryogenic modeling of the devices to be used for the design of the VCO and of the Frequency Divider. A cryogenic temperature of 4 K is assumed, because of the recent demonstrations of silicon-based qubits able to operate at temperatures higher than 1 K instead of the usual sub −1 K range [29,30]. A higher operating temperature allows for a higher cooling power for the dilution fridge. This turns into a greater power dissipation headroom available for the microelectronics engineer. The estimated power budget roughly rises from 1 mW to 1 W, when the operating temperature increases from 100 mK to 4 K.

Several compact models are reported in the literature for MOSFET operating at cryogenic temperature: MOS11, PSP, and BSIM [31–33]. In these works, the models were improved by adding additional Verilog-A software modules. The present work adopts the MOS3 compact model due to its simplicity and allowing the modeling of second order effects like the short-channel effect and mobility degradation without additional Verilog-A code. This makes the models compatible with the large set of SPICE-based circuit simulators. In particular, cryogenic MOS3 models were extracted for n-channel and p-channel MOSFET with gate length of 40 nm and gate widths of 1200 nm and 120 nm from the data reported in [32]. During the design, these two different sized MOSFET form a small set of transistors, which can be connected to obtain equivalent transistors of different aspect ratio. It is worth noticing that the modeling procedure takes advantage of the absence of kink effect in the transistor output characteristics, as it is expected for gate length shorter than 0.7 μm [31,32].

One of the most important parameters for the MOS3 model is the threshold voltage, VTO. Its value was extracted from the experimental transcharacteristics reported in [32]. The obtained results are reported in Table 1. Another important model parameter is PHI, which is the threshold surface potential $\phi_S{}^T$. At room temperature is provide by the usual expression:

$$\phi_s^T = 2V_{TH} \ln\left(\frac{N_A}{n_i}\right) \quad (1)$$

where V_{TH} is the thermal voltage, n_i the intrinsic carrier concentration, and N_A the substrate doping concentration. When the temperature goes down to cryogenic, $\phi_S{}^T$ changes by $\Delta\phi_F$ in the case of an n-channel MOSFET [34]:

$$\phi_s^T = 2V_{TH} \ln\left(\frac{N_A}{n_i}\right) - \Delta\phi_F \quad (2)$$

where

$$\Delta\phi_F = V_{TH} \ln\left(\frac{1+\sqrt{1+\frac{4\alpha N_A}{n_i}}}{2}\right) \quad (3)$$

where $\alpha = g_A \exp[(E_A - E_i)kT]$, with g_A ground-state degeneracy factor, E_A the energy level of the acceptor impurity and E_i the intrinsic Fermi energy level. The quantity α accounts for the dopant incomplete ionization; in the case of complete ionization $\alpha = 0$ and thus $\Delta\phi_F = 0$. The values of PHI computed from these equations are reported in Table 1. Moving from the work of Beckers et al. [34], it is possible to demonstrate that the threshold voltage V_{TN} of an n-channel MOSFET with n-type doped poly-silicon gate is given by:

$$V_{TN} = V_{TH} \ln \frac{N_A}{N_C} + \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C'_{ox}} \sqrt{2V_{TH} \ln \frac{N_A}{n_i} - \Delta\phi_F} \quad (4)$$

where N_C is the effective state concentration in the conduction band, ε_{Si} the silicon dielectric permittivity, and C'_{ox} the gate capacitance per unit area.

By using an oxide thickness of 1.7 nm reported in [32], assuming a dielectric permittivity equal to the silicon dioxide, default for the MOS3 model, and a substrate doping of few 10^{18} cm^{-3}, typical for deep sub-micron CMOS technologies, the previous equation gives V_{TN} = 0.53 V at room temperature and V_{TN} = 0.61 V at cryogenic temperature, in good agreement with the range of the extracted values for VTO. Because of the field ionization occurring under the Si/SiO_2 interface [34–36], the N_A was kept equal to its room temperature value. The thickness oxide model parameter TOX was set equal to 1.7 nm.

The transconductance coefficient KP parameter, the ETA parameter for the DIBL effect and the THETA parameter for the mobility degradation were first extracted by following basic extraction techniques described in [37] and [38]. Next, parameters KP, ETA and THETA were used as fitting parameters in order to obtain the same behavior of the measured DC characteristics, together with the source and drain resistance parameters RS and RD, respectively. The values obtained for KP, ETA and THETA are reported in Table 1. The obtained RS and RD values of 10 Ω were kept common for all the transistors. A gate resistance parameter RG of 15 Ω was adopted from [39].

To complete the models, gate resistance and parasitic capacitances have to be added. For the model parameters CBD, CBS, CGSO and CGDO, describing the parasitic capacitances per unit channel width, typical values for a 45 nm technology [38,40,41] were assumed. In particular, for the substrate related capacitances C_{BD} and C_{BS}, it was set CBD = CBS = 0.45 fF/μm (CBD = CBS = 0.6 fF/μm) for an n-channel (p-channel) MOSFET at room temperature. For the overlap capacitances C_{GSO} and C_{GDO}, it was set CGSO = CGDO = 0.5 fF/μm. When the temperature decreases from room to cryogenic values, the drain-substrate and source-substrate parasitic capacitances C_{BD} and C_{BS} drop by a factor of ten, because these parasitic capacitances are associated to the space charge region of a reversed biased on junction [42]. In agreement, the cryogenic values of the model parameter CBD and CBS are ten times smaller than the corresponding room temperature values. On the other hand, the overlap gate-source and gate-drain capacitances C_{GSO} and C_{GDO} are temperature independent.

The flicker noise model parameters used for KF and AF for 40 nm technology were from [43]. The value of AF remains nearly one over the temperature range from room temperature down to cryogenic temperature; the value of KF is temperature independent for n-channel MOSFET [44–46]. The values for AF and KF used are also listed in Table 1, where the parameters for the PMOS transistor are also reported.

Table 1. Parameters of the MOS3 models for NMOS and PMOS transistors at 4 K and 300 K.

Parameter	Unit	NMOS Large Size		PMOS Large Size		NMOS Small Size		PMOS Small Size	
		Temperature [K]		Temperature [K]		Temperature [K]		Temperature [K]	
		300	4	300	4	300	4	300	4
PHI	[V]	0.9579	1.156	0.9579	1.156	0.9579	1.156	0.9579	1.156
VTO	[V]	0.55	0.65	−0.55	−0.71	0.5	0.6	−0.5	−0.63
KP	[μA/V²]	200	300	81	131	200	300	81	131
ETA	[–]	0.16×10^{-3}		0.23×10^{-3}		0.21×10^{-3}		0.23×10^{-3}	
THETA	[V^{-1}]	1.923		1.64		1.45		0.98	
CBD	[F]	5.4×10^{-16}	5.4×10^{-17}	6×10^{-16}	6×10^{-17}	5.4×10^{-17}	5.4×10^{-18}	6×10^{-17}	6×10^{-18}

CBS	[F]	5.4×10^{-16}	5.4×10^{-17}	6×10^{-16}	6×10^{-17}	5.4×10^{-17}	5.4×10^{-18}	6×10^{-17}	6×10^{-18}
CGSO	[F/m]	5×10^{-10}		5×10^{-10}		5×10^{-11}		5×10^{-11}	
CGDO	[F/m]	5×10^{-10}		5×10^{-10}		5×10^{-11}		5×10^{-11}	
KF	[FV²]	3×10^{-24}		5.5×10^{-24}	5.5×10^{-23}	3×10^{-24}		5.5×10^{-24}	5.5×10^{-23}

The extracted MOS3 models are able to reproduce the output characteristics reported in [32] pretty well, both at room temperature and at 4 K. In particular, Figure 2 addresses the large-size NMOS and the small-size PMOS. The absolute error between the experimental and the MOS3 drain currents is about 3.2% (9.5%) for the large-size NMOS transistor at 300 K (4 K) and about 5% (14%) for the small-size PMOS transistor at 300 K (4 K). A similar good agreement was also obtained for the other transistors.

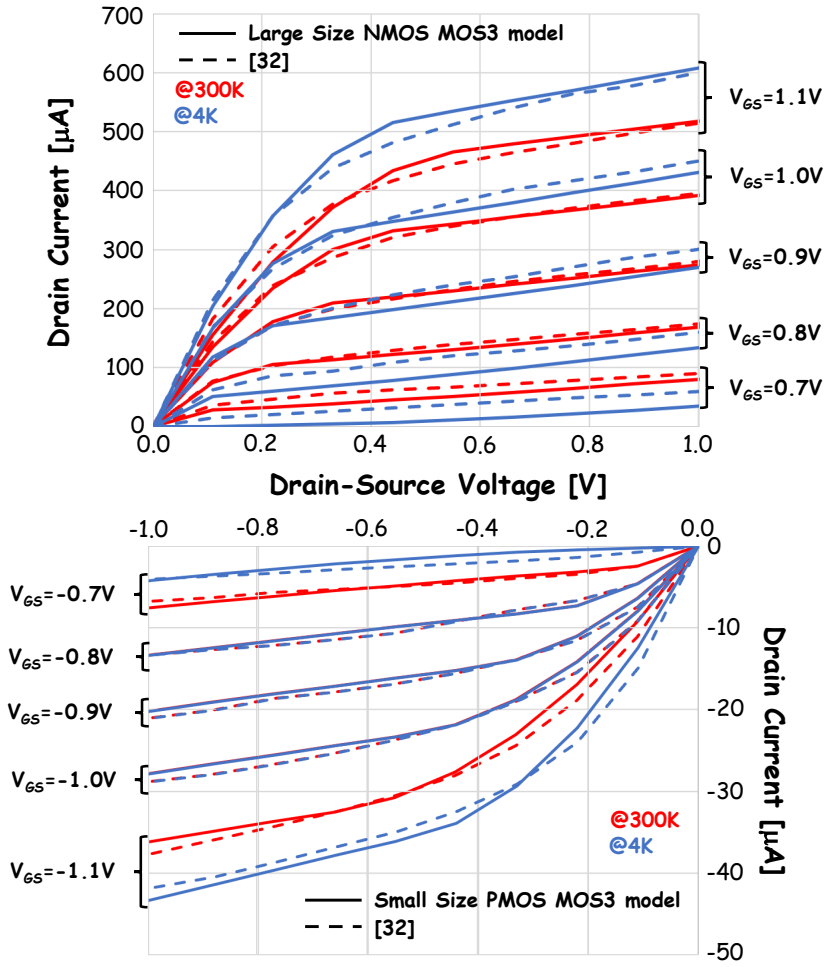

Figure 2. Output characteristics of the large-size NMOS (upper) and the small-size PMOS (lower) transistors. Dashed lines: from [32], solid lines from MOS3 model. Red curves: 300 K, blue curves: 4 K.

Poly-Si resistors and Metal-Oxide-Metal (MOM) capacitors maintain their values at deep-cryogenic temperatures, while the inductor exhibits a reduction of the inductance of approximately 5% and an improvement of the quality factor [47,48]. Therefore, only the inductor needs cryogenic modeling. In the present work, it was assumed a simplified compact model constituted by an inductor in series with a resistor, accounting for the metal losses and skin effect. The substrate losses were modeled by placing a resistor in parallel to the previous RL circuit. As an effect of reducing the temperature down from room to

cryogenic, the series resistance drops by about 40%, while the parallel resistance increases by three orders of magnitude.

5. VCO and Frequency Divider

The VCO and Frequency divider were first designed at 300 K and then simulated at 4 K, in order to investigate the effect of the temperature decrease on the critical interface between the VCO and the Frequency divider. Following the considerations carried out in the Introduction, VCO and Frequency divider were designed to operate around 15 GHz.

5.1. Voltage Controlled Oscillator: Design and Modeling

Figure 3 depicts the VCO schematic adopted in the present work. It is a differential oscillator, whose core is the cross-coupled pair of n-channel transistors M_1 and M_2 providing the energy required to maintain the oscillation. The inductors and the capacitors C are the resonator, which fix the oscillation frequency f_{OSC}. The capacitor C is designed by using MOM capacitors or similar, because their capacitance does not change with the temperature [48]. This frequency is tunable, because of the varactors, implemented by using capacitor connected p-channel MOSFETs. The tuning voltage V_{tune} is applied on the gate of these transistors. The resistors R_p and R_s in the inductor model account for the losses in the inductors, as previously described.

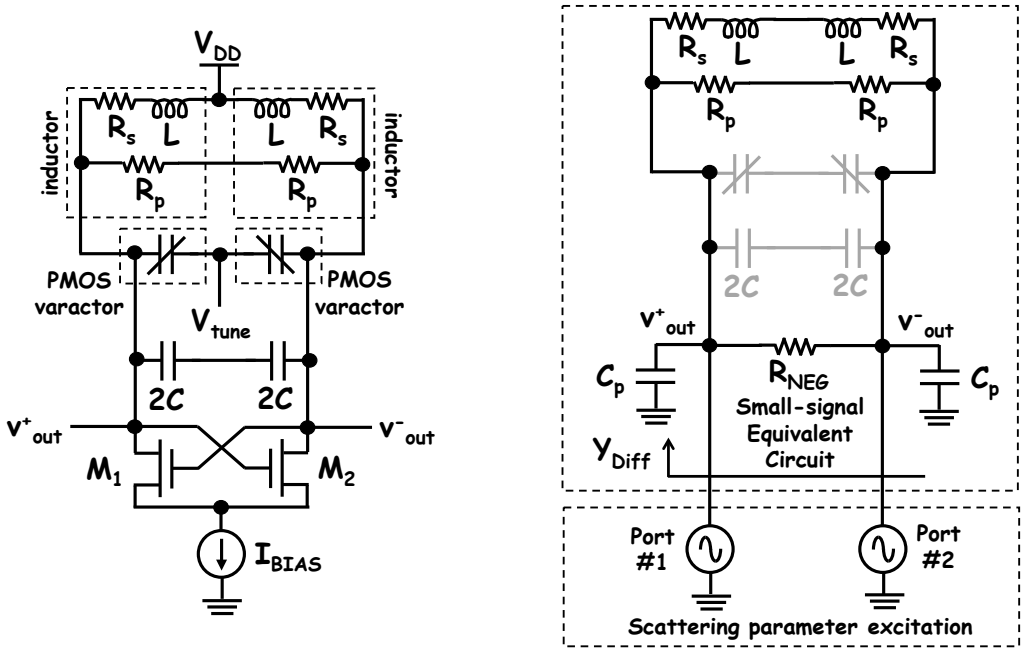

Figure 3. N-type cross-coupled oscillator: schematic (**left**) and small-signal model of the differential admittance Y_{Diff} (**right**).

They set the quality factor Q of the inductor at a given frequency f_0:

$$Q = \frac{2\pi f_0 L R_p}{(R_p + R_s)R_s + (2\pi f_0 L)^2} \quad (5)$$

Figure 3, on the right side, depicts the equivalent small-signal model of the differential admittance Y_{Diff}. In this model the two cross-coupled transistors M_1 and M_2 are equivalent to the differential negative resistance $R_{NEG} = -2/g_{m1(2)}$, where $g_{m1(2)}$ is the transconductance of the transistors M_1 and M_2, whose parasitic capacitances are accounted for by the two capacitors C_p. As shown in the figure, the inductors, but not the fixed capacitors and the varactors, participate to define Y_{Diff}. When the fixed capacitors and the varactors are

also accounted for, one gets the linearized model of the VCO. In this way, Y_{Diff} can be exploited as the core of the oscillator, whose oscillation frequency can be later tuned by adding the fixed capacitors C and the varactors. The linear model on the right side in Figure 3 returns the following mathematical expression:

$$Y_{Diff}(s) = \frac{1}{R_{NEG}} + \frac{1}{2R_p} + \frac{1}{2(R_s + sL)} + \frac{sC_p}{2} \tag{6}$$

where s is the Laplace complex variable. By putting $s = j\omega = j2\pi f$ and after some algebraic manipulations, one gets the dependence of Y_{Diff} on the frequency:

$$Y_{Diff}(j\omega) = -\frac{g_{m1(2)}}{2} + \frac{1}{2R_p} + \frac{R_s}{2(R_s^2 + \omega^2 L^2)} + j\omega\left[\frac{C_p}{2} - \frac{L}{2(R_s^2 + \omega^2 L^2)}\right] \tag{7}$$

Oscillations can start up if Y_{Diff} exhibits a negative real part, that is:

$$g_{m1(2)} > \frac{1}{R_p} + \frac{R_s}{R_s^2 + \omega^2 L^2} \tag{8}$$

Under these conditions, Y_{Diff} injects into the resonator more energy than that dissipated by R_p and R_s. Of course, the higher the injected energy, the higher the oscillation of the differential output signal $v_{out} = v^+_{out} - v^-_{out}$. In particular, for a given v_{out}, the value of the bias current I_{BIAS} can be estimated from the inductor model by describing the transistor during the oscillator operation as an ideal switch [49]:

$$I_{BIAS} = \frac{\pi v_{out}}{8R_p \dfrac{R_s^2 + \omega^2 L^2}{(R_p + R_s)R_s + \omega^2 L^2}} \tag{9}$$

On the other hand, the imaginary part of Y_{Diff} can be described, due to the series of two inductors whose inductance L_{eq} is expressed by the following mathematical expression:

$$L_{eq} = \frac{1}{\omega^2\left(C_p - \dfrac{L}{R_s^2 + \omega^2 L^2}\right)} \tag{10}$$

The capacitance of the fixed capacitor C should resonate, at the free running frequency f_0 of the VCO, with these two equivalent inductors. The values for C can be therefore estimated through the usual formula of the LC resonance frequency:

$$C = \frac{1}{(2\pi f_0)^2 L_{eq}} \tag{11}$$

With these equations in mind, the VCO was designed at room temperature by using the scattering parameters. As depicted in the previous Figure 3, the circuit, without the fixed capacitor and the varactors, was excited by a couple of ports, with the same characteristic impedance Z_0, at the frequency of interest f_0. The circuit is therefore described as a two port network through the four scattering parameters S_{11}, S_{12}, S_{21}, and S_{22}. The differential reflection coefficient Γ_{Diff} can be obtained from these parameters through the following formula:

$$\Gamma_{Diff} = \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2} \tag{12}$$

from which Y_{Diff} can be obtained as:

$$Y_{Diff} = \frac{1 - \Gamma_{Diff}}{(1 - \Gamma_{Diff}) 2 Z_0} \quad (13)$$

The inductors used in the present design were set equal to 0.75 nH. Assuming a quality factor of 10 and a f_0 = 15 GHz, Equation (1) gives R_p = 1413 Ω and Rs = 3.53 Ω. By choosing a peak-to-peak differential output voltage of 1 V, I_{BIAS} results to be about 560 μA from Equation (9). The start-up condition, see Equation (8), implies $g_{m1(2)} > 1.4$ mS. By choosing $g_{m1(2)}$ = 3.2 mS, the transistor overdrive is about 0.18 V; the aspect ratio of the transistors M_1 and M_2 results to be about 3.6/0.04. In order to keep the gate length in the range of 1 μm, each transistor was obtained as the parallel of three transistors with an aspect ratio of 1.2/0.04. The supply voltage V_{DD} was set equal to 1V, in order to keep the dissipated power low.

With these values, the scattering parameter simulation gave $Y_{Diff} = -(880 + j6440)$ μS at 15 GHz. The simulated value of the real part of Y_{Diff} is close to the value of −893 μS, provided by Equation (7). The small difference has to be ascribed to the channel modulation effect. The transistor output characteristics in Figure 2 show its presence but, for the sake of simplicity, it was not accounted for in the equivalent small-signal model in Figure 3. The simulated value of the imaginary part of Y_{Diff} results are very close to the value of 6470 μS predicted by Equation (7), by putting the transistor parasitic capacitance C_p = 12.5 fF. At 15 GHz, the imaginary part of Y_{Diff} corresponds to L_{eq} = 0.82 nH, from which Equation (11) gives C = 68.6 fF.

Figure 4 reports, on the left side, the waveforms of the differential carrier v_{out} generated by the oscillator working at 300 K. The start-up phase, during which the small-signal approximation applies, last about 4 nsec. Afterward, the transistor non-linearities make the oscillator enter the steady state regime, where the oscillation frequency is 15 GHz and the peak-to-peak amplitude is close to 1V. In order to get the desired frequency, the value of C was tuned to 69 fF. This tuning is a consequence of the non-linearities excited in the steady state regime.

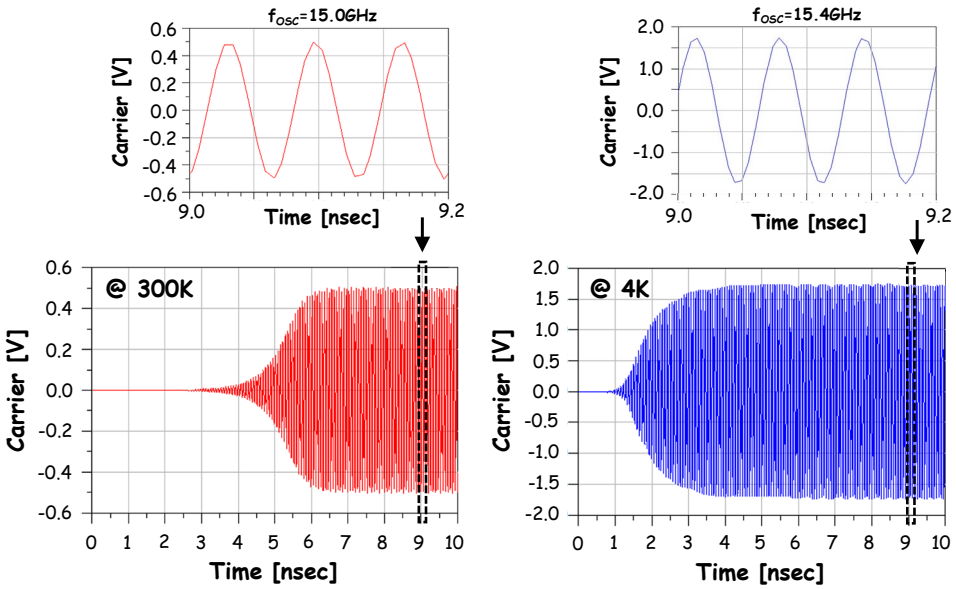

Figure 4. Carrier waveforms at 300 K (**left**) and at 4 K (**right**).

Once the correct behavior of the oscillator at room temperature was observed, the oscillator was simulated at 4 K by using the cryogenic models for transistors and inductors. Concerning the inductors, following what was stated in the previous section, R_p increased

by three orders of magnitude, R_s reduced by about 40%, and L decreased by about 5%. The transistors model was modified in agreement with Table 1. As the tail bias current I_{BIAS} was kept constant, the cryogenic transconductance resulted to be about 3.9 mS and the transistor overdrive weakly decreased to 0.14V. The obtained waveforms are depicted on the right side of Figure 4. The duration of the start-up phase reduced to about 1 nsec and the steady state oscillation differential amplitude increased to about 3.2 V, in agreement with the reduction of the losses in the inductor. The cryogenic values of the inductor model parameters give indeed a quality factor of about three times higher than that at 300 K. A more ideal reactive response of the inductor allows therefore to get oscillation amplitudes higher than the supply voltage. It is worth noticing that Equation (9) predicts a differential output amplitude v_{out} = 3.15 V when the increased value of R_p and the decreased value of R_s at cryogenic temperature are used.

The oscillation frequency increases to about 15.4 GHz, compatible with the 5% reduction in the inductance. The increased quality factor of the inductor leads also to an improvement in the phase noise as depicted in Figure 5. The phase noise spectrum at room temperature exhibits a slope of −20 dB/dec, indicating that is dominated by up-conversion of thermal white noise. When the temperature falls to 4 K, the phase noise magnitude decreases and the slope changes to about −30 dB/dec, a signature that the phase noise at cryogenic temperature is dominated by up-conversion of the flicker noise; at this temperature the white noise up-conversion appears for frequency offset higher than 100 MHz. The phase noise simulations in Figure 5 were carried out by using the Harmonic Balance method. They account for the up-conversion of the low frequency noise only and not for the phase noise floor. It is worth citing here that, for an oscillation frequency of about 13 GHz, quite close the 15 GHz addressed in the present work, a phase noise floor of −145 dBc/Hz was reported for a 40 nm CMOS VCO working at 3.5 K [28].

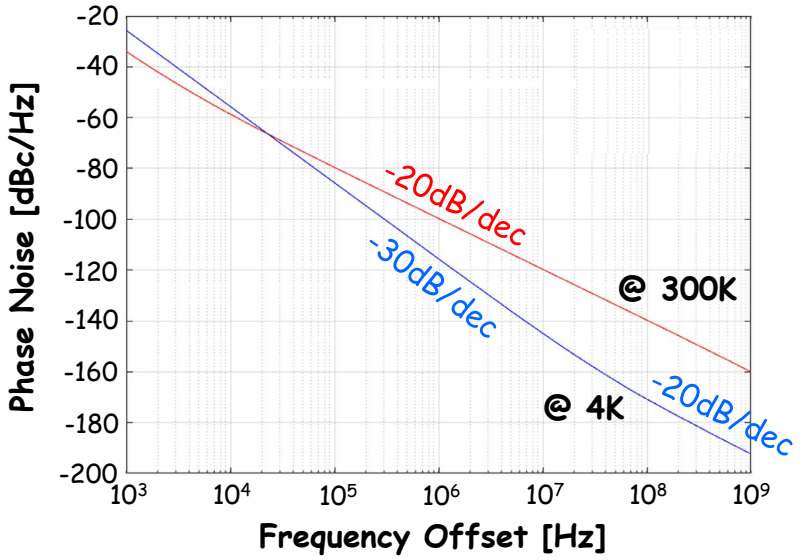

Figure 5. Phase noise at 300 K and 4 K.

The VCO tuning capability was obtained by adding PMOS varactors, as sketched in Figure 3. Figure 6 shows on the left side the capacitance-voltage characteristics of the used varactor. The two characteristics are shifted by about 0.1 V, in agreement with the variation observed in the threshold voltage of the PMOS transistors. With the same procedure used for the NMOS transistors, from the data reported in [32], it was indeed found that the threshold voltage of the PMOS transistors decreases of about 150mV when the temperature drops from room to cryogenics values.

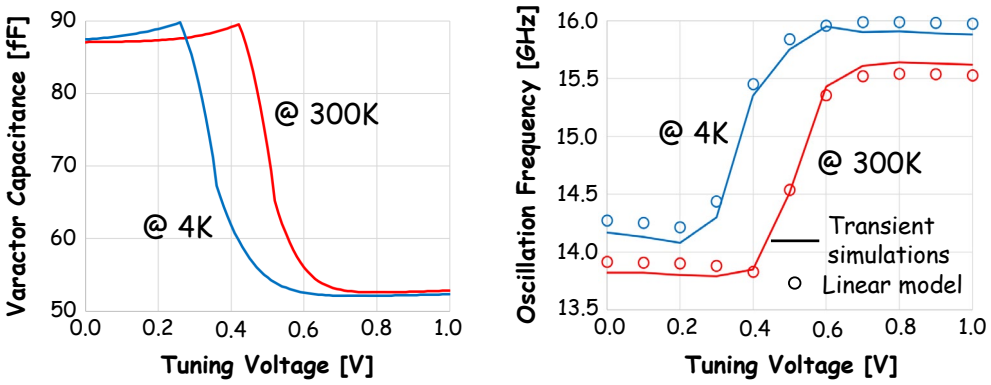

Figure 6. Tuning characteristics of the varactor (on the **left**) and of the VCO (on the **right**).

The previous Equation (7) can be modified into $Y_{Diff,OSC}$, in order to also take into account the fixed capacitances C and the varactors capacitance C_{VAR} as well:

$$Y_{Diff,OSC}(j\omega) = -\frac{g_{m1(2)}}{2} + \frac{1}{2R_p} + \frac{R_s}{2(R_s^2 + \omega^2 L^2)} + j\omega\left[\frac{C_p}{2} + C + \frac{C_{VAR}}{2} - \frac{L}{2(R_s^2 + \omega^2 L^2)}\right] \quad (14)$$

At the oscillation frequency ω_{OSC}, the inductor resonate out with the capacitor and imaginary part of $Y_{Diff,OSC}(j\omega)$ should be zero:

$$\frac{C_p}{2} + C + \frac{C_{VAR}}{2} - \frac{L}{2(R_s^2 + \omega_{OSC}^2 L^2)} = 0 \quad (15)$$

Some algebraic manipulations give the following mathematical expression of ω_{OSC}:

$$\omega_{OSC} = \sqrt{\frac{1}{L(C_p + 2C + C_{VAR})} - \frac{R_s^2}{L^2}} \quad (16)$$

Figure 6 compares, on the right side, the tuning voltage characteristics of the VCO obtained from the non-linear transient simulations (bold curve) with that predicted by the linear small-signal model (open circles) depicted on the right in Figure 3, but this time by accounting for the fixed capacitors and the varactors, as well, and by neglecting the excitation ports #1 and #2, previously used to simulate Y_{Diff}. The value of C was reduced by about 32 fF with respect to the value of 69 fF, in order to account for introduction of the varactors ($2C + C_{VAR} = 2 \times 69$ fF). The obtained curves show a fairly good agreement; a small difference has to be expected, because of the transistor non-linearities excited during the simulations in the time domain. In particular, the differences are more pronounced at cryogenic temperatures, because the oscillation amplitudes are larger. The application of the model shows that the vertical shift in the two characteristics is due to the 5% variation in the inductance induced by the temperature.

5.2. Frequency Divider: Design and Modeling

The front-end electronics of a Frequency Divider usually takes the form of a fixed modulus or of a dual-modulus Frequency Divider. As depicted in Figure 7, in the present work, it was a divide-by-two Frequency Divider obtained by closing in a negative feedback a register, constituted by a cascade of two static Current Mode Logic (CML) latches in a master-slave configuration driven by counter-phase clocks.

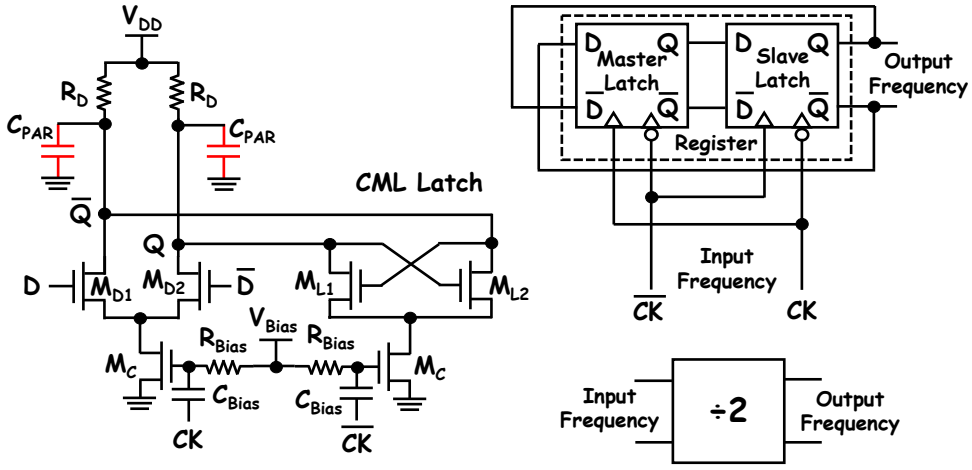

Figure 7. Divide-by-two Frequency Divider.

Because bias voltage V_{DD} is 1V, in order to save bias headroom, the clock differential pair MC was biased by applying a voltage V_{Bias} on their gate, as in [50,51], instead of using the traditional tail current solution, that requires to stack further transistors. The CML is coupled to the VCO with the coupling capacitor C_{Bias}. The R_{Bias} resistors avoid that the AC component of the clock coming from the VCO is drained to ground. R_{Bias} and C_{Bias} work therefore as a bias tee. The latch is constituted by two differential pairs. The driver differential pair M_D works like a differential amplifier; it is activated when the clock is high. The latch is in the transparent phase, because it samples the input differential signals D and Dbar. When the clock goes down, the circuit enters the opaque phase. In this phase the latching differential pair M_L is active, and it stores the signal previously sampled by the M_D pairs. When only the DC component of the clock is applied, because of the negative feedback used for the register, the Frequency Divider behaves like a CML ring oscillator [50,52] exhibiting a self-oscillation frequency f_{SO}. The condition for the self-oscillation is captured by the following equation [52]:

$$g_{m,L}\left(1 + j\frac{W_D}{W_L}\right) = \frac{1}{R_D} + j2\pi f_{SO} C_{PAR} \tag{17}$$

where W_D and W_L are the channel width of the driving and latching transistors, respectively. During the self-oscillation the oscillation amplitudes are usually large enough to excite the non-linearities. The transconductances of the transistors in the circuit are therefore time variant. In Equation (17) $g_{m,L}$ is the DC value of the time variant transconductance of the M_L transistors [52] and C_{PAR} is the parasitic capacitance, highlighted in red in the schematic, at each drain terminal of the M_D transistors. The previous Equation (17) for the self-oscillation implies:

$$g_{m,L} = \frac{1}{R_D} \tag{18}$$

$$f_{SO} = \frac{1}{2\pi} \frac{\frac{W_D}{W_L}}{R_D C_{PAR}} \tag{19}$$

Equation (18) means that the cross-coupled M_L transistors should generate a small-signal equivalent negative resistance able to compensate the losses due to the load resistors R_D. It is also worth presenting the mathematical expression of f_{SO} reported in [53] in the case of a Frequency Divider constituted by n latches, where n is even.

$$f_{SO} = \frac{1}{2\pi} \frac{\sin\frac{\pi}{n}}{\cos\frac{\pi}{n} + \frac{|I_{LSO}|}{|I_{DSO}|}} \frac{1}{R_D C_{PAR}} \quad (20)$$

where $|I_{LSO}|$ and $|I_{DSO}|$ are the modules of the phasors, rotating at $2\pi f_{SO}$ pulsation, of the currents flowing in the M_D and M_L transistors, respectively, under the self-oscillation condition. For n = 2, as in the present case, the previous equation reduces to the following one:

$$f_{SO} = \frac{1}{2\pi} \frac{\frac{|I_{DSO}|}{|I_{LSO}|}}{R_D C_{PAR}} \quad (21)$$

This equation is similar to Equation (19), and it suggests that $|I_{DSO}|/W_D$ should be equal to $|I_{LSO}|/W_L$.

When the clock is applied, the Frequency Divider can be described as an injection locked oscillator. The amplitude of the input clock signal useful to lock the oscillator exhibits its minimum when the clock input frequency f_{CLK} is $2f_{SO}$ [50,54]. In the case of a frequency offset Δf between $2f_{SO}$ and f_{CLK}, the minimum clock amplitude $V_{CLK,min}$, needed to keep the Frequency Divider correctly working, increases; the larger Δf, the higher $V_{CLK,min}$. The plot of $V_{CLK,min}$ versus f_{CLK}, called the Frequency Divider sensitivity curve, exhibits therefore a typical V-shape centered around $2f_{SO}$ [54]. For excessively large Δf, the Frequency Divider enters the cut-off region. The V-shaped sensitivity curve can be reproduced through the following formula [50]:

$$V_{CLK,min} = K_{inj} \frac{\left|\frac{f_{CLK}}{2f_{SO}} - 1\right|}{\sqrt{1 + \left(\frac{f_{CLK}}{2f_{SO}}\right)^2}} \quad (22)$$

where K_{inj} is an injection parameter describing how much the current injected by the clock signal is stronger than the DC current.

In the present work, R_D was kept equal to 1070 Ω, requiring a $g_{m,L}$ higher than 935 μS, corresponding to a minimum bias current of about 20 μA for the M_L transistors. This condition was satisfied, both at 300 K and 4 K, by choosing W_D and W_L equal to 4800 nm, leading to a bias current of about 139 μA and 120 μA at 300 K and 4 K, respectively, for both the M_D and M_L transistors.

Figure 8 compares self-oscillation waveforms and the sensitivity curves for the Frequency Divider simulated at 300 K and 4 K. The self-oscillation frequency shifts from 13.6 GHz to 15.6 GHz when the temperature drops from 300 K to 4 K.

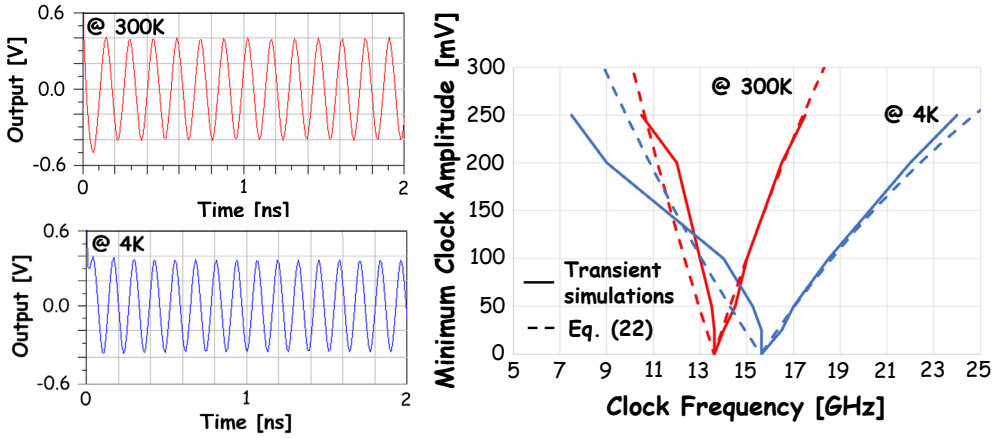

Figure 8. Self-oscillation differential output waveforms (on the **left**) and sensitivity curves (on the **right**) of the Frequency Divider.

Since f_{SO} is inversely proportional to the time constant RC_{PAR}, (see Equations (19)–(21)), to investigate the f_{SO} shift induced by the temperature change it is useful to get a rough estimation of this time constant. Following [53] the parasitic capacitance C_{PAR} was estimated as sum of several contributes. Focusing on the $\bar{Q}$ node in Figure 8, one can write:

$$C_{PAR} = C_{DB,D1} + C_{GD,D1} + C_{DB,L2} + 2\,C_{GD,L1} + 2C_{GD,L2} + C_{OX,L1} + C_{GS,L1} + C_{LOAD} \quad (23)$$

In this expression, $C_{DB,D1}$ and $C_{GD,D1}$ are the drain-bulk and the overlap gate-drain capacitances, respectively, of the M_{D1} transistor, $C_{GD,L1}$ and $C_{GS,L1}$ are the overlap gate-drain and gate-source capacitances of the M_{L1} transistor, $C_{GD,L2}$ is the overlap gate-drain capacitance for the M_{L2} transistor, $C_{OX,L1}$ is the gate oxide capacitance of the M_{L1} transistor and C_{LOAD} is the capacitive load provided by the $\bar{D}$ input node of the following register. In Equation (23), the $C_{GD,L1}$ and $C_{GD,L2}$ capacitances are multiplied by two, because they are excited by a differential signal. Since the input node is constituted by the gate of the M_{D2} transistor of the following register, the C_{LOAD} capacitance can also decomposed in several contributes:

$$C_{LOAD} = C_{OX,D2} + C_{GD,D2} + C_{GS,D2} \quad (24)$$

where $C_{GD,D2}$ and $C_{GS,D2}$ are the overlap gate-drain and gate-source capacitances of the M_{D2} transistor and $C_{OX,D2}$ is the gate oxide capacitance of the M_{D2} transistor. Because the M_D and M_L transistors have been sized at minimum length and with the same channel width, it is reasonable to consider all the overlap parasitic capacitances equal to a given value C_{OV}, $C_{DB,D1}$ and $C_{DB,L2}$ equal to a given value C_{DB}, and $C_{OX,L1}$ and $C_{OX,D2}$ equal to a given value $C_{OX,LD}$. By replacing Equation (24) into Equation (23) one gets:

$$C_{PAR} = 2C_{DB} + 8C_{OV} + 2C_{OX,LD} \quad (25)$$

In Equation (25) only the capacitance C_{OV} can be considered constant during the self-oscillation and independent of temperature. On the other hand, the capacitance C_{DB} depends on time, because it depends on the voltage present at the drain of the transistor, and it depends also on the temperature [42] while the capacitance $C_{OX,LD}$ depends only on the time. For a given temperature, Equation (25) contains therefore two time-dependent capacitive contributes, whose average values have to be estimated. The estimation was carried out by assuming that the transistors behave like a switch during the self-oscillation with a given duty cycle δ.

When the transistor is on, since it is biased in the saturation region, $C_{OX,LD,ON}$ can be estimated to be $2/3\varepsilon_{OX}/t_{OX}$. The drain current I_D flowing in the channel causes now a voltage drop on the load resistor R and therefore the C_{DB} exhibits its high value, $C_{DB,ON}$, because the reverse voltage across the drain-bulk junction is $-V_{DD}+I_DR_D$. Finally, the resistance R_{DS} of the channel can be estimated as V_{DS}/I_D. In this case, the resistance at the drain node R_{ON}, with the transistor on, can be estimated as reported in [52]:

$$R_{ON} = \frac{R_D R_{DS}}{R_{DS} + R_D\left(1 + \frac{W_D}{W_L}\right)} \tag{26}$$

When the transistor is off the $C_{OX,LD,OFF}$ capacitance was assumed to be 10% of $C_{OX,LD,ON}$, because it is constituted only by the substrate space charge region capacitance, being that the channel is absent. The drain voltage can be assumed equal to V_{DD}, because there is no voltage drop on the load resistor, zero being the drain current of the transistor. Therefore, the C_{DB} exhibits its low value, $C_{DB,OFF}$, because the reverse voltage across the drain-bulk junction is $-V_{DD}$. In addition, the resistance of the channel can be assumed infinite, because the drain current of the transistor is zero. The resistance at the drain node $R_{D,OFF}$, with the transistor off, is therefore simply equal to R_D.

On the basis of the previous considerations, the average value of the $C_{OX,LD}$ capacitance can be therefore estimated as:

$$\langle C_{OX,LD}\rangle = \delta\frac{2}{3}\frac{\varepsilon_{OX}}{t_{OX}} \tag{27}$$

and the average value of the C_{DB} capacitance as:

$$\langle C_{DB}\rangle = \delta C_{DB,ON} + (1-\delta)C_{DB,OFF} \tag{28}$$

Similarly, the average value of the resistance at the drain node can be estimated as:

$$\langle R\rangle = \delta R_{ON} + (1-\delta)R_{OFF} \tag{29}$$

In this way the self-oscillation frequency can be estimated by replacing average values of C_{PAR} and R into Equation (19):

$$f_{SO} = \frac{1}{2\pi\langle R\rangle\langle C_{PAR}\rangle} \tag{30}$$

where W_D/W_L was taken equal to one, because the M_D and M_L transistors are sized with the same channel width.

With the parameter values reported in Table 1, the used device size, the simulated drain currents, and a duty cycle of 40%, it is possible to compute <R> = 870 Ω, <C_{PAR}> = 23.5 fF at 300 K and <R> = 873 Ω, <C_{PAR}> = 20.9 fF at 4 K, leading to $2f_{SO}$ = 14.9 GHz at 300 K and $2f_{SO}$ = 16.9 GHz at 4 K. The comparison with the values of $2f_{SO}$ obtained from the simulation (see Figure 8) gives an error of about 10% at 300 K and of about 8% at 4 K. On the other hand, the $2f_{SO}$ shift predicted by Equation (30) results to be the same as obtained from simulations. This agreement suggests that the increase of the self-oscillation frequency is mainly due to the drop of one order of magnitude of the drain-substrate and source-substrate parasitic capacitances C_{BD} and C_{BS} [42]. The average value of the resistance at the drain node changes very little.

Figure 8 also compares the simulated sensitivity curves obtained from transient simulations with the sensitivity curves predicted by Equation (22). A general fairly good agreement was achieved by setting K_{inj} = 1450mV for the sensitivity curve at 300 K and K_{inj} = 800mV for the curve at 4 K. In both the cases, it is possible to remark that the agreement

is better for frequency higher than $2f_{SO}$. A similar asymmetrical agreement between the upper side and the lower side of the sensitivity curve was observed also for the more complex model proposed in [52]. It is worth noticing that the injection factor decreases by about 50% as a consequence of the temperature drop, leading to wider sensitivity curve, as it is possible to observe this in the figure. For a given frequency offset from $2f_{SO}$, the Frequency Divider needs a lower amplitude of the clock signal at cryogenic temperature. At cryogenic temperature, the Frequency Divider seems therefore working better.

6. Design Guidelines

The modeling activity developed in Section 3 for the temperature effect on the frequency behavior of the VCO and of the Frequency Divider suggest some guidelines in the absence of an available Design Kit at cryogenic temperatures for the adopted technology. Concerning the VCO, the carried-out considerations suggest that the VCO can be designed using the available 300 K Design Kit but considering a 5% reduction in the inductance of the tank inductor [47,48] and a variation in the transistor threshold voltage, which can be estimated by using the cryogenic modeling described in Section 2. Similarly, even the Frequency Divider can be designed by using the 300 K available Design Kit, but by taking into account that the bulk-drain capacitances at 4 K are one order of magnitude lower than at 300 K [41]. Usually, the designer can find information about process parameters useful for these evaluations in the Design Rule Manual (DRM) or, at least, by investigating the technical literature.

It is worth noticing here that the investigation of the Process-Voltage-Temperature corners, the Montecarlo analysis, and the Post-Layout-Simulations are necessary steps for the robust design of oscillators [55–57] and Frequency Dividers [58,59]. Nevertheless, in the absence of cryogenic DKs, these investigations can be carried out only at room temperature. The proposed guideline may therefore be considered also as a useful integration to make up for the absence of the statistical data needful for the corner and Montecarlo analysis at cryogenic temperature, also in light of the first experimental evidence on the mismatch in MOS technology at cryogenic temperature reported in [31].

7. Conclusions

The PLL appears attractive for the generation of the microwave signals to control the qubits, because of its interesting phase noise properties. VCO and Frequency Divider interface is very critical for a correct operation of the PLL, because an excessive frequency mismatch between VCO and frequency may prevent the PLL to reach the lock condition. The unavailability of a cryogenic Design Kit is currently a quite common situation, as VCO and Frequency Divider are designed at room temperature, without insights on the frequency mismatch between the VCO and the Frequency Divider may rise up at cryogenic temperatures. The present work addressed by means of simulations the effects of the temperature drop, from 300 K down to 4 K, on the frequency behavior of a differential LC VCO and a static CML Frequency Divider designed in a 40 nm CMOS technology.

After having presented cryogenic models of both active and passive components, VCO and Frequency Divider were simulated and their frequency behavior were investigated. In particular, for the VCO a linear model was adopted while for the Frequency Divider a time-variant model was preferred. The modeling suggests that the frequency variations observed in the VCO, as a consequence of the temperature drop, have been mainly ascribed to changes in the threshold voltage of the transistors and in the inductance of the tank inductor. Concerning the Frequency Divider, the modeling suggests that the variations in the self-oscillation frequency, induced by the temperature drop, are mainly due to the reduction of the bulk-drain parasitic capacitances.

In the absence of an available Design Kit at cryogenic temperatures, the previous conclusions may be a rough useful guideline for the microelectronics designer. They suggest indeed that the VCO can be designed using the available 300 K Design Kit but considering a 5% reduction in the inductance of the tank inductor [47,48] and a variation in the transistor threshold voltage, which can be estimated by using the cryogenic modeling described in Section 3. Even the Frequency Divider can be designed by using the 300 K available Design Kit but by taking into account that the bulk-drain capacitances at 4 K are one order of magnitude lower than at 300 K [42].

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