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The impact of interface and border traps on current-voltage, capacitance-voltage, and split-CV mobility measurements in InGaAs MOSFETs

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In this paper, we present coupled experimental/simulated results about the influence of interface and border traps on the electrical characteristics and split-CV mobility extraction in InGaAs MOSFETs. These results show that border traps limit the maximum drain current under on-state conditions, induce a hysteresis in the quasi-static transfer characteristics, as well as affect CV measurements, inducing an increase in the accumulation capacitance even at high frequencies where trap effects are commonly assumed to be negligible. Hysteresis in the transfer characteristics can be used as a sensitive monitor of border traps, as suggested by a sensitivity analysis where either the energetic or the spatial distribution of border traps are varied. Finally, we show that mobility extraction by means of the split-CV method is affected by appreciable errors related to the spurious contributions of interface and border traps to the total gate charge, ultimately resulting in significant channel mobility underestimation. In very narrow channel devices, channel electron spilling over the InP buffer layer can also contribute to mobility measurement inaccuracy.

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1 Introduction. In recent years, Indium Gallium Arsenide (InGaAs) has been pointed out as a possible candidate for replacement of Silicon (Si) in the n-channel MOSFET devices for CMOS technology extension beyond the 11-nm node. Research on this channel material stems from the ever increasing difficulty faced in the scaling of current Si technology transistors. As Moore's law approaches a critical turning point, technologies like the InGaAs MOSFET offer solutions that could enable further scaling of CMOS technology through the next technological nodes [1].

Although promising, InGaAs MOSFETs suffer from parasitic effects that still require thorough investigation and proper solutions before the superior, intrinsic channel material properties of InGaAs can be exploited fully. In particular, interface traps (ITs) and border traps (BTs) are among the most severe limiting factors in these devices, leading to threshold voltage (V_{TH}) shifts and contributing to degradation of key parameters such as sub-threshold slope and channel mobility, as well as representing a reliability issue [2]. For these reasons, developing an in-depth understanding of interface- and border-trap effects is important at the current stage of InGaAs MOSFET develop-

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ment, characterized by intense technological optimization efforts, as well as, prospectively, in view of the phase when reliability of these devices will start being systematically tested and analysed.

Accurate channel mobility measurement is another key requirement for design and optimization of InGaAs MOSFETs, as the potential of these devices for logic performance improvement over Si MOSFETs relies on actual achievement of high mobility values in the device channel [3]. In this regard, the split-CV technique represents a simple method widely adopted for fast channel mobility assessment [4], despite its accuracy has been shown to be affected by several error sources (including the contribution of interface traps) [5-8].

Within the above context, this work shows measurements and device simulations of InGaAs MOSFETs, aiming to provide insight into the effects induced by ITs and BTs on IV, CV and split-CV measurements in these devices. Simulation results are calibrated against experimental data from devices having different channel thicknesses. The BT distribution is in particular adjusted, to reproduce the hysteresis observed in the drain-current (I_D) vs gate-source-voltage (V_{GS}) curves. The sensitivity of the hysteresis magnitude to BT parameters is then analysed, in order to provide indications about the possibility for the technologist to use this parameter as a reliable metrics for gate stack optimization. The impact of the spurious contributions of ITs and BTs to the total gate charge is eventually investigated, allowing possible, critical aspects in the interpretation of CV measurements in ultrathin-channel devices and in the accuracy of split-CV mobility data to be pointed out.

The paper is organised as follows. In Section 2 devices under study and the corresponding adopted simulation set-up are described. Results are shown in Section 3, including the analysis of current-voltage, capacitance-voltage and split-CV mobility data. Conclusions are drawn in Section 4.

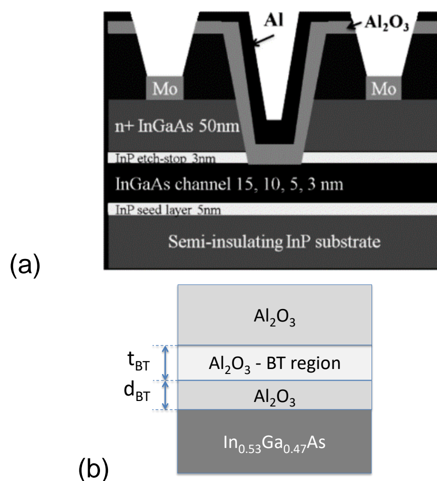

Figure 1. (a) Schematic cross section of the InGaAs MOSFETs under study (not to scale). (b) Sketch of the border trap region (not to scale) within the Al_2O_3 gate dielectric and definition of the BT region thickness (t_{BT}) and distance from interface (d_{BT}).

2 Samples and simulation set-up. Devices adopted for this study are $In_{0.53}Ga_{0.47}As$ MOSFETs having the cross section shown in Fig. 1a. The gate length is 10 µm. The high-k gate dielectric is ALD-deposited Al_2O_3 having a thickness of 10 nm (EOT of 4.9 nm). More details about fabrication technology can be found elsewhere [9].

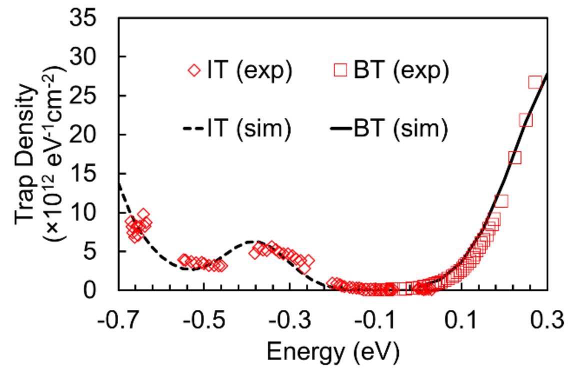

Figure 2. Experimental (symbols) energetic distribution of interface (IT) [11] and border (BT) traps [12] and fitting curves adopted in the simulations (lines). Fitting curves are combinations of Gaussian and exponential functions. Energy is referred to the InGaAs conduction-band edge.

Device simulations were carried out, by using the Sentaurus Device simulator [10]. The drift-diffusion transport model was adopted, with quantization effects in the thin InGaAs channel accounted for by means of the “density-gradient” model [10]. BTs were included in our simulations by defining a separate layer embedded into the gate dielectric at a distance d_{BT} from the Al_2O_3/InGaAs interface and having a thickness t_{BT}, see sketch in Fig. 1b. Energetic distribution of ITs and BTs traps were taken from [11] and [12], respectively, where measurements are reported for the same Al_2O_3/ $In_{0.53}Ga_{0.47}As$ gate stack technology considered here. Measured IT and BT distributions are shown in Fig. 2 as symbols. In agreement with previous literature, we assumed the charge neutrality level at the Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface to be located at about the InGaAs conduction band edge [12], this practically meaning that ITs and BTs were assumed to be all donor- and all acceptor-like traps, respectively. The distributions that were implemented in the simulator are shown in Fig. 2 as lines. The IT distribution was specifically approximated by the sum of a Gaussian and an exponential distribution, whereas the BT one was simply modelled by a single Gaussian distribution.

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The peak BT density of 3×10^{13} $eV^{-1}cm^{-2}$ adopted in our simulations (see Fig. 2) corresponds to a volumetric concentration of 6×10^{19} $eV^{-1}cm^{-3}$ over a 5-nm thick BT region, which compares well with the values ranging from 1.5×10^{19} to 1×10^{20} eV^{-1} cm^{-3}, obtained with capacitance/conductance measurements in [13] and with transconductance vs frequency techniques in [14]-[16].

Nonlocal tunnelling from the Al_2O_3/InGaAs interface into BTs allows the latter to capture channel electrons as the device is driven into on-state conditions. The simulator's so-called "tunnelling-into-traps" model [10] was activated to account for this effect under both dynamic voltage sweeps and ac multi-frequency CV simulations. In this model, the capture rate (typical of a SRH formalism) is calculated by taking into account the tunnelling probabilities obtained by using the WKB approximation [10].

InGaAs mobility used in the simulations is shown as curve #2 in Fig. 7 for the device having a channel thickness (t_{CH}) of 15 nm and in Fig. 9 for the MOSFETs having t_{CH}=10 nm and 5 nm. These mobility values are significantly larger than the ones measured by using the split-CV technique. This aspect will be commented in detail in Section 3.3.

3 Results

3.1 Hysteresis in the transfer IV characteristics. Double-sweep, experimental and simulated I_D vs V_{GS} characteristics are shown in Fig. 3 at two different drain-source voltages (V_{DS}) for a device having a 15-nm thick channel. The sweep rate is ≈0.32 V/s in both measurements and simulations, that results in t = 91 ms measurement time per point. The holding time is zero. Moreover, there is no delay between the up- and the down-direction curves. As can be noted, experimental curves exhibit a small hysteresis effect. An enlarged plot of the region where hysteresis is maximum is plotted in the inset in Fig. 3(a) for V_{DS}=0.5 V only. BTs capture channel electrons via the nonlocal tunnelling process as the device is driven from off to on state (up-direction). When V_{GS} is then decreased back to off-state conditions (down-direction), owing to the finite trap emission time, the negative charge trapped into BTs dynamically reduces the channel conductivity. This leads to a transfer curve that is right-shifted with respect to the up-direction one, thus generating the hysteresis. As can be noted, simulations with the inclusion of BTs are in good agreement with experimental curves and, specifically, allow the hysteresis effect to be reproduced. Simulations without the inclusion of BTs are also reported for the case of V_{DS}=0.5 V. If BTs are not accounted for in the simulations, no hysteresis is predicted by simulations. This confirms the fact that BTs are at the origin of the hysteresis in the transfer curves, as also found in [17].

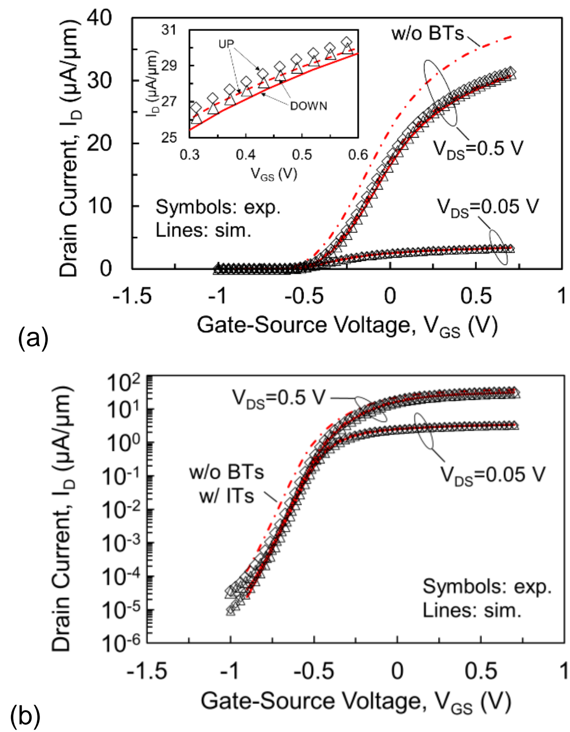

Figure 3. (a) Double sweep experimental (symbols) and simulated (lines) drain-current vs gate-source-voltage characteristics for two drain-source voltages (V_{DS}=0.05 V and 0.5 V). Simulated curves obtained without including the border traps are also shown for the case of V_{DS}=0.5 V. The device has a 15-nm thick channel. The inset shows an enlarged plot of the region where hysteresis is maximum for the case of V_{DS}=0.5 V. (b) Same as (a) but in semi-log scale.

Besides generating the hysteresis, BTs also lead to on-state I_D reduction (compare simulated transfer curves at V_{DS}=0.5 V with and without BTs in Fig. 3). Other causes can however contribute to I_D decrease at high V_{GS}, namely series resistances and mobility degradation. It is therefore important to decouple the effect of BTs from these other degradation sources, so that their impact can be evaluated correctly for process and device optimization. Hysteresis magnitude can be adopted to this purpose, as a simple but sensitive BT marker, as analysed in the next section.

3.2 Sensitivity of hysteresis to BT parameters. In this section we present and discuss the result of simulations obtained by varying the BT energy distribution and the geometrical parameters d_{BT} and t_{BT} defining the BT region (see Fig. 1b). The aim of this analysis is to assess sensitivity of hysteresis in the transfer IV curve to BT parameters and, ultimately, to get indications about the suitability of the hysteresis as a BT monitor in the device/technology optimization loop.

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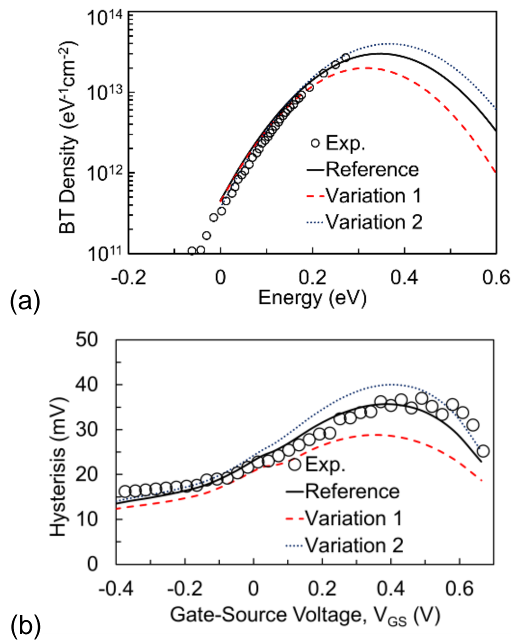

Figure 4. (a) Gaussian energy distributions of border traps adopted in the simulations (parameters listed in Table 1), as compared to data from [12]. Energy is referred to the InGaAs conduction-band edge. (b) Corresponding hysteresis magnitude as a function of gate-source voltage. The device has a 15-nm thick channel.

Table 1. BT energetic distribution parameters.

	Peak concentration N_0 ($eV^{-1}cm^{-2}$)	Peak position E_0 (eV)	Standard deviation E_S (eV)
Reference	$3x10^{13}$	2.90	0.120
Variation 1	$2x10^{13}$	2.93	0.115
Variation 2	$4x10^{13}$	2.88	0.120

As far as the BT energy distribution is concerned, we used three different sets of parameters. This is shown in Fig. 4a where we used three different Gaussian distributions to match the experimental BT profile extracted in [12]. The corresponding distribution parameters are summarised in Table 1, where N_0 is the peak of the concentration per unit area (the spatial BT distribution within the t_{BT}-thick region being assumed uniform), E_0 is the peak position (in energy) referred to the conduction band edge of the gate oxide material (Al_2O_3), while E_S is the standard deviation of the assumed Gaussian distribution.

Figure 4b shows the hysteresis magnitude, evaluated at different constant I_D values, as a function of the corresponding V_{GS} (on the up-direction curve), for the three BT energy distributions of Fig. 4a and Table 1. As can be noted, the reference distribution is the one that allows the hysteresis magnitude to be reproduced more accurately and was obtained through calibration of the IV transfer curves, as shown in Fig. 3. As shown in Fig. 4b, the two varied BT distributions give rise to different hysteresis vs V_{GS} curves. Even though all of the three BT distributions approximate fairly well the experimental data in the energy range where they could be extracted (see Fig. 4a), they give rise to appreciable deviations in the maximum hysteresis magnitude (see Fig. 4b). It is worth pointing out that hysteresis magnitude in Fig. 4b does not vanish at the extreme V_{GS} points simply as a result of the way hysteresis is calculated, i.e. as the difference in the V_{GS} values required on the up- and down- direction curves to yield the same current value. Other possible contributions to transfer IV curve hysteresis effects in these narrow-gap channel devices can come from trapping of holes generated by either band-to-band tunnelling or impact ionization at the drain side of the channel. These phenomena can have an appreciable impact in the subthreshold regime only (not investigated in this work).

Table 2. Geometrical parameters defining the BT region.

Configuration	d_{BT} (nm)	t_{BT} (nm)
A	0.5	5
B	0.5	3
C	0.5	1
D (reference)	1	5
E	1	3
F	1	1
G	1.5	5
H	1.5	3
I	1.5	1

A variation on the hysteresis is produced also by changing the geometrical parameters t_{BT} and d_{BT} defining the BT region thickness and distance from the interface (see Fig. 1). A total of 9 different configurations were considered, as summarised in Table 2. The corresponding hysteresis vs V_{GS} curves are shown in Fig. 5. Again, the reference configuration D (d_{BT}=1 nm, t_{BT}=5 nm) is the one obtained from the calibration of the IV curves. Comparable results, in good agreement with experimental hysteresis data, are also obtained for the other two configurations characterized by t_{TB}=5 nm, i.e. configurations A and G. On the other hand, one can observe how almost no hysteresis is present if the BT layer is 1 nm thick, regardless of the distance between this layer and the Al_2O_3/InGaAs interface, as if no border traps were included (configurations C, F, and I). The same holds true also for t_{BT}=3 nm if d_{BT} is too small (configurations B and E), whereas configuration H (d_{BT}=1.5 nm, t_{BT}=3 nm) yields hysteresis data not too far from experimental results. This suggests that, in order for the border traps to produce a hysteresis effect that agrees

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with measurement, BTs must extends deeply enough inside the gate dielectric ($d_{BT} + t_{BT} > 4.5$ nm in the devices under study).

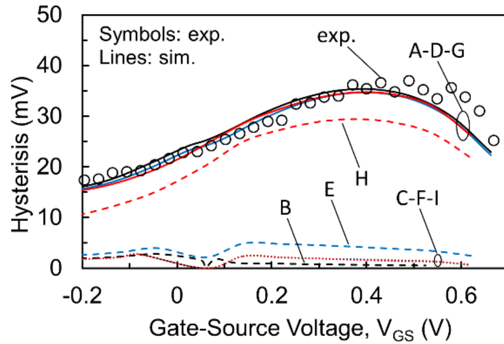

Figure 5. Hysteresis magnitude as a function of gate-source voltages for the different geometrical BT parameter configurations listed in Table 2. The device has a 15-nm thick channel.

3.3 Effect of ITs and BTs on split-CV mobility extraction.

In this section we discuss the errors caused by the presence of ITs and BTs on mobility measurements based on the split-CV technique [4]. Mobility is obtained from the I_D vs V_{GS} relationship that holds in linear region, i.e.

$$\mu_n = \frac{L}{W}\frac{I_D}{Q_n V_{DS}} \qquad (1)$$

where L and W are the gate length and width, respectively, whereas Q_n is the free electron charge in the channel. The latter is calculated by integrating the gate capacitance C_G, i.e.

$$Q_n = \int_{-\infty}^{V_{GS}} C_G\,(V)dV \qquad (2)$$

Measured and simulated C_G-V_{GS} curves are shown in Fig. 6 for 1 kHz and 1 MHz frequency. As can be noted, simulations yield CV curves in reasonably good agreement with experiments, considering that no further adjustment of input parameters was carried out, i.e. input parameters (including IT and BT ones) are the same adopted for IV simulations shown in Fig. 3. The frequency dispersion in the CV curves is commonly attributed to the presence of ITs/BTs. In the subthreshold or depletion region ITs are generally held responsible for dispersion, whereas in above-threshold region or accumulation region BTs are blamed. Our simulations confirm this. Particularly, as can be noted in Fig. 6, if no BTs are included, no dispersion is found in the accumulation region.

It is worth stressing that the BT contribution to the accumulation capacitance somewhat compensates for the quantization effects occurring in the channel, as far as their impact on gate capacitance is concerned. In this sense, our simulations yield the same qualitative results obtained with models that consider border traps as a distributed RC network [13, 18]. Actually, BTs tend to increase the total gate capacitance, whereas quantization effects in the narrow channel tend to decrease it, by shifting the electron density centroid away from the dielectric-semiconductor interface. This is insidious for the technologist since it may lead to CV data misinterpretation.

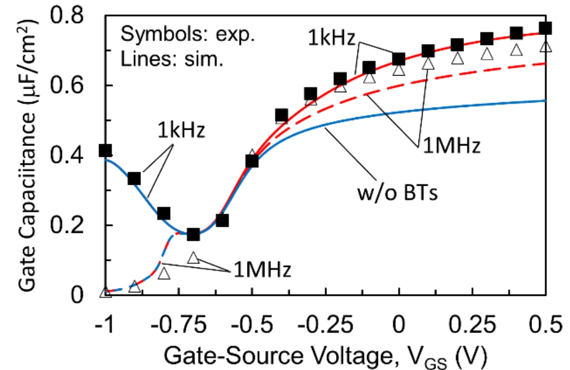

Figure 6. Experimental and simulated gate-capacitance vs gate-source-voltage curves at two different frequencies. Simulations without border traps are also shown. The device has a 15-nm thick channel.

Our analysis of the effects of ITs and BTs on split-CV mobility extraction is illustrated in Fig. 7, where experimental mobility vs V_{GS} data (symbols) are compared to several different simulated mobility curves (curves #1 to #5) for the device with t_{CH}=15 nm. First of all curve #1 is the mobility obtained by applying to simulated IV and CV data the same formulas (1) and (2) used experimentally. Not surprisingly, curve #1 is in good agreement with measured mobility as a trivial consequence of the good agreement achieved between simulated and experimental curves in Fig. 3 and 6. Curve #2 represents instead the mobility that was used as an input to simulations. Once BT parameters had been adjusted so as to match the hysteresis magnitude and source/drain contact resistances had been set to measured values [9], the on-state current remained a sensitive function of channel mobility only, this allowing the latter to be adjusted in a rather controlled way. Only the peak mobility was actually used as a fitting parameter in the calibration phase, while keeping the mobility degradation rate at increasing V_{GS} same as in the experimental mobility curve. The large discrepancy between curves #1 and #2 suggests that mobility extraction by means of the split-CV method is affected by large errors. A factor-of-3 larger mobility had actually to be assumed in simulations compared to extracted values (compare curve #2 and symbols in Fig. 7). Similar results were obtained by one of the authors in [5]. It is important, in our opinion, having confirmed here this result in a different InGaAs MOSFET technology.

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Curve #3 in Fig. 7 represents mobility values obtained still by using (1), but with Q_n obtained by integrating the free electron density in the channel (extracted by simulations) in place of using (2). As can be noted, in this case mobility almost completely reconciles with the one used as an input to simulations, pointing out that inaccuracies in mobility extraction by means of (1)-(2) are mainly related to calculation of Q_n based on (2).

Curves #4 and #5 are finally the mobilities calculated by respectively adding the BT charge and both IT and BT charges to the free channel charge in the calculation of Q_n before plugging it into (1). The mobility curve #4 drops significantly compared to curves #2 and #3. This means that a large contribution to split-CV mobility inaccuracy is due to BT spurious contribution to the total gate charge. Curve #5, including also IT charge, drops further, closely approaching measured data, indicating that also ITs contribute to mobility extraction inaccuracy (yet to a lesser extent than BTs).

Table 3 summarizes the different methods and quantities used to derive the mobility curves shown in Fig. 7 and described above.

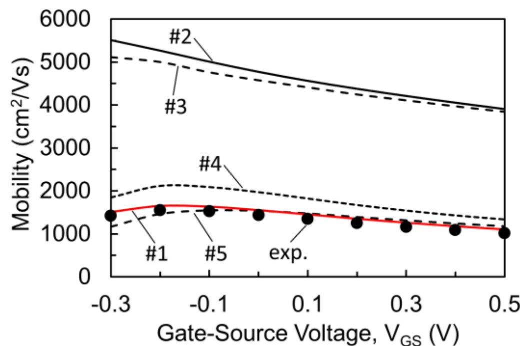

Figure 7. Channel mobility measured as a function of gate-source voltage with the split-CV method (symbols), as compared to several simulated mobility curves (see Table 3). The device has a 15-nm thick channel.

Table 3. Quantities used in (1) to derive mobility curves in Figs. 7 and 9.

Curve label	Drain current, I_D	Gate charge, Q_n
exp.	Measured I_D	Integral of measured gate capacitance.
#1	Simulated I_D	Integral of simulated gate capacitance.
#2	I_D and Q_n are not used. This is the mobility that had to be adopted as an input in the simulations to fit experimental IV curves.	
#3	Simulated I_D	Integral of simulated free electron charge in the channel.
#4	Simulated I_D	Integral of simulated free electron charge in the channel plus BT charge.
#5	Simulated I_D	Integral of simulated free electron charge in the channel plus BT and IT charges.

Extension of our analysis to narrower channel devices is illustrated by Figs. 8 and 9. Experimental and simulated transfer characteristics are reported in Fig. 8 for a V_{DS} of 0.5 V. The curves for t_{CH} =15 nm already shown in Fig. 3 are included here for easier comparison. As can be noted, a good agreement between simulated and measured characteristics is achieved also for the two smaller t_{CH} values of 10 and 5 nm. This was achieved by adjusting the mobility in the InGaAs channel. A degradation in the latter parameter for decreasing t_{CH} was actually expected based on results shown in [9]. However, consistently with results shown in Fig. 7 for t_{CH}=15 nm, even for narrower channel devices the mobility values that had to be accounted for in the simulations were significantly larger than those extracted by means of the split-CV method. This is illustrated in Fig. 9, where experimental mobility vs V_{GS} data (symbols) are compared, for the two cases of t_{CH}=10 nm and 5 nm, to: (i) the mobility that was used as an input to simulations (curves labelled as #2), (ii) the mobility obtained with (1), after adding both IT and BT charges to the free channel charge in the calculation of Q_n before plugging it into (1) (curves labelled as #5). As can be noted, similarly to what obtained for t_{CH}=15 nm (see Fig. 7), curves #2 are characterized by mobility values significantly larger than those obtained experimentally with the split-CV technique, whereas curves #5 are in good agreement with the experimental one.

It is worth pointing out that correction of Q_n requires the latter to be depurated from IT and BT contributions for the case of t_{CH}=10 nm (exactly as for t_{CH}=15 nm), whereas it also necessitates the free electron charge in the InP bottom channel confinement layer to be excluded (in addition to the IT and BT charges) in the case of t_{CH}=5 nm. This as a consequence of the nonnegligible electron deconfinement out of the InGaAs channel predicted by our simulations in the narrowest t_{CH} device, in agreement with k.p calculations shown in [9].

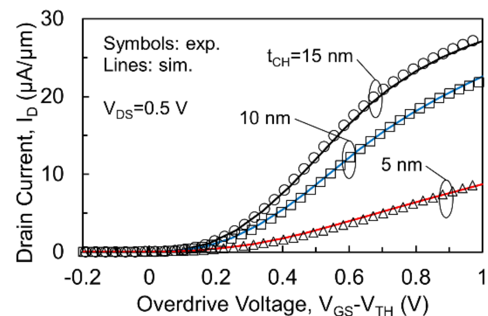

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Figure 8. Experimental (symbols) and simulated (lines) drain-current vs overdrive voltage (V_{GS}-V_{TH}) characteristics at a drain-source voltage of 0.5 V for devices having different channel thicknesses (t_{CH}).

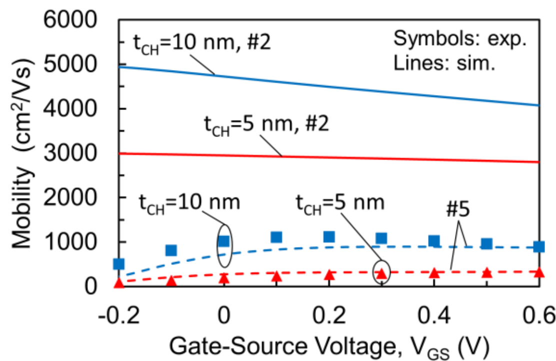

Figure 9. Channel mobility measured as a function of gate-source voltage with the split-CV method (symbols) in the devices with 10-nm and 5-nm channel thickness, as compared to simulated mobility curves (curves labelled as #2 and #5, see Table 3).

4 Conclusions. We presented the results of a coupled experimental/simulation analysis of InGaAs MOSFETs, especially addressing the effects of interface and border traps on the electrical characteristic and on the accuracy of split-CV mobility measurements in these devices. We showed how the hysteresis observed in double-sweep transfer IV characteristics can be used as a sensitive monitor for the border trap distribution. We pointed out that mobility measurement by the split-CV method can lead to a drastic underestimation of actual InGaAs channel mobility in these devices, as a result of the appreciable spurious contributions of interface and border traps to the total gate charge. In the case of very narrow channel devices, electron deconfinement into the InP bottom buffer layer also contributes to mobility measurement inaccuracy.

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