Insights into the Off-State Breakdown Mechanisms in Power GaN HEMTs

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Abstract

We analyse the off-state, three-terminal, lateral breakdown in AlGaN/GaN HEMTs for power switching applications by comparing two-dimensional numerical device simulations with experimental data from device structures with different gate-to-drain spacing and with either undoped or Carbon-doped GaN buffer layer. Our simulations reproduce the different breakdown-voltage dependence on the gate-drain-spacing exhibited by the two types of device and attribute the breakdown to: *i*) a combination of gate electron injection and source-drain punch-through in the undoped HEMTs; and *ii*) avalanche generation triggered by gate electron injection in the C-doped HEMTs.

1. Introduction

In AlGaN/GaN HEMTs for power switching applications, the three-terminal off-state breakdown voltage (V_{BR}) is typically extended up to the vertical breakdown limit by compensating the unintentional conductivity in the buffer through Carbon (C) doping and by increasing the lateral gate-to-drain spacing (L_{GD}) [1]. V_{BR} is typically found to scale about linearly with L_{GD} with a $\Delta V_{BR}/\Delta L_{GD}$ slope that is smaller than the critical field for avalanche (E_{CRIT} = 3.9 MV/cm [2]). This is often considered to be an indication that avalanche generation should be ruled out as the V_{BR} limiting phenomenon. Doing so corresponds, however, to assuming a quite idealized, constant electric-field distribution throughout the access region between gate and drain. The latter is on the contrary two-dimensional and, above all, characterized by intense accumulation spots at the drain-end of the gate, under the field-plate end (if present), and at the drain contact border. Moreover, it is critically impacted by the intrinsic or doping-related traps in the buffer. For these reasons, numerical device simulations are probably the only means by which the role possibly played by avalanche generation in the off-state breakdown can be clarified.

Paper [1] by Bahat-Treidel et al. is one of the very few works in the open literature providing a systematic analysis of the V_{BR} vs L_{GD} dependence in AlGaN/GaN HEMTs with and without C doping in the GaN buffer. Many other works show breakdown data for C doped devices only and/or for ungated ohmic-to-ohmic isolation structures.

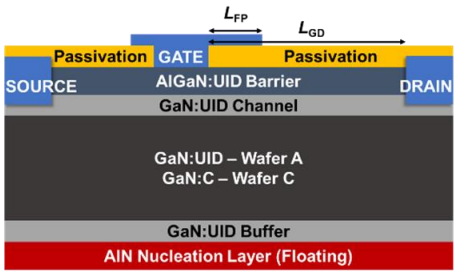

Fig. 1. Schematic cross-section of the GaN HEMT device without (Wafer A) and with C doping (Wafer C) in the buffer.

The purpose of this work is to provide physical insight into the off-state, three-terminal, lateral breakdown in AlGaN/GaN HEMTs for power switching applications and to highlight the role of avalanche generation and the other possible breakdown limiting phenomena.

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2. Device structures and simulation models

In this work, device structures and experimental data from [1] have been adopted as a reference for the numerical simulations carried out with the aim of clarifying the possible physical mechanisms limiting

Tab. I. Geometrical and model parameters of the undoped (Wafer A) device used in the simulations.

Geometrical Parameters (μm)		Model Parameters	
GaN:UID Channel Thickness	1.65	Ir/Ti/Au Gate Schottky Barrier (eV)	1.0
AlGaN Barrier Thickness	0.025	TiN S/D Workfunction (eV)	4.1
Si_3N_4 Passivation Thickness	0.15	S/D Contact Resistance (Ω.mm)	0.2
S/D Contact Length	0.1	Low-field mobility μ_n ($cm^2/V.s$)	1800
Gate-to-Source Length L_{GS}	1	Saturation velocity v_{sat} (cm/s)	$1.5x10^7$
Gate-to-Drain Length L_{GD}	1-15	UID Doping (cm^{-3})	$1x10^{15}$
Gate Extension (Source) Length	0.2	Deep Acceptor Traps Conc. N_{A1} (cm^{-3})	$5x10^{15}$
Gate Length L_G	0.7	Deep Acceptor Traps Level E_{A1} –E_V (eV)	0.6
Gate Extension (Drain) Length L_{FP}	0.6	Deep Donor Traps Conc. N_{D1} (cm^{-3})	$1x10^{16}$
		Deep Donor Traps Level E_C – E_{D1} (eV)	1.0
		Al molar fraction x ($Al_xGa_{1-x}N$)	0.26
		Polarization Activation	50%

Tab. II. Geometrical and model parameters of the C-doped (Wafer C) device used in the simulations.

Geometrical Parameters (μm)		Model Parameters	
GaN:UID Buffer Thickness	0.250	Ir/Ti/Au Gate Schottky Barrier (eV)	1.0
GaN:C Back Barrier Thickness	1.5	TiN S/D Workfunction (eV)	4.1
GaN:UID Channel Thickness	0.035	S/D Contact Resistance (Ω.mm)	0.2
AlGaN Barrier Thickness	0.025	Low-field mobility μ_n ($cm^2/V.s$)	1800
Si_3N_4 Passivation Thickness	0.15	Saturation velocity v_{sat} (cm/s)	$1.5x10^7$
S/D Contact Length	0.1	UID Doping (cm^{-3})	$1x10^{15}$
Gate-to-Source Length L_{GS}	1	Deep Acceptor Conc. N_{DA} (cm^{-3})	$8x10^{17}$
Gate-to-Drain Length L_{GD}	1-5	Deep Acceptor Level E_{DA} – E_V (eV)	0.9
Gate Extension (Source) Length	0.2	Deep Donor Conc. N_{DD} (cm^{-3})	$4x10^{17}$
Gate Length L_G	0.7	Deep Donor Level E_C – E_{DD} (eV)	0.11
Gate Extension (Drain) Length L_{FP}	0.6	Al molar fraction x ($Al_xGa_{1-x}N$)	0.25
		Polarization Activation	50%

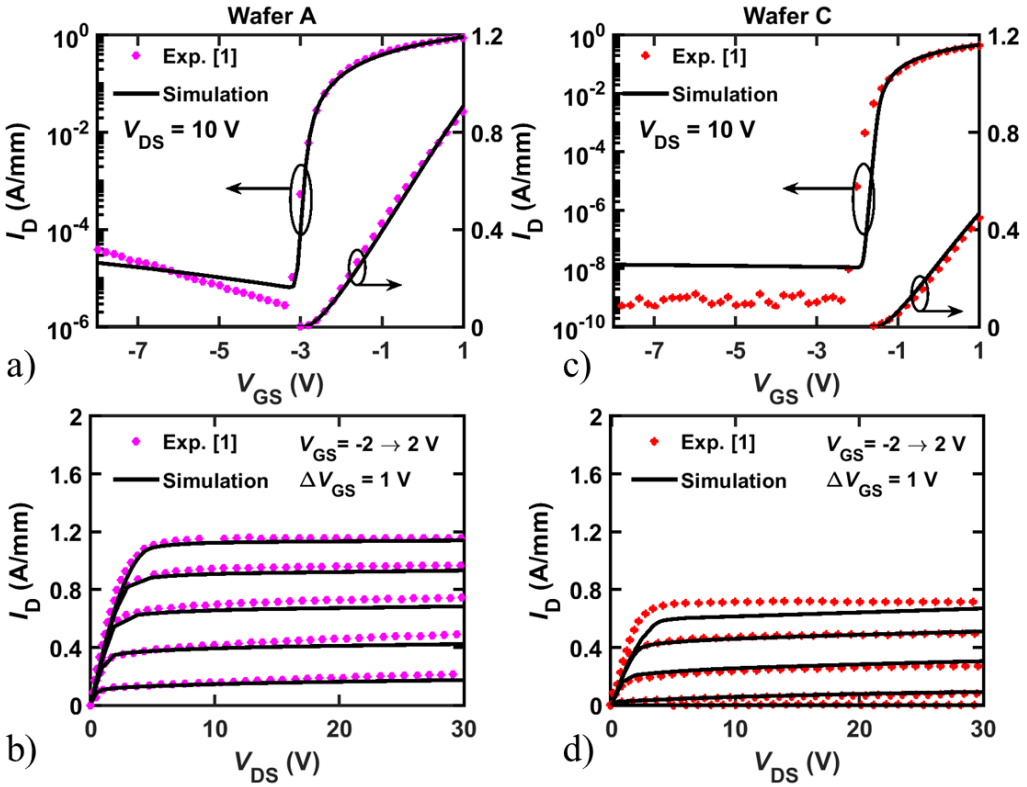

Fig. 2. I_D-V_{GS} (transfer) and I_D-V_{DS} (output) curves for a, b) Wafer A and c, d) Wafer C. For the transfer characteristic, V_{DS} is set to 10 V. For the output characteristic, V_{GS} is swept between -2 and 2 V at 1 V steps. Good overall agreement was found between experimental data [1] (symbols) and simulations (lines).

Tab. III. Chynoweth's Law coefficients values for GaN and AlGaN for the Wafer A and Wafer C devices. Values are taken from Monte Carlo simulations reported in [4] .

Impact Ionization – Chynoweth's Law Coefficients

	GaN		**$Al_xGa_{1-x}N$ (x = 0.26) Wafer A**		**$Al_xGa_{1-x}N$ (x = 0.25) Wafer C**	
	Electrons	**Holes**	**Electrons**	**Holes**	**Electrons**	**Holes**
a (cm^{-1})	$2.32x10^6$	$5.41x10^6$	$3.76x10^6$	$4.76x10^6$	$3.94x10^6$	$4.89x10^6$
b (V/cm)	$1.4x10^7$	$1.89x10^7$	$2.71x10^7$	$2.79x10^7$	$2.71x10^7$	$2.79x10^7$

V_{BR}. A sketch of the analyzed device structures is shown in Fig. 1. Gate-source spacing (L_{GS}), gate length (L_G) and gate field plate overhang (L_{FP}) are for all structures 1, 0.7, 0.6 µm, respectively. More details on device fabrication can be found in [1]. The substrate is semi-insulating SiC. The substrate contact was left floating during both measurements [1] and simulations, so that vertical breakdown is not expected to play a role for the voltage range and gate-to-drain spacing under investigation in this work. Device simulations were carried out by means of the Sentaurus Device simulator (Synopsys). Carrier distribution was modeled with Fermi-Dirac statistic, SRH recombination was included as well as mobility degradation due to doping and high field. Piezoelectric polarization was included by using the strain model included in the simulator. Both gate and source/drain contacts were modeled as Schottky contacts with proper barrier/workfunction. Electron tunneling was activated at the contacts to properly reproduce leakage currents (at the gate) and to mimic ohmic contacts (at the source and drain) [3]. In the

simulations, all process and geometrical parameters were set to their nominal values stated in [1]. A list of the parameters used in the simulation is reported in Tab. I and Tab. II for the undoped and C-doped devices, respectively. Impact-ionization coefficients for both electrons and holes were set in agreement with recent Monte-Carlo calculations [4]. Parameters used in the Cynoweth's law are listed in Tab. III.

In undoped HEMTs, the GaN buffer was modeled by assuming a pair of intrinsic donor-acceptor traps like in [5]. In C-doped HEMTs, C doping was instead modeled by dominant deep acceptor levels (at 0.9 eV from the valence-band edge, E_V) partially compensated by shallow donors (close to the conduction-band edge, E_C). In this way, the effective acceptor trap concentration was only a small fraction of the nominal C doping density, about 1%. By adjusting the donor/acceptor auto-compensation ratio, this model for C doping indeed allowed us to accurately reproduce dynamic effects in different power GaN technologies [6]–[8]. As a matter of fact, a higher donor concentration in GaN:C compared with the donor density measured in unintentionally doped samples has been confirmed experimentally in [9] and attributed to auto-compensation between C-related donors and acceptors. Moreover, a similar C model with high donor/acceptor auto-compensation ratio has recently been shown by other authors to be instrumental to achieving a realistic description of breakdown effects in C-doped GaN HEMTs [10].

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3. Results

Simulations were first calibrated against experimental transfer and output IV curves for both undoped and C-doped devices. The outcomes are illustrated in Fig. 2, showing the experimental and simulated transfer and output characteristics for undoped (Wafer A) and C-doped (Wafer C) devices. As can be noted, a satisfactory agreement was achieved in all cases.

Simulations were then used to analyze the V_{BR} vs L_{GD} scaling. Results are reported in Figs. 3 and 4, showing the experimental and simulated off-state I_D-V_{DS} curves for undoped (Wafer A) and C-doped (Wafer C) devices with different L_{GD} values and the corresponding V_{BR} vs L_{GD} plots, respectively. Consistently with [1], V_{BR} is defined as the V_{DS} value for which I_D reaches 1 mA/mm. As can be noted, an overall reasonable agreement is achieved between simulated and experimental data. In particular, the simulations are able to fully capture the completely different behavior exhibited by undoped and C-doped devices in terms of V_{BR} vs L_{GD} relationship. Namely,

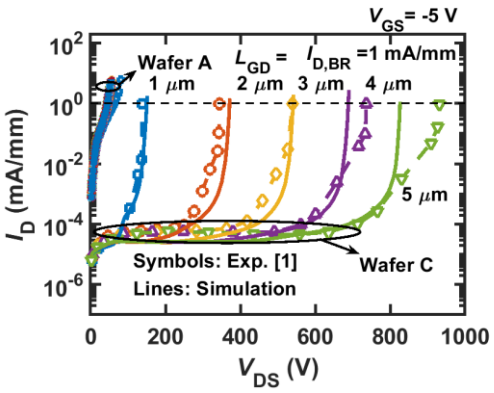

Fig. 3. Experimental **[1]** (symbols) and simulated (lines) off-state I_D-V_{DS} curves for undoped (Wafer A) and C-doped (Wafer C) devices with different L_{GD} values.

V_{BR} shows no appreciable dependence on L_{GD} in the HEMT with undoped buffer, whereas it scales almost linearly with L_{GD} in the HEMT with C-doped buffer. In this latter case, our simulations are in very good agreement with measurements for L_{GD} ranging from 1 to 3 μm, while they tend to underestimate V_{BR} for longer L_{GD} values, along with a steeper slope than experimental results. The maximum discrepancy (for L_{GD}= 5 μm) in terms of breakdown voltage matching is however less than 15% of the experimental value. Simulation results for the C-doped devices were not compared with experiments for L_{GD} > 6 μm because measurements were limited to V_{DS} = 1000 V [1], and no breakdown occurred in this range for the longer devices.

We mention the fact that breakdown voltage benefits related to C-doping are expected to come at the price of increased current collapse effects (i.e., degraded R_{ON} as well as dispersion in the I_D-V_{DS} as a consequence of increased trapping). Although we did not focus on these aspects in this contribution, it is worth noting that this trade-off is experimentally investigated in the reference paper adopted for calibration of our simulations [1].

Figure 5 shows the simulated I_D up to breakdown for the undoped and C doped devices with L_{GD}= 2 μm, along with the corresponding electron currents entering the device from the gate and the source. In both devices, I_D is about equal to the gate electron current up to breakdown, while the source electron current becomes comparable with, and, in the case of the undoped device, even larger than I_G in the breakdown regime. In the device with C-doped buffer, however, C doping effectively suppresses both gate electron injection and source-drain punch-through, so that breakdown occurs at much higher V_{DS} (at the same L_{GD}).

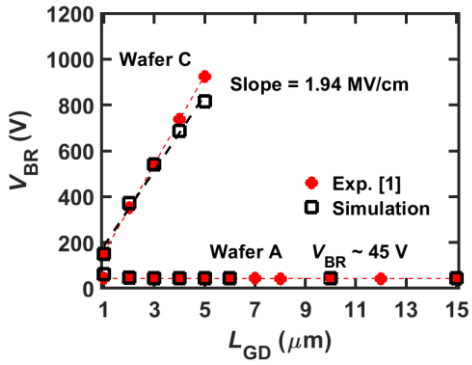

Fig. 4. Experimental [1] (red dots) and simulated (hollow black squares) off-state breakdown voltage (V_{BR}) as a function of gate-drain spacing (L_{GD}).

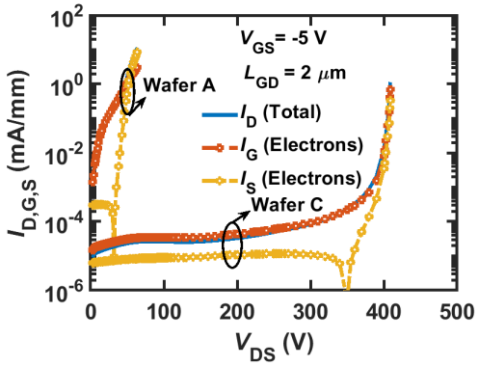

Fig. 5. Simulated drain (blue lines), gate electron (red lines), and source electron (yellow lines) currents as a function of V_{DS} for the undoped (Wafer A) and C-doped (Wafer C) devices having L_{GD}=2 µm.

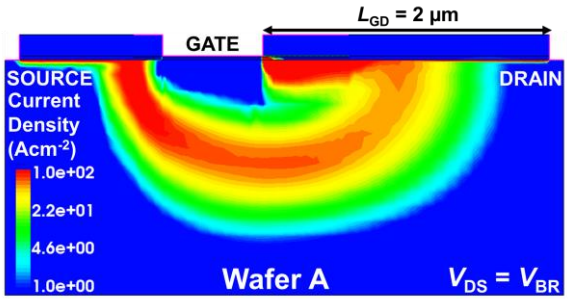

Fig. 6. Contour plot of the electron current density distribution at V_{DS}=V_{BR} in the undoped device with L_{GD}=2 µm.

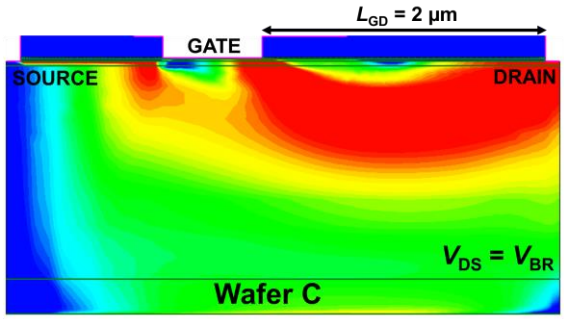

Fig. 7. Contour plot of the electron current density distribution at V_{DS}=V_{BR} in the C-doped device with L_{GD}=2 µm (same scale of Fig. 6 is used).

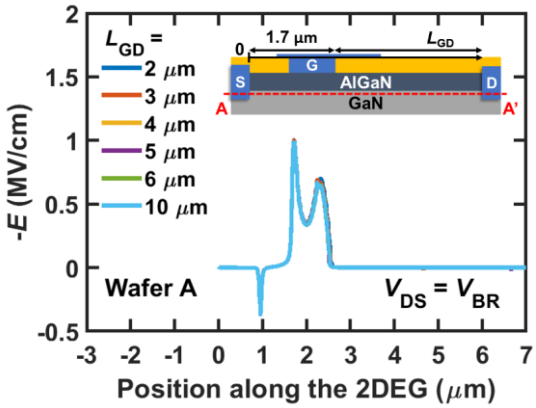

Fig. 8. Parallel component of the electric-field as a function of position along the AlGaN/GaN interface in the undoped device for different L_{GD} values at V_{DS}=V_{BR}.

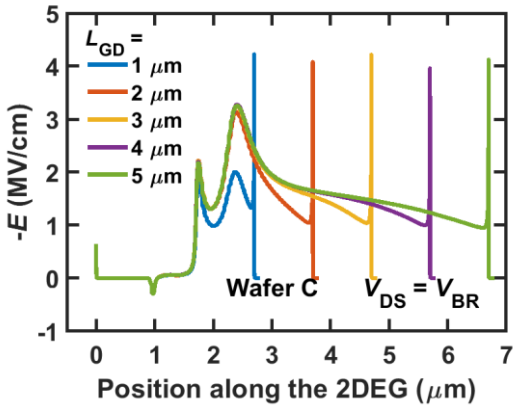

Fig. 9. Parallel component of the electric-field as a function of position along the AlGaN/GaN interface in the C-doped device for different L_{GD} values at V_{DS}=V_{BR}.

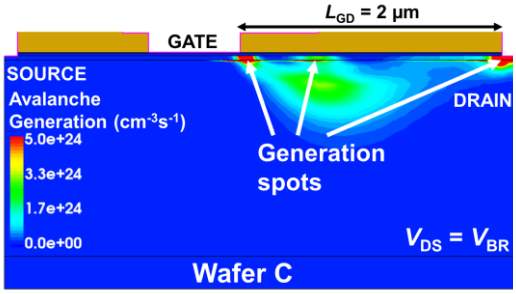

Fig. 10. Contour plot of the avalanche generation distribution at V_{DS}=V_{BR} in the C-doped device with L_{GD}=2 µm.

The presence of two conductive paths within the GaN channel/buffer, one connecting the gate to the drain, the other connecting the source to the drain, is clearly visible in Figs. 6 and 7, showing the 2D electron current density distribution at breakdown in the undoped and the C-doped device with L_{GD}=2 µm, respectively.

Figure 8 shows the electric-field distribution at breakdown (i.e., at the V_{DS} for which I_D = 1 mA/mm, consistently with measurements [1]) along the AlGaN-GaN interface in the device with undoped buffer for different L_{GD} values. In this device, the breakdown drain current limit of 1 mA/mm is reached due to the combination of gate-injected electron and source-drain punch-through currents. The electric field peak occurs at the drain-end of the gate. Its value is smaller than the critical field for avalanche and is negligibly impacted by changing L_{GD}. In the region between the end of the field plate and the drain contact, the electric field is negligibly small. For these reasons, V_{BR} is almost insensitive to L_{GD} as seen in Figs. 3 and 4.

Figure 9 shows the electric-field distribution at breakdown along the AlGaN-GaN interface in the device with C-doped buffer for different L_{GD} values. In this device, the high field region is effectively distributed throughout the gate-drain access region, and the field is nonnegligible even in the region between the field- plate end and the drain contact. For this reason, increasing L_{GD} shifts the breakdown to larger voltages. However, the electric field distribution is nonuniform, with distinct peaks at three positions along the AlGaN-GaN interface, namely in correspondence of the drain end of the gate, the field-plate end, and the drain contact. As a result, the $\Delta V_{BR}/\Delta L_{GD}$ slope is smaller than E_{CRIT}, even if breakdown is induced by avalanche generation. The critical field for breakdown is specifically reached at the drain contact for all L_{GD} values considered.

Figure 10 shows the avalanche generation distribution at V_{DS}=V_{BR} in the C-doped device with L_{GD}=2 µm, confirming the presence of the three generation spots.

4. Conclusions

We have analysed the off-state, three-terminal, lateral breakdown of AlGaN/GaN HEMTs for power switching applications, by comparing two-dimensional numerical device simulations with experimental data from device structures with different L_{GD} and with either undoped or Carbon-doped GaN buffer layers. In undoped HEMTs, the breakdown voltage is insensitive to L_{GD}, while it increases linearly with this parameter with a ≈2x10^6 V/cm slope in C-doped devices. These aspects are successfully captured by our simulations and are attributed to the different breakdown mechanisms in the two devices, namely: *i*) a combination of gate electron injection and source-drain punch-through current in undoped HEMTs; and *ii*) avalanche breakdown triggered by gate electron injection in C-doped HEMTs. In the latter case, the critical field for avalanche is reached at breakdown in correspondence of the drain contact for all L_{GD} values. The fact that the $\Delta V_{BR}/\Delta L_{GD}$ slope is, in spite of this, smaller than the critical field for avalanche is explained by the simulations as a result of the highly nonuniform electric field distribution within the gate-drain access region. Our TCAD model can be useful for designers to predict the voltage handling capabilities of GaN HEMTs during the device optimization loop, depending on the buffer doping employed. Moreover, it can also be adopted as an aid in the interpretation of failure modes during robustness and off-state step-stress tests.

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