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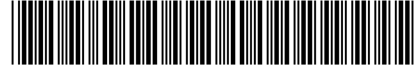

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(54) **HEMT TRANSISTOR INCLUDING FIELD PLATE REGIONS AND MANUFACTURING PROCESS THEREOF**

(57) HEMT transistor (50; 100; 150) having a semiconductor body (52) forming a semiconductive heterostructure (54, 56); a gate region (60), of conductive material, arranged above and in contact with the semiconductor body (52); a first insulating layer (58) extending above the semiconductor body, laterally to the conductive gate region (60); a second insulating layer (62) extending above the first insulating layer (58) and the gate region (60); a first field plate region (84), of conductive material, extending between the first and the second insulating layers (58), laterally spaced from the conductive gate region (60); and a second field plate region (85), of conductive material, extending above the second insulating layer (62), vertically aligned with the first field plate region (84).

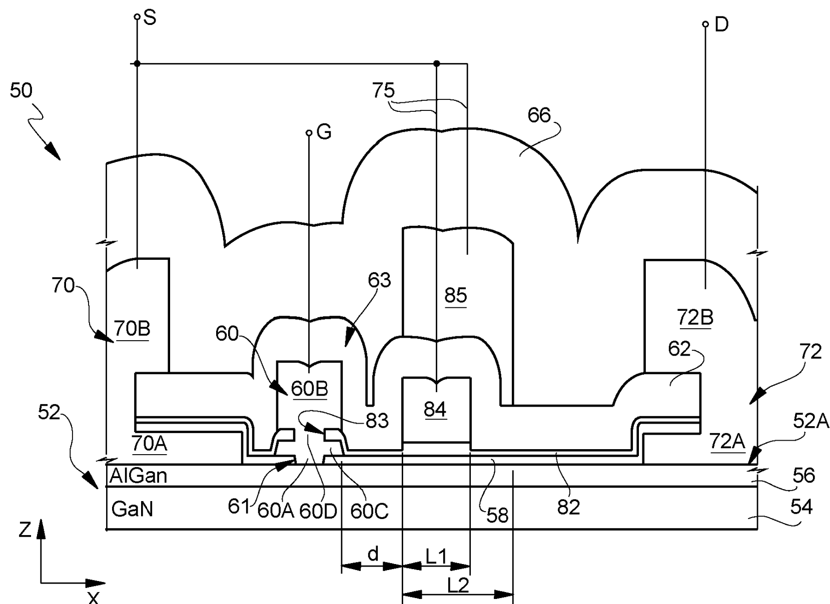

FIG. 3

EP 3 836 228 A1

Description

[0001] The present invention relates to a High Electron Mobility Transistor (HEMT) including field plate regions and the manufacturing process thereof.

[0002] As known, the HEMT transistors, also known as heterostructure field effect transistors (HFET), are finding wide diffusion, because of the possibility of operating at high voltages, as well as at high breakdown voltages.

[0003] In each HEMT transistor, a semiconductive heterostructure allows a so-called 2-dimensional electron gas (2deg), forming a channel region of the HEMT transistor, to be generated in an electronically controllable manner. Furthermore, each HEMT transistor comprises a gate region; the HEMT transistor channel is modulated by the voltage on the gate region.

[0004] For example, Figure 1 shows a HEMT transistor 1, comprising a semiconductor body 2, here formed by a first and a second layers 4, 6, hereinafter also referred to as lower layer 4 and upper layer 6.

[0005] The lower layer 4 is formed by a first semiconductor material, such as for example a first semiconductive alloy of elements of the groups III and V of the periodic table; for example, the lower layer 4 may be formed by gallium nitride (GaN).

[0006] The upper layer 6 overlies, and is in direct contact with, the lower layer 4, and is formed by a second semiconductor material, such as for example a second semiconductive alloy, different from the first semiconductive alloy, of elements of the groups III-V of the periodic table. For example, the upper layer 6 may be formed by aluminium gallium nitride (AlGaN). The lower layer 4 and the upper layer 6 are for example of N-type. Although not shown, the semiconductor body 2 further comprises a substrate, typically formed by silicon, on which the lower layer 4 is formed.

[0007] The HEMT transistor 1 further comprises a source metallization 20 and a drain metallization 22 arranged, at a mutual distance, above the upper layer 6. The source metallization 20 and the drain metallization 22 may be in direct ohmic contact with respective source and drain regions, as taught, e.g., in US 2020/0168718 (corresponding to EP 3 660 923A1). In particular, the source 20 and drain metallizations 22 have a respective lower portion 20A, 22A, directly overlying and contiguous to the upper layer 6, and a respective upper portion 20B, 22B, contiguous and in prosecution with the respective lower portion 20A, 22A. The source 20 and drain metallizations 22 are for example of titanium and aluminium or multi-layer stacks.

[0008] A first insulating layer 8, for example of silicon nitride, extends above the upper layer 6 and part of the lower portions 20A, 22A of the source 20 and drain metallizations 22. Furthermore, the first insulating layer 8 has an opening 11 arranged at an intermediate position between the lower portions 20A, 20B of the source 20 and drain metallizations 22.

[0009] A gate region 10, of conductive material, extends partly within the opening 11 (with a lower gate portion 10A) and partly above the first insulating layer 8 (with an upper gate portion 10B). The gate region 10 is formed, for example, by a stack of materials, such as nickel (Ni), gold (Au), platinum (Pt) and palladium (Pd), with the nickel layer directly in contact with upper layer 6 and forming therewith a metal-semiconductor junction of the Schottky type, that is rectifying.

[0010] A second insulating layer 12, for example of silicon nitride, extends above the first insulating layer 8 and surrounds the upper gate portion 10A. In practice, the second insulating layer 12 and the first insulating layer 8 form an insulating structure 13 sealing the gate region 10.

[0011] A field plate region 14 extends above the second insulating layer 12, partly vertically overlying the gate region 10 and partly laterally offset, towards the drain metallization region 22. The field plate region 14, for example of aluminium, has the aim of modifying the existing electric field during operation of the HEMT transistor 1. The field plate region 14 is electrically coupled to the source metallization 20, in a not shown manner.

[0012] A passivation layer 16, for example of silicon oxide, surrounds the upper portions 20B, 22B of the source 20 and drain metallizations 22 and the field plate region 14 and covers the whole structure.

[0013] Another embodiment of a HEMT transistor is described in Italian patent application 102018000011065 filed on 13 December 2018 in the name of the Applicant (corresponding to EP 3667735) and allows the drain leakage current to be reduced. This solution is shown in Figure 2, slightly modified with respect to what shown in the aforementioned patent application, to highlight the differences with respect to the HEMT transistor 1.

[0014] Figure 2 shows a HEMT transistor 30 having a general structure similar to the one of the HEMT transistor 1 of Figure 1; therefore like parts are identified with the same reference numbers and will no longer be described.

[0015] In the HEMT transistor 30 of Figure 2, the insulation structure 13 comprises, in addition to the first and second insulating layers 8, 12, a dielectric layer 32 extending between them and, partly, within the gate region 10. The dielectric layer 32 may also be of silicon nitride. In this way, the gate region 10, besides having a lower gate portion 10A and an upper gate portion 10B, has a first and a second intermediate gate portion 10C and 10D, arranged between the lower gate portion 10A and the upper gate portion 10B.

[0016] In detail, the first intermediate gate portion 10C is contiguous to the lower gate portion 10A, extends above the first insulating layer 8 and has an area (in a cross-section perpendicular to the drawing plane) approximately equal to that of the upper gate portion 10B. The second intermediate gate portion 10D is arranged between the first intermediate gate portion 10C and the upper gate portion 10B, in physical continuity with them, and has an area (in a cross-section perpendicular to the drawing plane) smaller than the area of the first interme-

diate gate portion 10C and the upper gate portion 10B. The second intermediate gate portion 10D has a thickness approximately equal to that of the dielectric layer 32.

[0017] In practice, the dielectric layer 32 extends partly laterally to the first intermediate gate portion 10C and partly (with a substantially annular portion thereof) between the first and the second intermediate gate portions 10C, 10D and has an opening (called second opening 33) accommodating the second intermediate portion 10D.

[0018] This allows the gate region 10 to be made by three different alloys (not shown); specifically, the lower gate portion 10A and the first intermediate portion 10C may be of a first metal (for example, nickel Ni) forming a Schottky contact with the body 2; the upper gate portion 10B may be of a second metal (for example, aluminium Al) having low resistance; and the second intermediate portion 10D may be of a third material (for example, tungsten nitride WN or tantalum nitride TaN or TiN), which serves as a barrier layer and prevents the aluminium of the upper gate portion 10B from diffusing, through the first intermediate portion 10C and the lower gate portion 10A, down to the upper layer 6 of the body 2, which would lead to damaging the Schottky junction.

[0019] The structures shown in Figures 1 and 2 have a very good behaviour in frequency, from frequencies lower than 6GHz up to frequencies in the range 30-50 GHz (millimetre-waves), and very good switching capacities, but are susceptible of improvement as regards the gain and electric field uniformity when high voltages are applied to the gate region.

[0020] The aim of the present invention is to provide an improved HEMT transistor.

[0021] According to the present invention, a HEMT transistor and the manufacturing process thereof are provided, as defined in the attached claims.

[0022] For a better understanding of the present invention, some embodiments thereof are now described, purely by way of non-limiting example, with reference to the attached drawings, wherein:

- Figure 1 schematically shows a cross-section of a known HEMT transistor;
- Figure 2 schematically shows a cross-section of another HEMT transistor;
- Figure 3 schematically shows a cross-section of an embodiment of the present HEMT transistor;
- Figure 4 schematically shows a cross-section of a different embodiment of the present HEMT transistor;
- Figure 5 schematically shows a cross-section of another embodiment of the present HEMT transistor;
- Figures 6A-6D show cross-sections similar to that of Figure 3, in subsequent manufacturing steps;
- Figures 7A-7D show cross-sections similar to Figure 4, in subsequent manufacturing steps; and
- Figure 8 shows the result of simulations carried out by the Applicant on the structures of Figures 1, 2, 3 and 4;
- Figure 9 is cross-section of another embodiment of the present HEMT transistor;
- Figures 10 and 11 are top plan views of different embodiments of the present HEMT transistor;
- Figure 12A-12C are top plan views of part of the HEMT transistor of Figure 5, in subsequent manufacturing steps, according to an embodiment; and
- Figures 13-17 are cross-sections of other embodiments of the present HEMT transistor.

[0023] Figure 3 shows a HEMT transistor 50 according to an embodiment.

[0024] The HEMT transistor 50 has a general structure similar to the HEMT transistor 30 of Figure 2, thus briefly described herein below; the regions thereof have been identified by numbers incremented by 50.

[0025] The HEMT transistor 50 comprises a semiconductor body 52, here formed by a lower layer 54, for example, of gallium nitride (GaN), and an upper layer 56, for example, of aluminium gallium nitride (AlGaN). The upper layer 56 forms a surface 52A of the semiconductor body 52. In a not shown manner, the semiconductor body 52 may further comprise a silicon substrate and/or the upper layer 56 may be a multilayer, including layers of AlGaN with different percentage of aluminum (for example one AlGaN layer with 20% of aluminum and another AlGaN layer with 40%).

[0026] A source metallization 70 and a drain metallization 72 extend, at a mutual distance, above the body 52. Also here, the source 70 and drain metallizations 72 comprise lower portions 70A, 72A and upper portions 70B, 72B, and are, for example, of aluminium. The source 70 and drain metallizations 72 form source and drain electrodes and are electrically coupled to respective source and drain terminals S, D.

[0027] A first insulating layer 58, for example of silicon nitride, extends above the upper layer 56 and part of the lower portions 70A, 72A of the source 70 and drain metallizations 72.

[0028] A gate region 60, of conductive material, extends above the semiconductor body 52 and comprises a lower gate portion 60A (extending into an opening, called first opening 61, of the first insulating layer 58, and in direct contact with the upper layer 56 of the semiconductor body 52), an upper gate portion 60B, a first intermediate gate portion 60C and a second intermediate gate portion 60D, arranged between the lower gate portion 60A and the upper gate portion 60B. Here again, the gate region 60 may be formed by a stack of materials, for example nickel (Ni), aluminium Al and tungsten nitride (WN) or tantalum nitride (TaN).

[0029] The gate region 60 is electrically coupled to a gate terminal G.

[0030] A dielectric layer 82, for example of silicon nitride, extends above the first insulating layer 58 and, partly, within the gate region 60. Therefore the dielectric layer 82 has an opening (also called second opening 83)

wherein the second intermediate portion 60D of the gate region 60 extends.

[0031] A second insulating layer 62, for example of silicon nitride, extends above the dielectric layer 82 and surrounds the upper gate portion 60A on the top and laterally. In practice, the second insulating layer 62 forms, with the first insulating layer 58 and the dielectric layer 82, an insulation structure 63 sealing the gate region 60.

[0032] A passivation layer 66, for example of silicon oxide, surrounds the upper portions 70B, 72B of the source and drain metallizations 70, 72 and covers the whole structure.

[0033] The transistor 50 of Figure 3 has a first and a second field plate region 84, 85, of conductive material such as a metal, for example of aluminium.

[0034] The first field plate region 84 extends above the dielectric layer 82, between the gate region 60 and the drain metallization 72, and is covered by the second insulating layer 62. In the embodiment shown, the first field plate region 84 is arranged closer to the gate region 60 than to the drain metallization 72. For example, in the direction in which the source metallization 70, the gate region 60, the first field plate region 84 and the drain metallization 72 are adjacent (direction parallel to a first Cartesian axis X in Figure 3), the first field plate region 84 may have a width L1 depending on the breakdown voltage, for example comprised between 0.1 and 3 μm, for example of 1 μm, and may be arranged at a distance d of 0.1 to 3 μm, for example of 1 μm from the gate region 60 (the distance d being calculated, approximately, from the edge of the upper gate portion 60B facing the first field plate region 84).

[0035] The first field plate region 84 may be of a same conductive material, in particular of the same metal layer, and manufactured in the same manufacturing step as the upper gate portion 60B, as discussed in detail below with reference to Figures 6A-6D.

[0036] The second field plate region 85 extends above the second insulating layer 62, vertically overlying (with respect to a second Cartesian axis Z) the first field plate region 84, and is covered by the passivation layer 66. The second field plate region 85 has a width L2 at least equal to, but generally greater than, the width L1 of the first field plate region 84. For example, the width L2 of the second field plate region 85 may be comprised between 0.1 and 5 μm.

[0037] The field plate regions 84, 85 are electrically coupled to the source metallization 70, as shown by lines 75. In particular, the second field plate region 85 may be formed together with and using the same metal layer as the upper portions 70B and 72B of the source and drain regions 70, 72.

[0038] The field plate regions 84, 85 have the effect of modifying the existing electric field and in particular making it more uniform during the operation of the HEMT transistor 50. Furthermore, the presence of the first field plate region 84 allows the gain of the HEMT transistor 50 to be considerably increased. In fact, in case of an increase in the drain voltage, the first field plate region 84, acting as a shield between the gate region 60 and the drain metallization 72, has the effect of decreasing the gate-drain capacity to which the gain is inversely related, as discussed below with reference to Figure 8.

[0039] Figure 4 shows a different embodiment of a HEMT transistor, here indicated with 100.

[0040] The HEMT transistor 100 has a general structure similar to the HEMT transistor 50 of Figure 3. The common parts have thus been provided with the same reference numbers and will not be further described.

[0041] In the HEMT transistor 100, the first field plate region, here indicated with 84', comprises a lower plate portion 84A' and an upper plate portion 84B'.

[0042] The upper plate portion 84B' of the first field plate region 84' roughly corresponds to the first field plate region 84 of Figure 3, and thus extends above the second insulating layer 62, laterally to the gate region 60, between the same and the drain metallization 72. The lower plate portion 84A' of the first field plate region 84' extends continuously from the upper plate portion 84B' towards the surface 52A of the semiconductor body 52 through an opening (called third opening 86) of the dielectric layer, here indicated with 82', and, partially, through the first insulating layer, here indicated with 58', in a cavity 87 thereof. The lower plate portion 84A', however, does not completely extend through the first insulating layer 58' and a thinner portion thereof, below referred to as thinned portion 58A', extends between the surface 52A of the semiconductor body 52 and the first field plate region 84', electrically separating the latter from the semiconductor body 52.

[0043] This embodiment is characterized by a marked increase in gain and a particularly uniform electric field, as discussed below with reference to Figure 8.

[0044] Figure 5 shows another embodiment of a HEMT transistor, here indicated with 150.

[0045] The HEMT transistor 150 has a general structure similar to the HEMT transistor 50 of Figure 3, except for the shape of the gate region (similar to the HEMT transistor 1 of Figure 1). The parts in common with the HEMT transistor 50 of Figure 3 have thus been provided with the same reference numbers and will not be further described.

[0046] In detail, the HEMT transistor 150 comprises a gate region 60" having a lower gate portion 60A" and an upper gate portion 60B". Furthermore, the HEMT transistor 150 comprises a first insulating layer, indicated with 58" and having an opening 61" accommodating the lower gate portion 60A", and a first field plate region 84". The first field plate region 84" extends above the insulating layer 58" and is coated, laterally and on the top, by the second insulating layer 62.

[0047] In this embodiment, the lower gate portion 60A" and the upper gate portion 60B" may be formed by a single deposited (for example "sputtered") metal layer or a single evaporated layer or by a stack of layers deposited separately. In the latter case, the first field plate

region 84" may be formed with one of the layers of the gate region 60".

[0048] Here again, the second field plate region 85 extends vertically (in direction of the second Cartesian axis Z) above the first field plate region 84".

[0049] This embodiment allows a simplification of the manufacturing process, due to the simple shape of the gate region 60".

[0050] The manufacturing process of the HEMT transistors 50 and 100 of Figures 3 and 4 will now be described, with reference to Figures 6A-6D and, respectively, 7A-7D. Figure 6A shows a cross-section similar to Figure 3 in an intermediate manufacturing step of the HEMT transistor 50.

[0051] In particular, Figure 6A shows an intermediate structure, wherein, above the semiconductor body 52, the lower portion 70A of the source metallization 70, the lower portion 72A of the drain metallization 72, and the first insulating layer 58 have already been formed in a per se known manner; furthermore, the first insulating layer 58 has been etched to form the first opening 61; the lower gate portion 60A in the first opening 61 and the first intermediate gate portion 60C above the lower gate portion 60A have been formed (for example, the lower gate portion 60A and the first intermediate gate portion 60C may be formed simultaneously, by physical vapor deposition (PVD) of a nickel layer within a cavity formed in a temporary structure and having a small-sized opening, related to the area of the first intermediate gate portion 60C) and, after removing the temporary structure, the dielectric layer 82 has been deposited, for example by PECVD deposition.

[0052] Next, Figure 6B, a portion of the dielectric layer 82 is removed, for example by dry etching, above the first intermediate gate portion 60C, forming the second opening 83.

[0053] Then, Figure 6C, two sputtering processes are carried out in succession; in particular a first sputtering process, of tungsten nitride (WN) or tantalum nitride (TaN), forms a first metal layer, which is thinner, fills the second opening 83 and is intended to subsequently form the second intermediate gate portion 60D, and a second sputtering process, for example of aluminium, forms a second metal layer which is thicker. The layer formed of the first and second metal layers is indicated with 200 in Figure 6C. Alternatively, a sequence of sputtered metal layers, including tungsten nitride/aluminium/titanium nitride WN/Al/TiN may be used.

[0054] Next, Figure 6D, for example using a resist mask not shown, portions of the metal layer 200 (also called gate metal layer) are selectively removed, forming the second intermediate gate portion 60D and the upper portion 60B of the gate region 60, as well as the first field plate region 84.

[0055] Known steps follow, including deposition of the second insulating layer 62, deposition of a third metal layer, for example aluminium based (such as an Al, AlSiCu or AlCu bilayer and a Ti, TiN metal layer) by sputtering and subsequent selective removal to form the upper portions 70B and 72B of the source and drain metallizations 70, 72 and the second field plate region 85. Finally the deposition of the passivation layer 66 follows.

[0056] In this way, the first field plate region 84 may be formed without adding process steps with respect to the manufacturing process of the HEMT transistor 30 of Figure 2, only through an etching mask modification of the metal layer 200, and thus without additional costs.

[0057] Figure 7A shows a cross-section similar to Figure 4 in an intermediate manufacturing step of the HEMT transistor 100.

[0058] In particular, Figure 7A shows an intermediate structure wherein, above the semiconductor body 52, the lower portion 70A of the source metallization 70, the lower portion 72A of the drain metallization 72 and the first insulating layer 58' have already been formed, in a per se known manner; furthermore, the first insulating layer 58' has already been etched to form the first opening 61, the lower gate portion 60A in the first opening 61 and the first intermediate gate portion 60C above the lower gate portion 60A have already been formed (for example, the lower gate portion 60A and the first intermediate gate portion 60C may be formed as described above for the HEMT transistor 50) and the dielectric layer 82' has been deposited, for example by PECVD deposition. The intermediate structure of Figure 7A is thus identical to that of Figure 6A.

[0059] Next, Figure 7B, a portion of the dielectric layer 82' is removed above the first intermediate gate portion 60C, forming the second opening 83. Furthermore, a portion of the dielectric layer 82' and the underlying portion of the first insulating layer 58' are selectively removed, laterally to the second opening 83, where it is desired to form the first field plate region 84', forming the third opening 86.

[0060] Then, Figure 7C, a gate metal layer 200' is deposited, for example in the manner described above with reference to Figure 6C, carrying out in succession a first sputtering process, of tungsten nitride (WN) or tantalum nitride (TaN), to form a first metal layer (which is thinner and intended to subsequently form the second intermediate gate portion 60D and the lower portion 84A of the first field plate region 84) and a second sputtering process, for example of aluminium, to form a second metal layer, which is thicker.

[0061] Next, Figure 7D, for example using a resist mask not shown, portions of the gate metal layer 200' are selectively removed, completing the gate region 60 and the first field plate region 84'.

[0062] Known steps follow, including deposition of the second insulating layer 62, deposition of a third metal layer, for example aluminium-based (as indicated above) by sputtering and subsequent selective removal to form the upper portions 70B and 72B of the source and drain metallizations 70, 72 and the second field plate region 85. Finally, the deposition of the passivation layer 66 follows.

[0063] Also in this case, the first field plate region 84 may be formed without adding process steps with respect to the manufacturing process of the HEMT transistor 30 of Figure 2, through an etching mask modification of the gate metal layer 200', and thus without additional costs.

[0064] Similarly, the manufacturing process of the HEMT transistor 150 does not require additional steps with respect to those foreseen for forming the HEMT transistor 1 of Figure 1, only requiring modification of the mask used to define the gate region 60" in order to form the first field plate region 84".

[0065] The HEMT device shown in Figures 3-5 has many advantages. As indicated, due to the presence of an additional shielding region (first field plate region 84, 84', 84"), the HEMT device described has a high gain, as shown in Figure 8.

[0066] In particular, Figure 8 shows the result of simulations carried out by the Applicant relative to the plot of the gain G obtainable with the HEMT transistor as a function of the frequency f in the range 2-10 GHz, for the HEMT transistor 1 of Figure 1 (curve A), the HEMT transistor 30 of Figure 2 (curve B), the HEMT transistor 50 of Figure 3 (curve C) and the HEMT transistor 100 of Figure 4 (curve D), respectively. As visible, the HEMT transistors 50 and 100 have a considerably greater gain with respect to the similar structures lacking the first field plate region 84, 84'.

[0067] In a not shown manner, the HEMT device shown in Figures 3-5 allows a not negligible improvement to be obtained also as regards electric field uniformity and thus its robustness at high voltages.

[0068] Finally, it is clear that modifications and variations may be made to the HEMT transistor and the manufacturing process thereof described and illustrated herein without thereby departing from the scope of the present invention, as defined in the attached claims. For example, the different embodiments described may be combined so as to provide further solutions.

[0069] For example, the second field plate 85 and the first field plate 84, 84', 84" may be connected in various ways to the source metallization 70; the first field plate 84" and the gate region 60" in Figure 5 may be positioned in different ways with respect to the insulating layer 58"; and the gate region 60" in Figure 5 may be defined in different ways, as discussed in detail hereinafter.

Connection of the second field plate 85

[0070] The second field plate 85 may be connected to the source metallization 70 through connecting regions extending either over an active area (where the 2-dimensional electron gas - 2deg- forms a channel region of the HEMT transistor and conducts current) or an inactive area surrounding the active area, as explained below.

[0071] For example, Figure 9 shows an embodiment where the HEMT transistor 150 of Figure 5 has the second field plate 85 connected to the source metallization 70 through a connecting portion formed in the third metal layer which also forms the upper portion 70B of the source metallization 70, the upper portion 72B of the drain metallization 72 and the second field plate region 85, and thus defined in the same etching step.

[0072] In particular, in Figure 9, a biasing metal portion 88 of the third metal layer extends on the second insulating layer 62 between the upper portion 70B of the source metallization 70 and the second field plate region 85 and forms a single region with them.

[0073] According to a different embodiment, the second field plate 85 is connected to the source metallization 70 through a connecting region extending over the inactive area of the HEMT transistor 150, as described hereinbelow with reference to Figure 10, which shows the structure of an elementary cell of the HEMT transistor 150 of Figure 5 in a plan view.

[0074] It is intended that the HEMT transistor 150 may comprise a plurality of elementary cells, each having at least one source metallization 70, at least one drain metallization 72, at least one first field plate 84, and at least one second field plate 85, extending as fingers along a direction (vertical direction of Figure 10).

[0075] Figure 10 shows a portion of an intermediate structure of the HEMT transistor 150 after depositing and defining the second insulating layer 62 (not visible in Figure 10) and depositing and defining a third metal layer, indicated by 98, to form the upper portions 70B and 72B of the source and drain metallizations 70, 72 and the second field plate region 85. In particular, Figure 10 shows the active area 90 (which accommodates high mobility conduction electrons of the 2-deg), surrounded by the inactive area 91, not participating to the conduction action. The inactive area 91 is generally doped, to avoid passage of current when the HEMT transistor 150 is switched off.

[0076] In figure 10, line 93 indicates the boundary of the active area 90.

[0077] Here, the third metal layer 98 is also defined to form a second field plate connecting region 97 extending over the inactive area 91 between the upper portion 70B of the source metallization 70 and the second field plate region 85, thereby connecting them electrically.

[0078] According to a different embodiment, Figure 11, the second field plate 85 is connected to the source metallization 70 through a plurality of clips or bridge portions 105 extending at a distance to each other over the active area 90 and formed by the second metal layer 200". In this case, in a cross-section, the clips 105 are not visible (as in Figure 5) or have a shape similar to the biasing metal portion 88 of Figure 9, depending on whether the cross section through the HEMT transistor 150 is drawn in an area between two adjacent clips 105 or crosses one of the clips 105.

[0079] According to still another embodiment, the second field plate 85 is connected to the source metallization 70 by both the second field plate connecting region of Figure 10 and the clips 105 of Figure 11.

Connection of the first field plate 84, 84', 84"

[0080] The first field plate 84, 84', 84" may be connected to the source metallization 70 through connecting regions extending over the inactive area 91 or through the second field plate 85, as explained below.

[0081] For example, the first field plate 84, 84', 84" may be connected to the source metallization 70 as shown in Figures 12A-12C, which show the structure of an elementary cell of the HEMT transistor 150 of Figure 5 in three intermediate manufacturing steps (connection over the inactive area 91).

[0082] Also here, the HEMT transistor 150 may comprise a plurality of elementary cells, each having at least one source metallization 70, at least one drain metallization 72, at least one first field plate 84, and at least one second field plate 85, extending as fingers along a direction (vertical direction of Figures 12A-12C).

[0083] Figure 12A shows a portion of the intermediate structure of the HEMT transistor 150 after forming the lower portions 70A, 72A of the source and drain metallizations 70, 72, and after forming and defining the insulating layer 58" (Figure 5) .

[0084] In figure 12A, the lower portions 70A, 72A of the source 70 and drain metallizations 72 extend mainly on the active area 90 and have ends portions 70A1, 72A1 extending on the inactive area 91. Line 93 indicates the boundary of the active area 90; line 94 indicates the boundary of insulating layer 58" (not visible) and line 95 indicates the first opening (61" in Figure 5).

[0085] Figure 12B shows the same portion of the intermediate structure of the HEMT transistor 150 after depositing and defining a metal layer (similar to gate metal layer 200' of Figure 7C), so as to form the gate region 60", the first field plate 84" and a first connecting region 96. The first connecting region 96 is integral with and in prosecution of the first field plate 84", extends from and end of the first field plate 84" onto the inactive area 91 and ends with an enlarged portion 96A.

[0086] Figure 12C shows the same portion of Figures 12A and 12B after depositing and defining the second insulating layer 62 (not visible in Figure 12C) and depositing and defining the third metal layer, indicated again by 98, to form the upper portions 70B and 72B of the source and drain metallizations 70, 72 and the second field plate region 85.

[0087] In Figure 12C, the second insulating layer 62 (Figure 5) has been defined to form a through opening 99 over the enlarged portion 96A of the first connecting region 96.

[0088] Here, the third metal layer 98 also extends over the inactive region 91 and in particular over the enlarged portion 96A and fills the through opening 99 to form a connection via (indicated by the same number 99 since it has the same shape as the through opening). The connection via 99 electrically connects the upper portion 70B of the source metallization 70 to the enlarged portion 96A of the first connecting region 96 (at a lower level) and thus to the first field plate 84".

[0089] Here, in addition, the third metal layer 98 is also defined to form the second field plate connecting region 97 extending over the inactive area 91 between the upper portion 70B of the source metallization 70 and the second field plate region 85.

[0090] Therefore, the first connecting region 96, the connection via 99 and the second connecting region 97 form line 75 of Figure 3, directly connecting the source metallization 70, the first field plate 84" and the second field plate region 85.

[0091] According to a different embodiment, the first field plate 84, 84', 84" may be connected to the source metallization 70 through the second field plate 85, as shown in Figure 13.

[0092] In detail, in Figure 13, the second insulating layer 62 has a through opening, called field plate connection opening 89, extending over the first field plate 84". Thereby, during deposition of the third metal layer 98, the metal enters and fills the field plate connection opening 89, forming a field plate via also indicated by 89 (since it has the same shape and is defined by the field plate connection opening 89). The field plate connection via 89 electrically connects the first field plate 84" to the second field plate region 85 and thus, through one of the solutions discussed above in section Connection of the second field plate 85, to the source metallization 70.

[0093] According to another embodiment, the first field plate 84, 84', 84" may be connected to the source metallization 70 both over the inactive area 91(through the first connecting region 96, the enlarged portion 96A, and the connection via 99, Figures 12A-12C) and over the active area 90 (through the field plate connection via 89, Figure 13), combining the solutions of Figures 12A-12C and Figure 13.

Arrangement of the first field plate 84"

[0094] The first field plate 84" may be arranged in different ways with respect to the insulating layer 58".

[0095] In particular, as an alternative to the arrangement shown in Figure 5, where the first field plate 84" is formed completely over the insulating layer 58", the first field plate 84" may be formed with its lower portion inside the insulating layer 58", as shown in Figure 14.

[0096] In this case, process steps similar to those described with reference to figures 7B-7D are performed. In particular, after depositing the insulating layer 58", the first opening 61 and, in a separate etching step, a cavity 87' (corresponding to the third opening 86 and the cavity 87 of Figure 4) are formed. Then, the gate metal layer (analogous to gate metal layer 200" of Figure 7C) is deposited and defined to form the gate region 60" and the first field plate region 84". Thereafter, the second insulating layer 62 and the third metal layer are deposited and defined and covered by the passivation layer 66.

[0097] According to a different embodiment, the first field plate 84" may be formed to contact the semiconduc-

tor body 52. In this case, the insulating layer 58" may be removed only partially, as shown in Figure 15.

[0098] In detail, in Figure 15, the third opening in the insulating layer 58" (here, indicated by 86') is a through opening, so that the bottom portion of the first field region 4" directly contacts the semiconductor body 52.

Arrangement of the gate region 60"

[0099] The gate region 60" may extend directly on and physical in contact with the semiconductor body 52, as shown in Figures 9, 12, 13-15 or may enter a recess in the semiconductor body 52, as shown in Figure 16.

[0100] In Figure 16, a lower gate portion 60A" of the gate 60" extends through part of the upper layer 56 of the semiconductor body 52 in a recess 79.

[0101] This solution may be used when the first field plate 84" is in direct contact with the semiconductor body 52.

Definition of gate region 60" and first field plate 84"

[0102] The gate region 60" and the first field plate 84" may be defined through known masking and etching steps, in which case the insulating layer 58" is slightly recessed as a consequence of the etching process, as shown in Figures 9, 13-17 or using a lift-off process. In this case, as shown in Figure 17, the insulating layer 58" has a planar upper surface, not recessed.

Claims

1. A HEMT transistor (50; 100; 150) comprising:

   a semiconductor body (52) having a semiconductive heterostructure (54, 56);
   a gate region (60; 60"), of conductive material, arranged on and in contact with the semiconductor body (52);
   a first insulating layer (58; 58'; 58") extending over the semiconductor body, laterally to the conductive gate region (60; 60");
   a second insulating layer (62) extending over the first insulating layer (58; 58'; 58") and the gate region (60; 60");
   a first field plate region (84, 84', 84"), of conductive material, extending between the first and the second insulating layers (58; 58'; 58", 62), laterally spaced from the conductive gate region (60; 60") and
   a second field plate region (85), of conductive material, extending over the second insulating layer(62), , the second field plate region overlying the first field plate region (84, 84', 84").

2. The HEMT transistor according to claim 1, wherein the first and the second field plate regions (84, 84', 84", 85) are of metal.

3. The HEMT transistor according to claim 1 or 2, wherein the gate region (60; 60") comprises a lower gate portion (60A; 60A") and an upper gate portion (60B, 60B"), the lower gate portion (60A; 60A") extending into a first opening (61) of the first insulating layer (58; 58'; 58") and in contact with the semiconductor body (52), and the upper gate portion (60B, 60B") being of the same material as the first field plate region (84, 84', 84").

4. The HEMT transistor according to the foregoing claim, wherein the upper gate portion (60B, 60B") and the first field plate region (84, 84', 84") are of aluminium.

5. The HEMT transistor according to any of the foregoing claims, further comprising a drain contact region (72) and a source contact region (70), of electrically conductive material, extending over and in electrical contact with the semiconductor body (52), through the first and the second insulating layers (58; 58'; 58", 62) on opposite sides of the gate region (60; 60"), wherein the first field plate region (84, 84', 84") extends between the gate region and the drain contact region (72).

6. The HEMT transistor according to the foregoing claim, wherein the first field plate region (84, 84', 84") is electrically coupled to the source contact region (70).

7. The HEMT transistor according to any of the foregoing claims, wherein the first field plate region (84, 84', 84") has a first width (L1), along the first direction(X), and the second field plate region (85) has a second width (L2), along the first direction (X), wherein the second width is greater than the first width.

8. The HEMT transistor according to any of claims 3-7, further comprising a dielectric layer (82') extending between the first and the second insulating layers (58', 62), wherein the dielectric layer (82') has a second and a third opening (83, 86), the gate region (60) having an intermediate gate portion (60C) extending into the second opening (83), between the upper gate portion (60B) and the lower gate portion (60A), and wherein the first field plate region (84') has a lower plate portion (84B') extending through the third opening (86) of the dielectric layer (82') and in a cavity (87) of the first insulating layer (58'), a reduced thickness portion (58A') of the first insulating layer (58') extending between the lower plate portion (84B') and the semiconductor body (52).

9. The HEMT transistor according to any of the forego-

ing claims, wherein the semiconductor body (52) comprises at least a first semiconductor layer (54) including aluminium gallium nitride (AlGaN), and a second semiconductor layer (56) including gallium nitride (GaN), wherein the second semiconductor layer (56) is contiguous to the first insulating layer (58; 58'; 58").

10. The HEMT transistor according to any of claims 1-4, further comprising a drain contact region (72) and a source contact region (70) of electrically conductive material, extending over and in electrical contact with the semiconductor body (52), through the first (58") and the second (62) insulating layers on opposite sides of the gate region (60"),
the semiconductor body comprising an active area (90) and an inactive area (91), the gate region, the first field plate region (84") and the second field plate region (85) extending over the active area,
wherein the first field plate region (84") is in electrical contact with the source contact region (70) through a field plate contact region (96; 96A) extending from the first field plate region on the inactive area and a connection via (99) extending between the field plate contact region and an upper portion of the source contact region.

11. The HEMT transistor according to any of claims 1-4, further comprising a drain contact region (72) and a source contact region (70), of electrically conductive material, extending over and in electrical contact with the semiconductor body (52), through the first (58") and the second (62) insulating layers on opposite sides of the gate region (60"),
the semiconductor body (52) comprising an active area (90) and an inactive area (91), the gate region (60"), the first field plate region (84") and the second field plate region (85) extending over the active area,
wherein the first field plate region (84") is in electrical contact with the second field plate region (85) through a field plate connection via (89) extending through the second insulating layer.

12. The HEMT transistor according to any of claims 1-4, further comprising a drain contact region (72) and a source contact region (70), of electrically conductive material, extending over and in electrical contact with the semiconductor body (52), through the first (58") and the second (62) insulating layers on opposite sides of the gate region (60"),
the semiconductor body comprising an active area (90) and an inactive area (91), the gate region (60"), the first field plate region (84") and the second field plate region (85) extending over the active area,
a metal portion (88; 97; 105) extending on the second insulating layer between the source contact region and the second field plate region.

13. A process for manufacturing a HEMT transistor (50; 100; 150), comprising:

forming a semiconductive heterostructure (54, 56) in a semiconductor body (52);
forming, on the semiconductor body (52), a first insulating layer (58; 58'; 58") having a first opening (61);
forming a gate region (60; 60"), of conductive material, on and in contact with the semiconductor body (52), the gate region extending into the opening (61);
forming a first field plate region (84, 84', 84"), of conductive material, on the first insulating layer (58; 58'; 58"),the first field plate region spaced laterally apart from the conductive gate region (60; 60");
forming a second insulating layer (62) over the gate region (60; 60"), the first field plate region (84, 84', 84") and the first dielectric layer (58; 58'; 58"), ; and
forming a second field plate region (85), of conductive material, over the second insulating layer (62), , the second field plate region overlying the first field plate region (84, 84', 84").

14. The process according to the foregoing claim, wherein forming a gate region (60; 60") and forming a first field plate region (84, 84', 84") comprises depositing and defining a same metal layer (200; 200').

15. The process according to the foregoing claim, comprising:

forming a lower gate portion (60A), of conductive material, in the first opening (61);
forming a dielectric layer (82; 82') over the first insulating layer (58; 58') and over the lower gate portion (60A); and
selectively removing the dielectric layer (82; 82') over the lower gate portion (60A);
wherein the metal layer (200; 200') forms an upper gate portion (60B) and the first field plate region (84; 84').

16. The process according to the foregoing claim, wherein selectively removing the dielectric layer (82') comprises removing a portion of the dielectric layer that is adjacent and not contiguous to the lower gate portion (60A), the process further comprising forming a cavity (87) in the first insulating layer (58') below the removed portion of the dielectric layer (82'), the cavity (87) overlying a reduced thickness portion (58A') of the first insulating layer (58') so that the metal layer (200') fills the cavity (87) and the removed portion of the dielectric layer.

17. The process according to any of claims 14-16,

wherein the metal layer (200; 200') is aluminium.

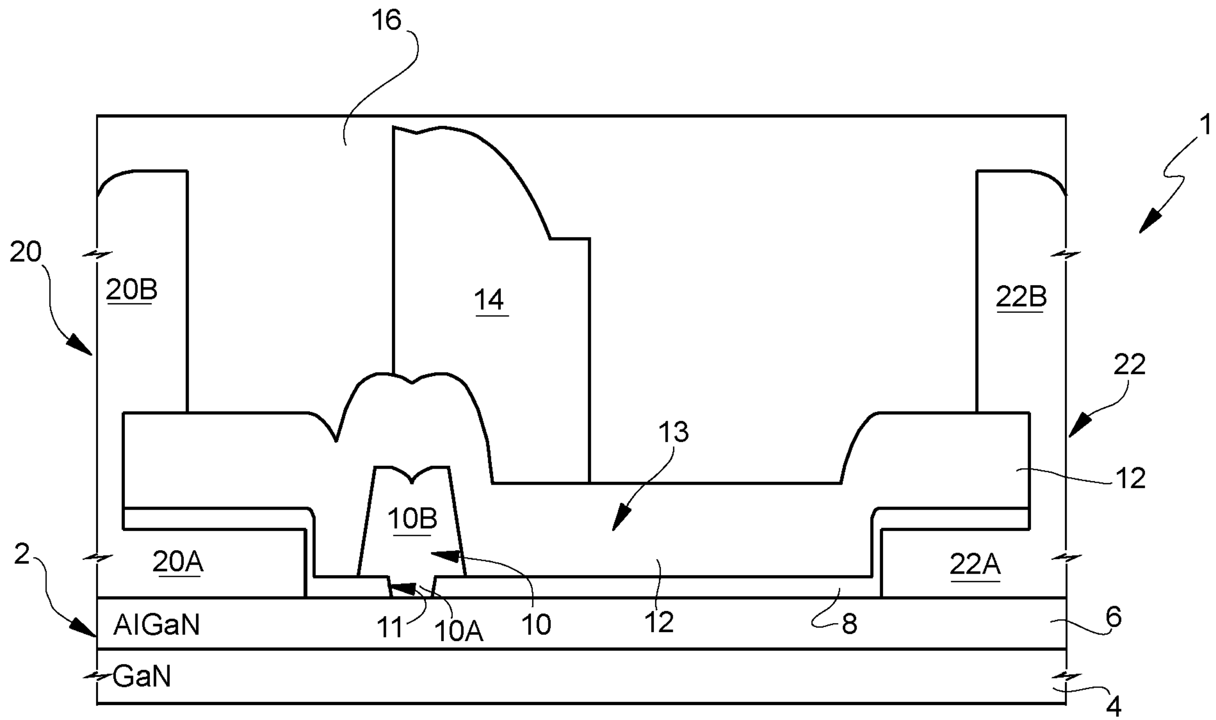

FIG. 1

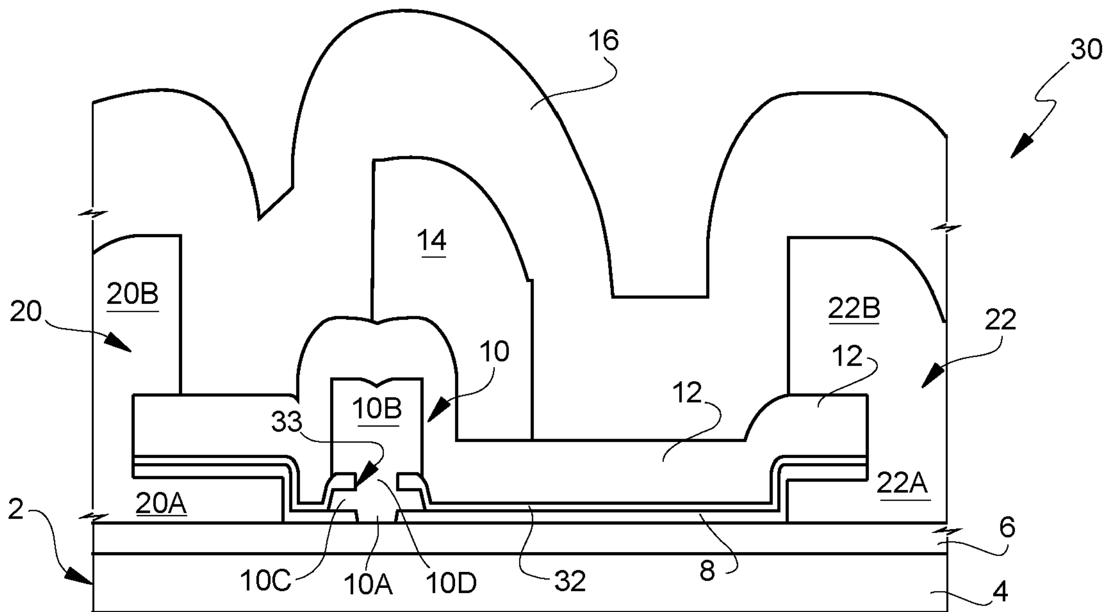

FIG. 2

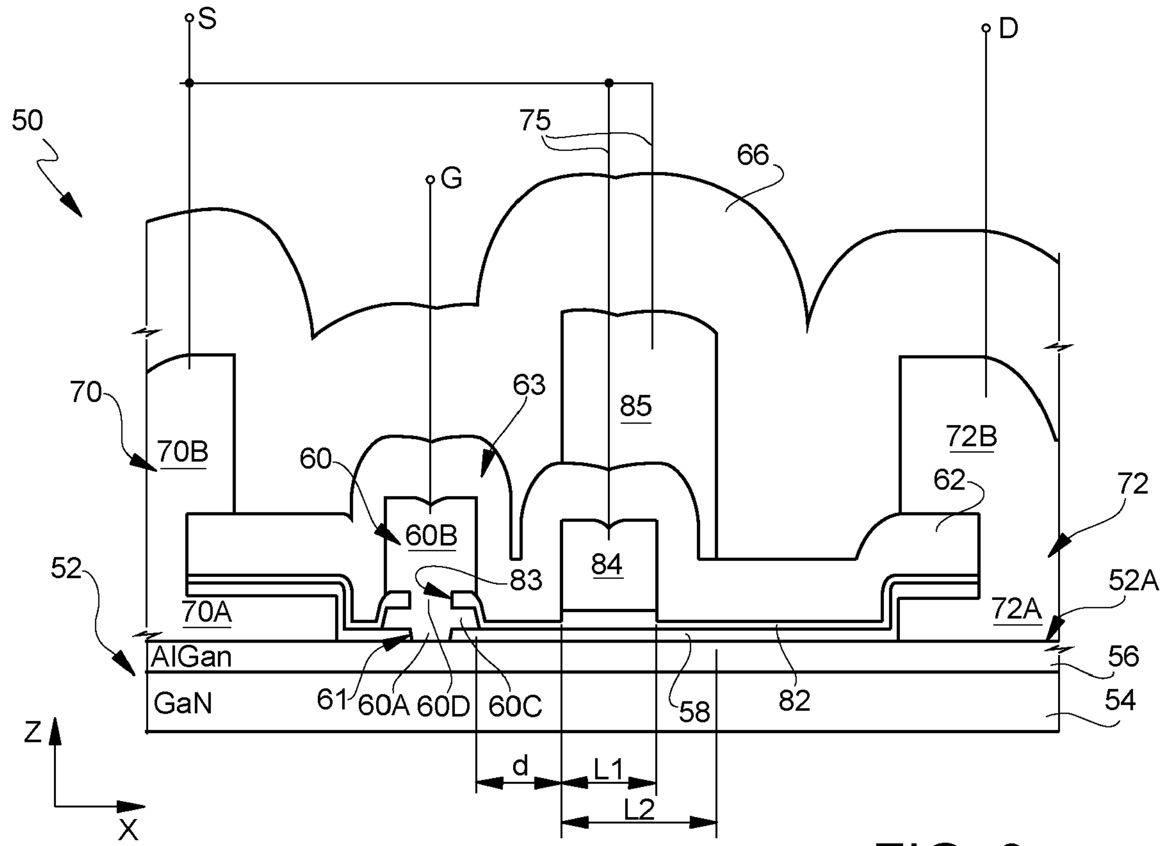

FIG. 3

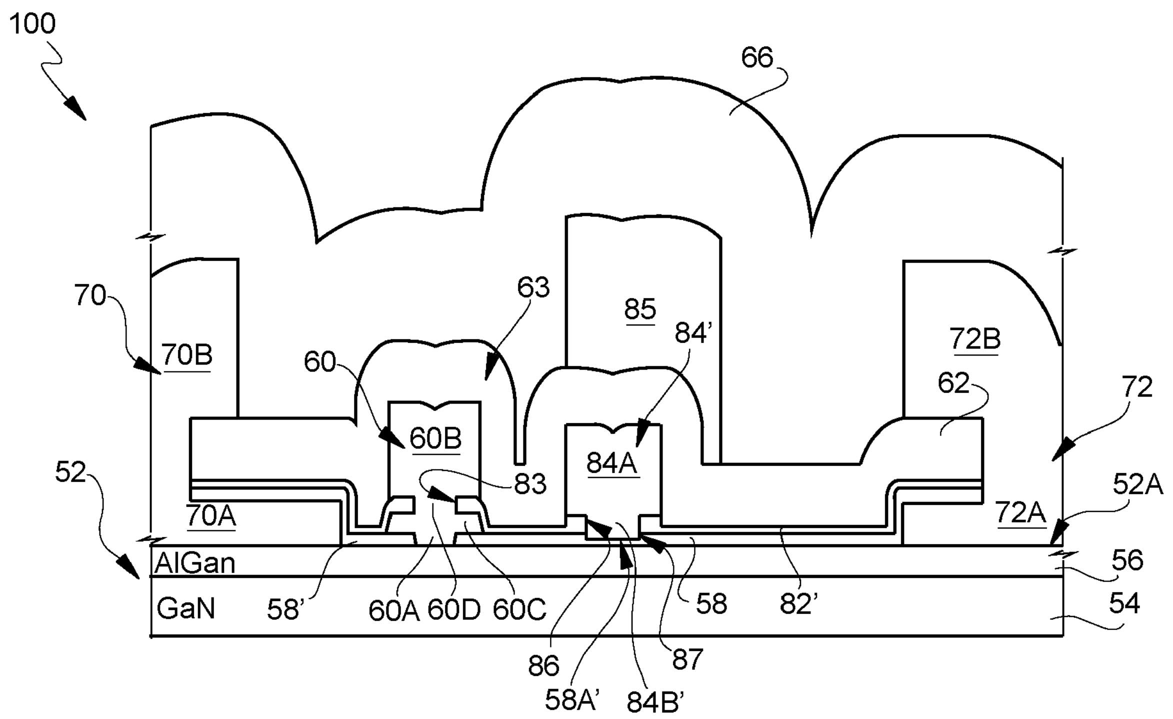

FIG. 4

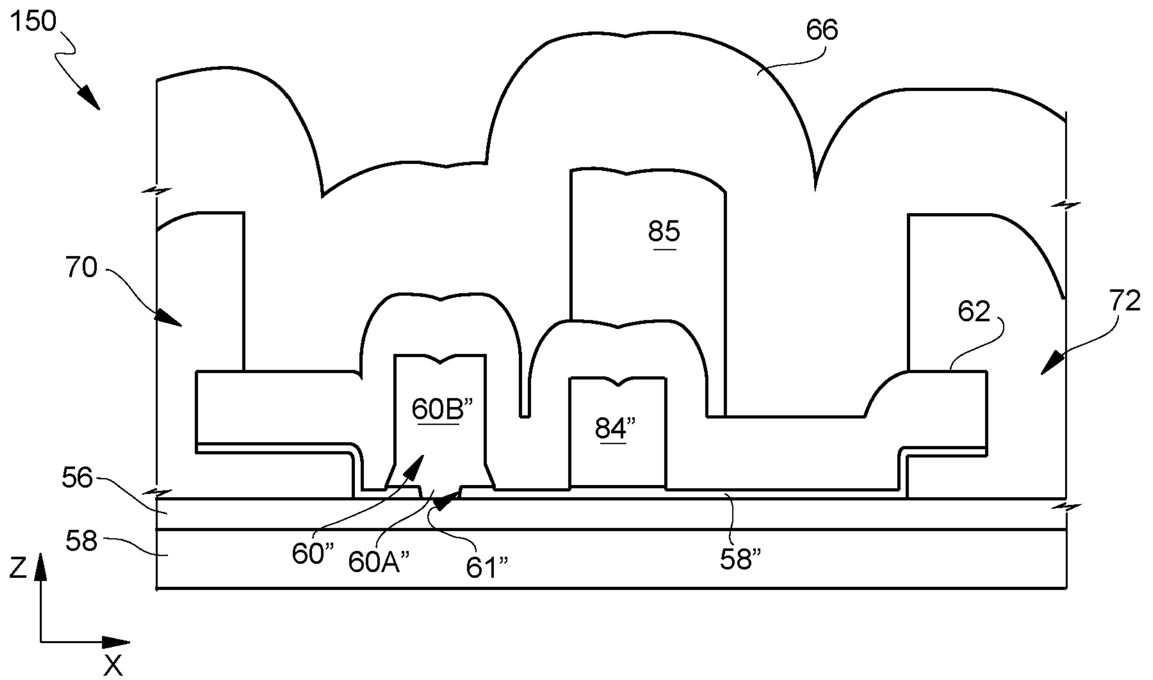

FIG. 5

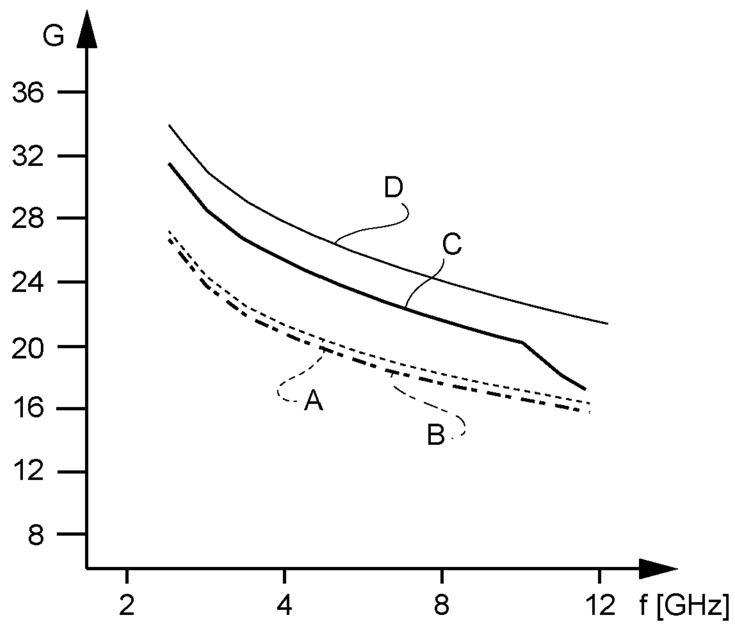

FIG. 8

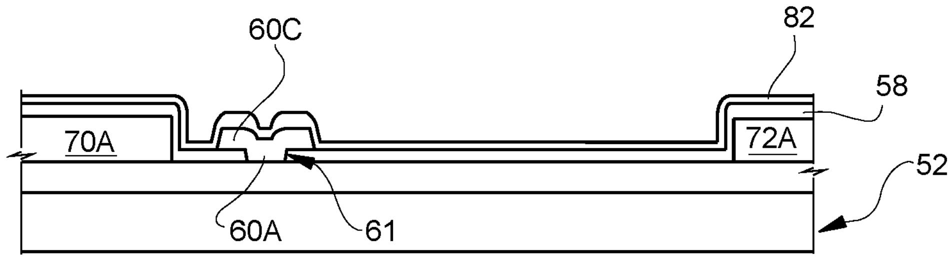

FIG. 6A

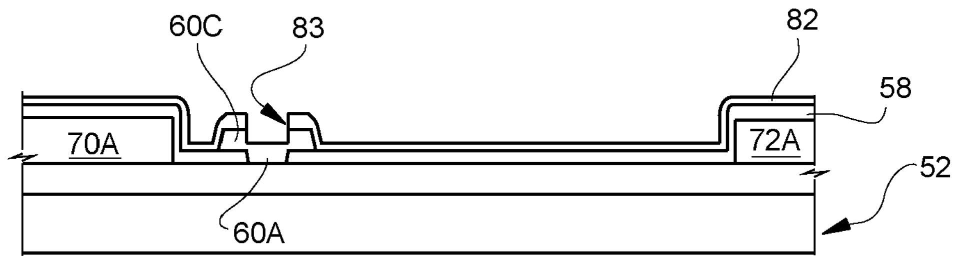

FIG. 6B

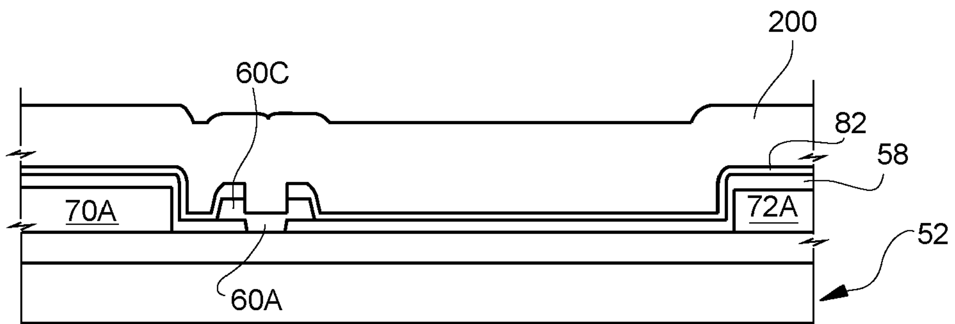

FIG. 6C

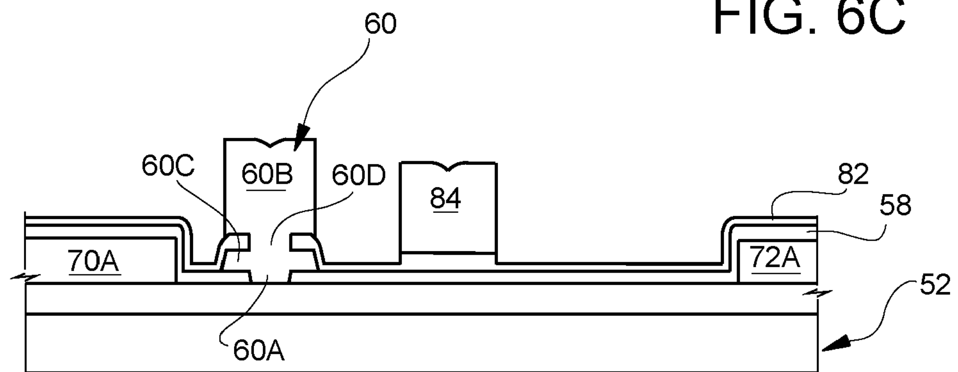

FIG. 6D

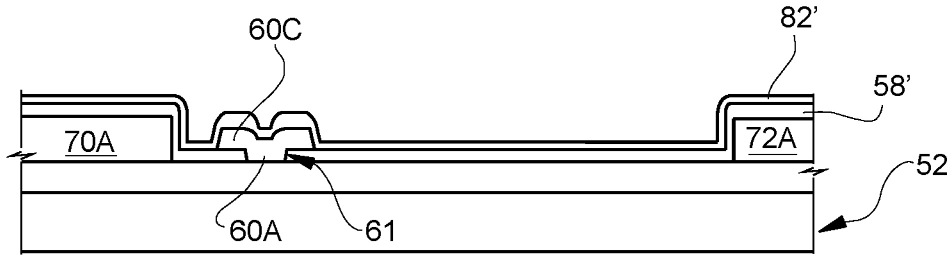

FIG. 7A

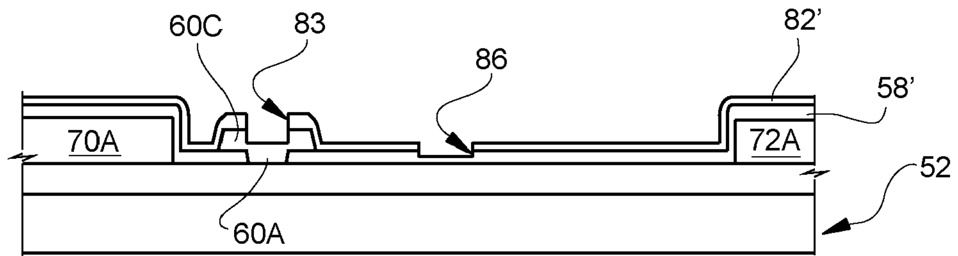

FIG. 7B

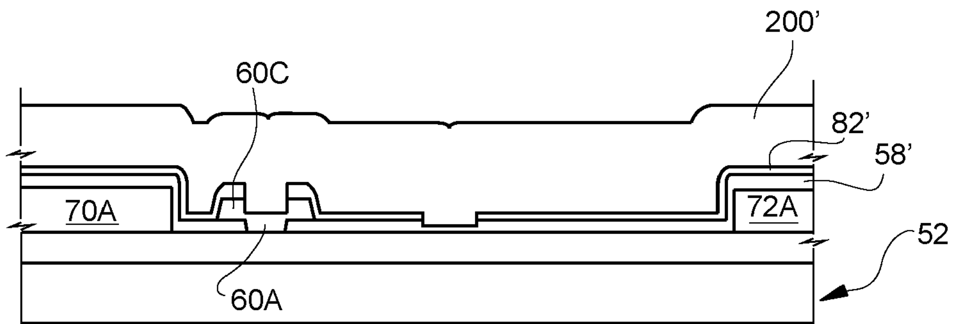

FIG. 7C

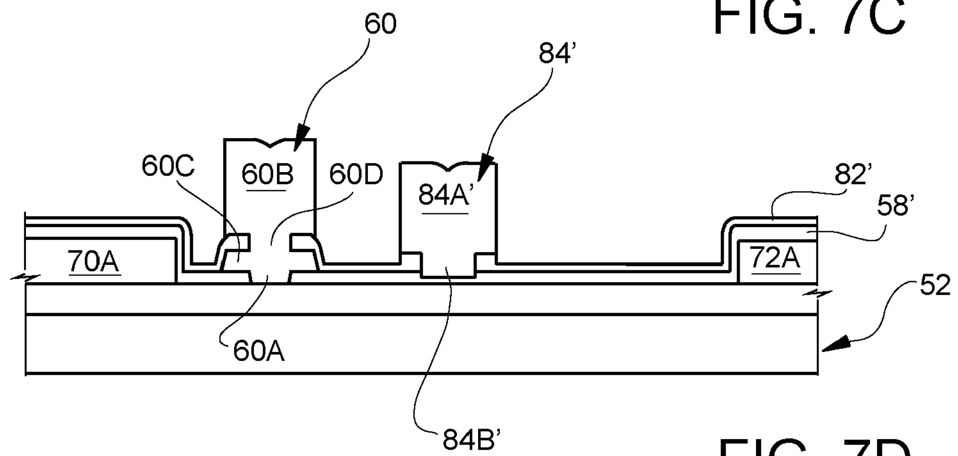

FIG. 7D

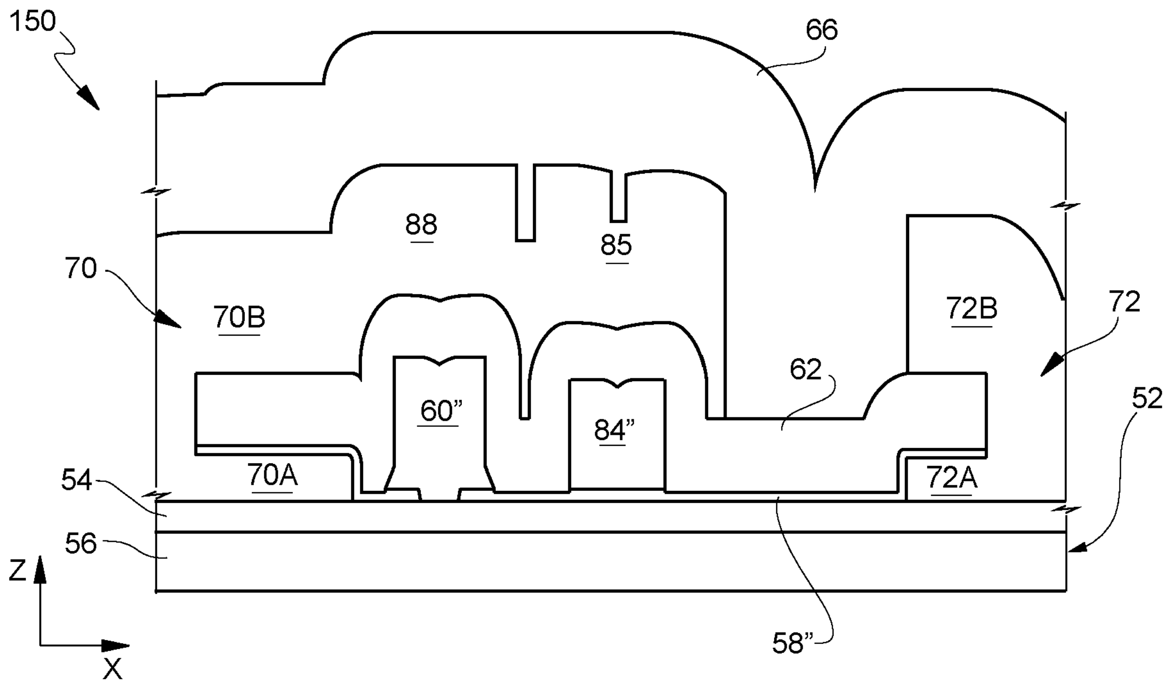

FIG. 9

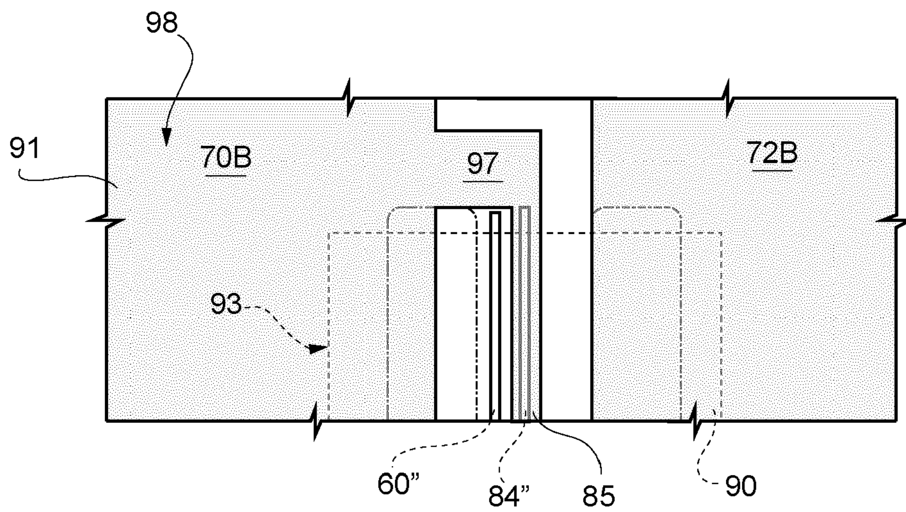

FIG. 10

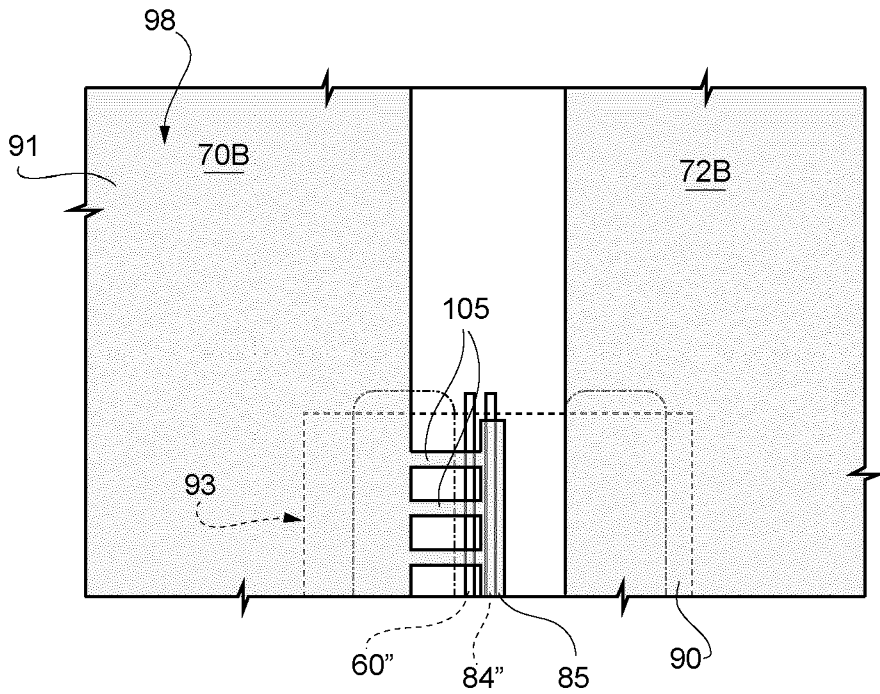

FIG. 11

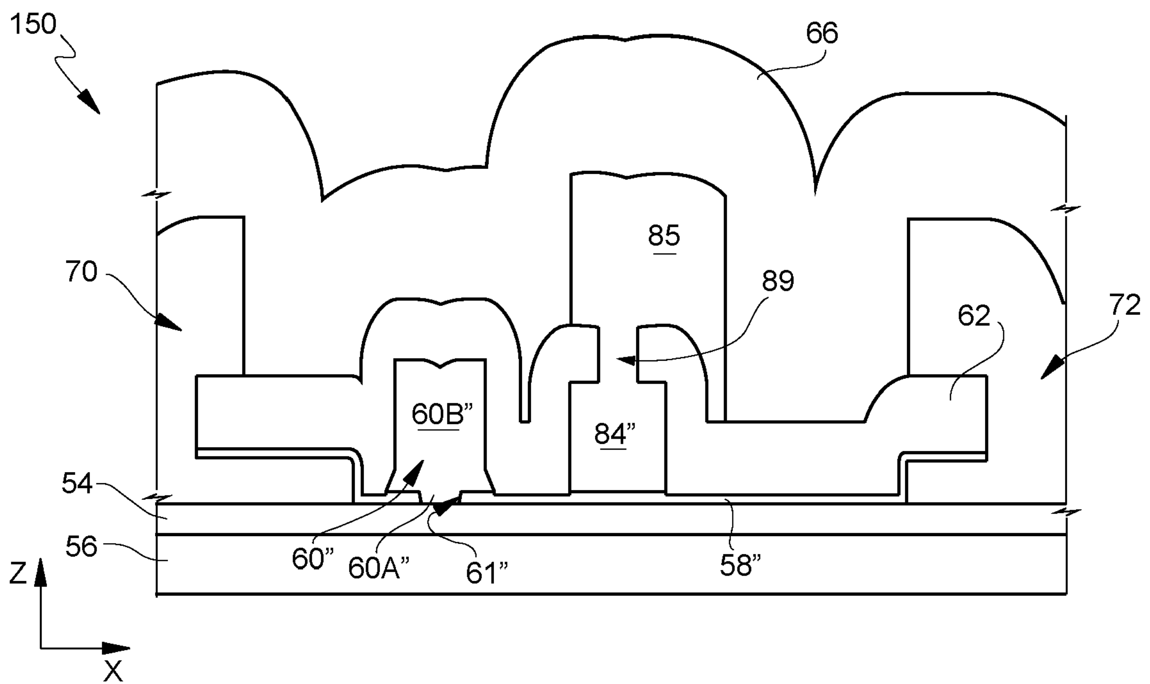

FIG. 13

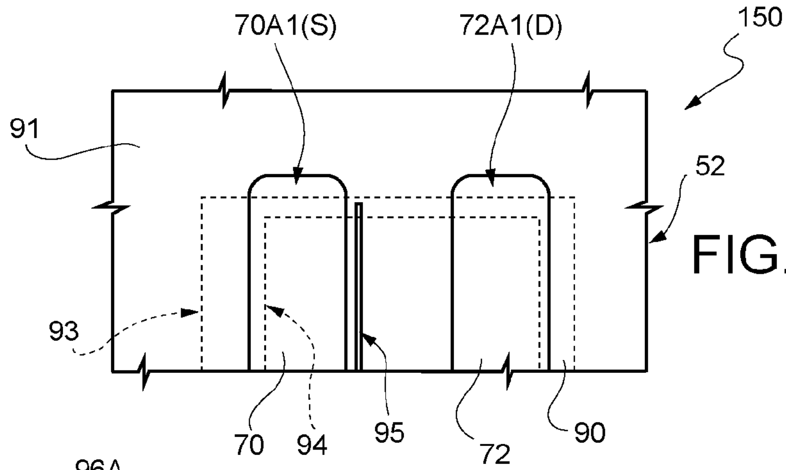

FIG. 12A

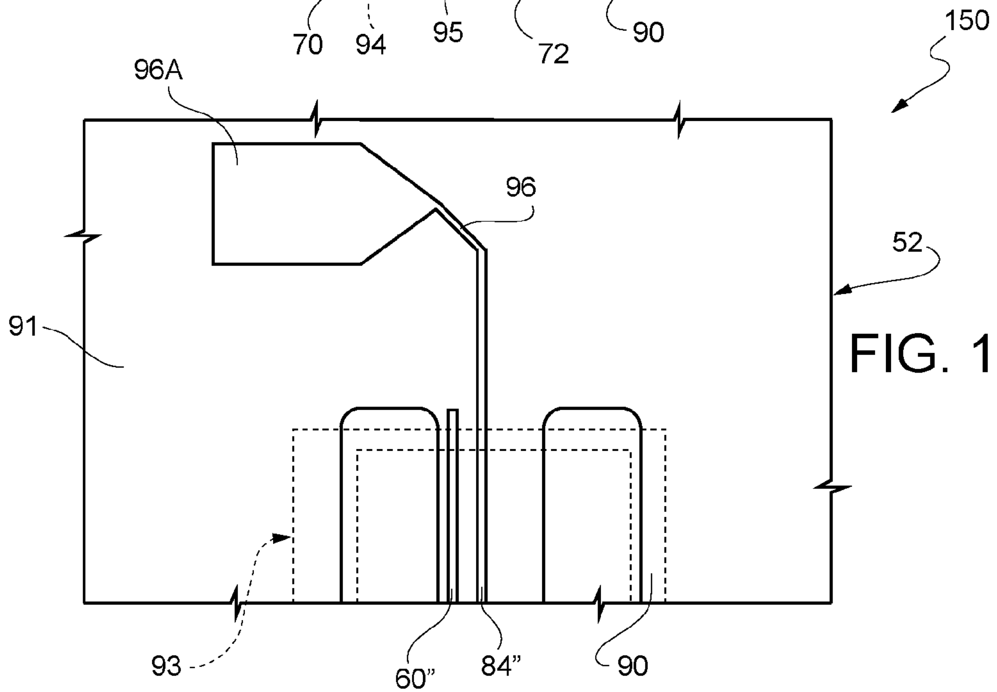

FIG. 12B

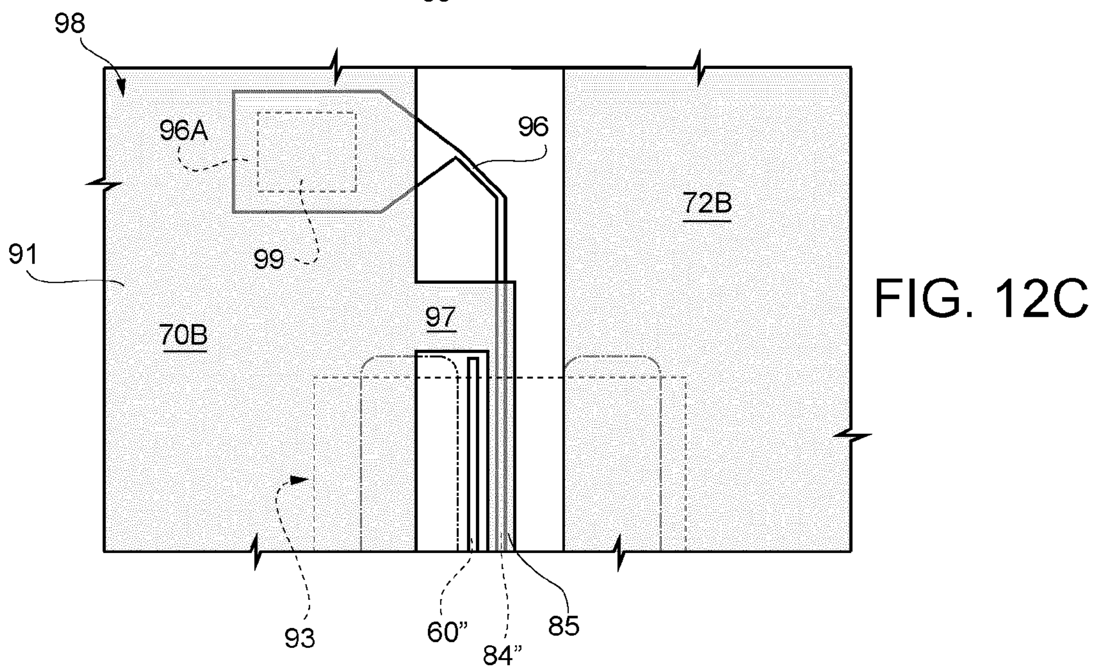

FIG. 12C

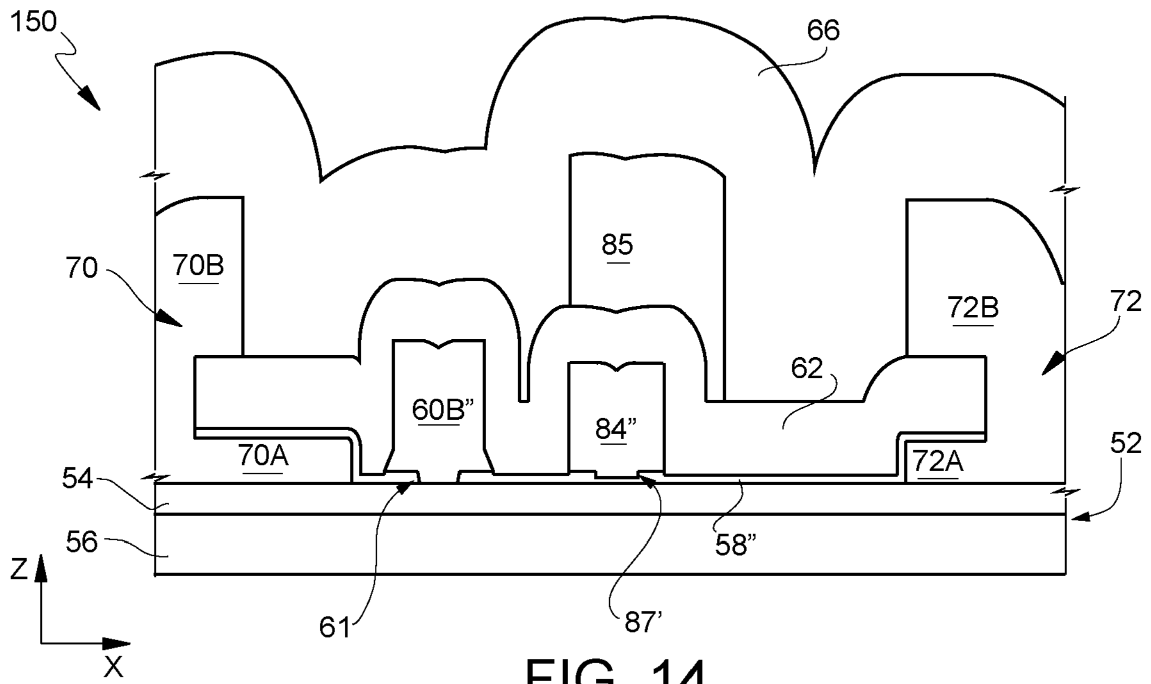

FIG. 14

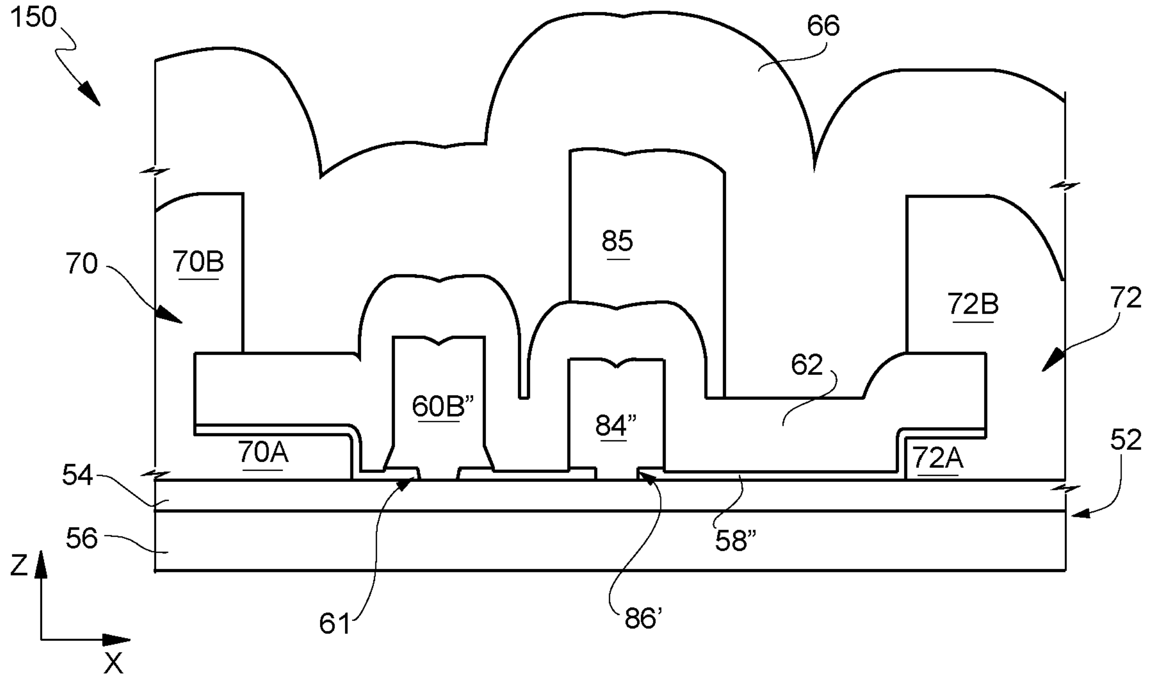

FIG. 15

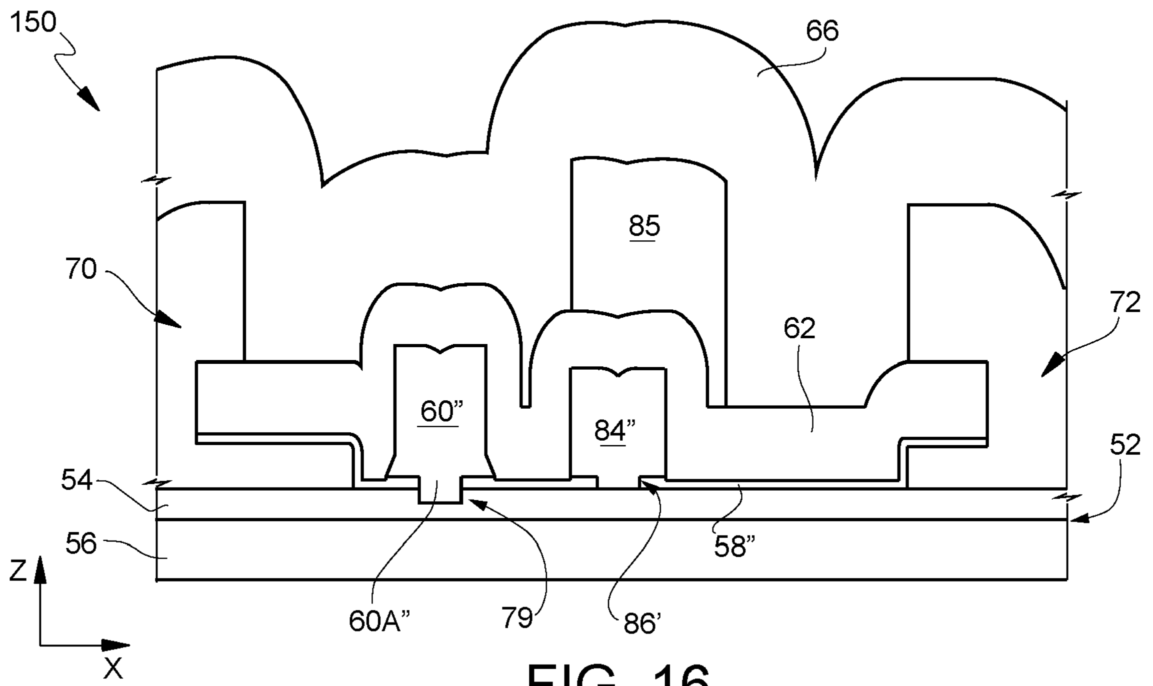

FIG. 16

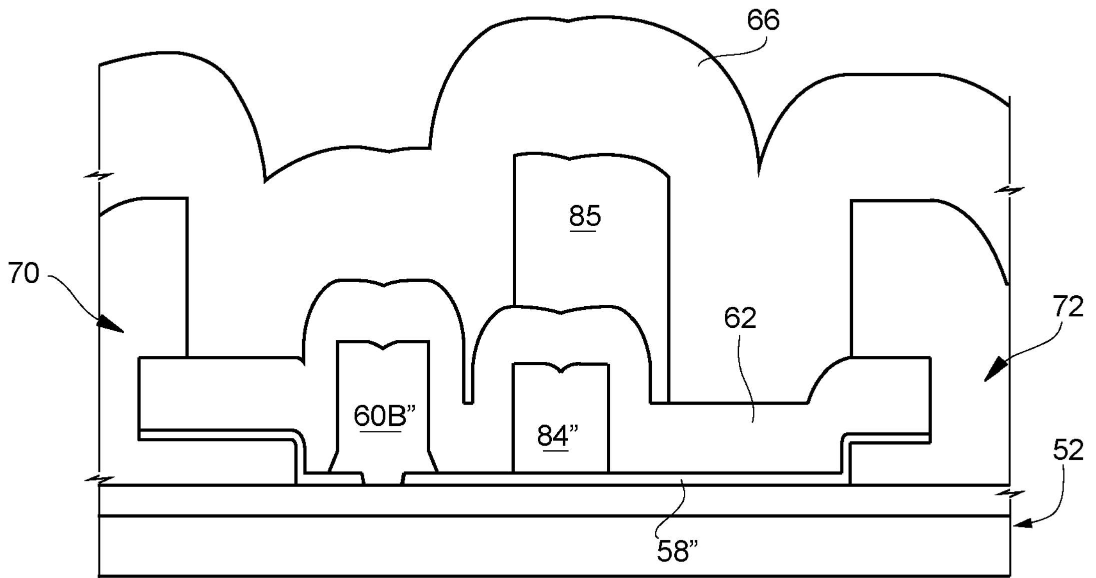

FIG. 17

EUROPEAN SEARCH REPORT

Application Number
EP 20 21 1345

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2017/294530 A1 (MOENS PETER [BE] ET AL) 12 October 2017 (2017-10-12) * figures 2-12 and associated text * -----	1-17	INV. H01L29/778 H01L21/338 H01L29/41 ADD. H01L29/423 H01L29/20

TECHNICAL FIELDS SEARCHED (IPC)

H01L

The present search report has been drawn up for all claims

1

Place of search	Date of completion of the search	Examiner
Munich	28 April 2021	Moehl, Sebastian

CATEGORY OF CITED DOCUMENTS

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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 20 21 1345

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28-04-2021

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2017294530 A1	12-10-2017	CN 207149559 U	27-03-2018
		US 2017294530 A1	12-10-2017

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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- EP 3660923 A1 **[0007]**
- IT 102018000011065 **[0013]**
- EP 3667735 A **[0013]**