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Single-phase series active power filter with transformer-coupled matrix converter

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Abstract: This study presents a series active power filter based on a single-phase matrix converter. Back-to-back voltage-source converters with nested control loops and passive filters are normally used for this application. A matrix converter, as proposed in this study, allows a simpler implementation both in terms of hardware (no grid filter and no DC link) and of control. Moreover, a novel zero-voltage compensation technique is introduced in order to reduce the distortion around the input voltage zero crossing. Simulations and experiments are used to validate the considered control methods, confirming the feasibility of the proposed architecture.

1 Introduction

Active power filters (APFs) are used to eliminate unwanted frequency components from power lines or sensitive loads. They were proposed in the 1970s, but they rose to mainstream utilisation only recently, thanks to advances in power electronics (with the emergence of fast and efficient power switches such as metal-oxide-semiconductor field effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs)) and microelectronics (with the advent of cheap and abundant embedded computing power in microcontrollers, digital signal processors (DSPs), field-programmable gate arrays (FPGAs)).

APFs can be divided into three main categories: shunt filters, series filters and unified power quality conditioners (UPQCs), that are the combination of a series and a shunt filter [1–3]. Shunt filters operate in parallel with the load and are usually employed to compensate the harmonics introduced by non-linear loads connected to the grid. They are generally very efficient due to the fact that they need to draw only the unwanted current components. On the other hand, series filters carry the whole load current but are more versatile, being able to operate on the fundamental as well as on the unwanted harmonic components [4]. They are employed to protect sensitive loads in polluted grid scenarios [5].

Series filters need galvanic isolation between the converter and the power line in order to avoid short-circuit paths. Isolation is usually achieved using a transformer, either inside the converter (high-frequency transformer) or at the output of the converter (line frequency transformer) [6–9].

The goal of eliminating unwanted harmonic components can be logically divided into two tasks: detecting the unwanted components and filtering them out. Some authors stress the importance of the detection stage to the overall performance of the filter [9–11] while, in most other cases, a closed-loop architecture makes it difficult to separate detection from filtering [12–16].

Several solutions can be found in the existing literature for the control of APFs. Many authors use variations of the synchronous reference frame or d–q transform control with the attractive feature of controlling constant quantities in steady state. In [17], a d–q controller is enhanced with the use of an adaptive pole placement technique for optimal control. In [18], the d–q control is applied to a current-source inverter (CSI) that ensures rapid control response and intrinsic short-circuit protection, but can result in lower efficiency with respect to voltage-source inverters (VSIs).

A similar approach considers the use of the instantaneous active and reactive power theory (p–q control) to control active filters [19]. Also, in this case the controlled variables are constant in ideal steady-state conditions.

Many solutions are based on proportional–integral (PI) or PI–derivative controllers, with different tuning approaches. In [14], artificial neural networks (ANNs) are used. Linear control theory is used in [15] through Bode diagrams to tune the controller of a single-phase shunt active filter, and in [16] through the Routh criterion to determine the stability bounds.

Furthermore, some researchers are applying predictive controllers (PCs) to APFs. PCs promise the fastest dynamic response but are very sensitive to parameter drift [13, 20]. A safer alternative with fast dynamic response is hysteresis controllers. In addition to being less sensitive to parameter variations, hysteresis controllers have intrinsic peak current limiting capabilities, a feature that is generally lacking in PCs [21]. In [2], the authors propose a solution in which a hysteresis controller drives a UPQC with series capacitors that enable operation with reduced DC-link voltage.

The possibility to reduce, or even to eliminate, DC energy storage components is very appealing, since the DC-link capacitor is among the weakest and most reliability-critical components in an electronic power converter. Among the converter architectures operating without DC-link capacitors, some researchers are studying the use of matrix converters (MCs) in APFs for both three-phase [5, 22] and single-phase applications [23].

MCs were first proposed in the 1980s, but viable real-world applications took long to take off since, even to this day, some technological challenges remain, such as non-ideal commutations of the power devices and the consequent voltage and current distortions [24]. MCs can connect any input line to any output line through bidirectional switching devices, and their main advantage is the elimination of the reactive components used for energy storage (line inductors in CSIs, bus capacitors in VSIs) [25].

This paper employs a series active filter, based on a single-phase MC (SPMC), to protect sensitive loads from the effects of voltage disturbances at the point of common coupling. The SPMC feeds a step-down transformer connected in series with the load. The voltage waveform inserted by the transformer is added to the distorted grid voltage, obtaining a pure sinusoidal voltage waveform across the load. The use of a step-down transformer allows to employ power switches with lower current ratings, while the series connection enables a limited control of the fundamental voltage amplitude. The key advantage of this solution is that, with respect to a back-to-back converter (Fig. 1*a*), it requires less passive components (the grid side inductor and DC-link capacitor)

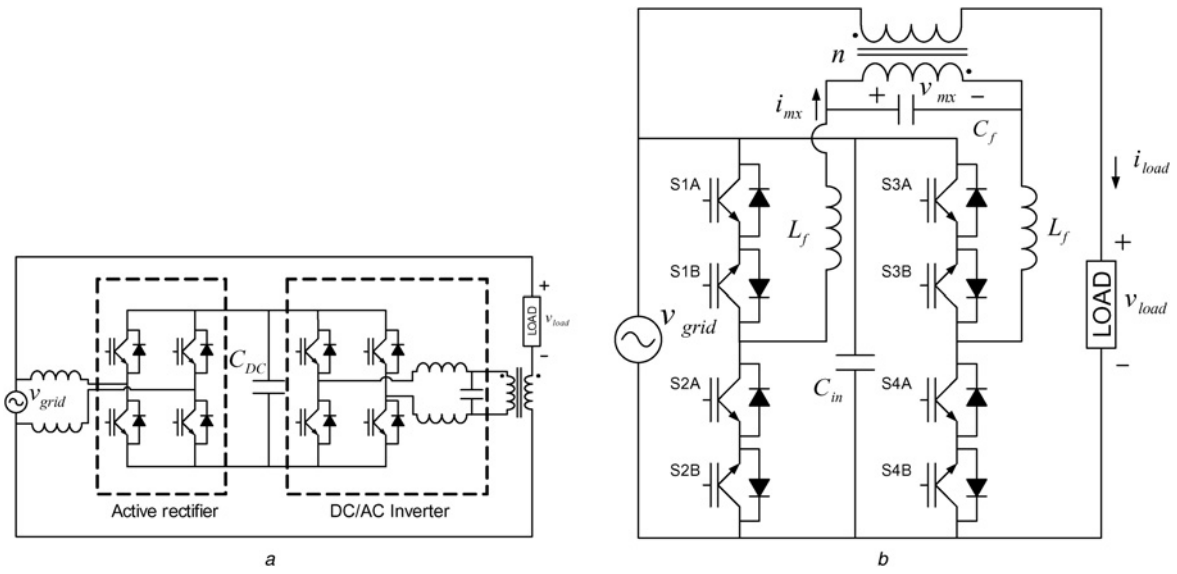

Fig. 1 *Active filter topologies*

a Back-to-back single-phase series active filter
b Topology of the proposed active filter

and a simple control is sufficient. Moreover, with the proposed modulation strategy, no current sensors are needed. Instead, a back-to-back converter requires a fast grid current control and DC-link voltage control [26]. The drawback of the MC solution is the reduced compensation capabilities due to the absence of a stable DC voltage. Moreover, the input current quality of the MC is inferior, since the back-to-back converter can absorb sinusoidal current [27].

The topology adopted in this work was already proposed in literature [23] for the protection of sensitive loads from fast grid voltage variations (i.e. voltage sags and swells) and harmonic pollution. Nevertheless, the strategy in [23] did not involve a closed-loop control: the voltage waveform to compensate the distorted grid voltage was calculated by subtracting the desired load voltage v_{load} from the sampled grid voltage v_{grid}. This method is very fast to compensate voltage sags or swells, but the harmonics rejection accuracy can be poor, since all the control variables are extracted from the input grid voltage and no feedback is provided from the load. Moreover, the control is sensitive to variations of the system parameters, since they cannot be compensated as with closed-loop controls.

In [28], the same control strategy proposed in [23], but with a different pulse-width modulation (PWM), is implemented to compensate only the harmonic distortion of the grid voltage. In this case, a low-pass filter (LPF) in the d–q reference frame is employed to detect the fundamental component v_{grid} of the grid voltage, which is then subtracted from the polluted grid voltage to generate the compensating waveform.

In this paper, the active filter's performance is enhanced by a harmonic closed-loop compensator based on the fast Fourier transform. Furthermore, a zero-voltage compensation strategy is proposed to reduce the output voltage distortion that occurs in SPMCs in correspondence with the input voltage zero crossing.

A version of this paper appeared in the proceedings of the IEEE IECON 2013 conference [29]. This paper is better organised, describes the control strategy in detail, presents a thorough review of the state of the art, reports further experimental results and proposes a novel PWM technique that allows removing the output current sensor.

The paper is organised as follows. Section 2 describes the proposed converter and the control strategy. Section 3 describes the PWM technique and the zero-voltage compensation strategy, comparing the adopted control techniques with the previous works proposed in literature. The following sections describe and discuss the simulations and experiments used to validate the proposed system; the last section reports the concluding remarks.

2 Active filter control strategy

The proposed circuit is shown in Fig. 1*b*. Every bidirectional switch consists of two IGBTs in series, with the emitters in common, driven by the signals SxA and SxB. L_{f}, C_{f} constitute the output filter for rejecting the high-frequency harmonics introduced by the modulation, whereas C_{in} is the input filter capacitor.

The input filter of a MC represents a non-trivial design topic, since it must be ensured that the high-frequency current harmonics generated by the converter do not pollute the grid voltage or current. For this reason, in a three-phase MC, an inductor–capacitor (LC) filter is normally adopted, and particular care is taken to avoid resonance (by adding a resistor in parallel with the inductor) [30]. Considering a single-phase application, and that normally the transformer of the APF is designed with a turn ratio smaller than one, effectively reducing the input current, for this application a single capacitor at the input is adopted. This solution proved to be satisfying even considering a wide range of line impedance values.

The block scheme of the APF control is shown in Fig. 2. The load voltage is processed by an array of harmonic compensators, and the result is the MC voltage set point, v^*_{mx}. To generate the correct output voltage, a duty cycle m for the MC is computed dividing the voltage

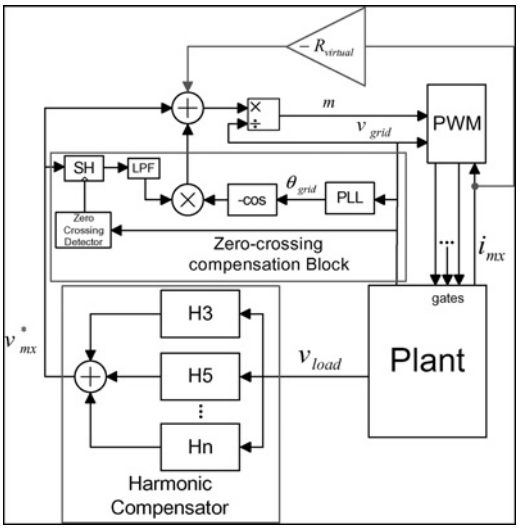

Fig. 2 *Block scheme of the control*

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set point by the input voltage, $m = v^*_{mx}/v_{grid}$. The PWM block generates the correct switching sequence for the converter, as will be thoroughly explained in the following section.

Regarding the harmonic detection algorithms, several solutions are present in literature. In the following, the most relevant will be briefly described, and then a choice will be made.

In [31], the instantaneous reactive power (IRP) theory is used; in a three-phase system transformed in $\alpha\beta$ coordinates, the average of the instantaneous power is related to the fundamental frequency, while the oscillating part corresponds to the harmonics. In [11, 32], the harmonics are separated in the d–q current frame, so that the fundamental components assume DC values and can be easily isolated with low-pass filtering. A modified approach that uses the decomposition of multi-phase voltage vectors to represent different power components is presented in [9].

A further possibility is to use an array of adaptive second-order generalised integrators [33] and isolate the harmonics of the output voltage. Unfortunately, given the limited frequency separation between the grid harmonics, very narrow bandwidth must be ensured for this solution, triggering potential numerical stability problems. A straightforward solution is to perform the discrete Fourier transform (DFT) of the output voltage. As a matter of fact, this method allows to obtain the coefficients of the Fourier series with an extremely high rejection of the other harmonics. In [34], the Fryze–Buchholz–Depenbrock power theory was proposed. This theory states that a utility-connected load that absorbs non-sinusoidal currents can be decomposed into conductance and susceptance at the different harmonics. Once these values are calculated, it is possible to isolate the harmonics via low-pass filtering. ANNs [35] were also employed to detect harmonics in power systems. Kalman filters (KF) can also be adopted for this kind of operation.

The aforementioned compensation strategies were evaluated in [36]. Each solution presented good harmonic rejection capabilities, in particular the KF and the DFT methods presented similar accuracy, with the KF being more sensitive to measurement noise. The IRP and the d–q decomposition are suitable only for single-phase systems. While the DFT is apparently the most demanding methods in terms of computation and memory requirements, the recursive DFT (RDFT) can replace the DFT in real-time applications and obtain the same accuracy. Considering the extensive work present in literature, and limiting the choice to single-phase and low-cost systems, it is the opinion of the authors that the RDFT represents the best solution, being more robust than the KF with high noise and demanding less computational power than the ANN approach. The only drawback is the increased working memory needed to store the old samples.

Considering the circuit in Fig. 1*b*, it is possible to obtain the simplified model of the system as shown in Fig. 3*a*. The voltage generator v_{mx} simulates the MC output voltage, and impedance Z_1 represents the matrix output filter inductor plus the transformer leakage inductance. Z_m takes into account the magnetising inductance of the transformer

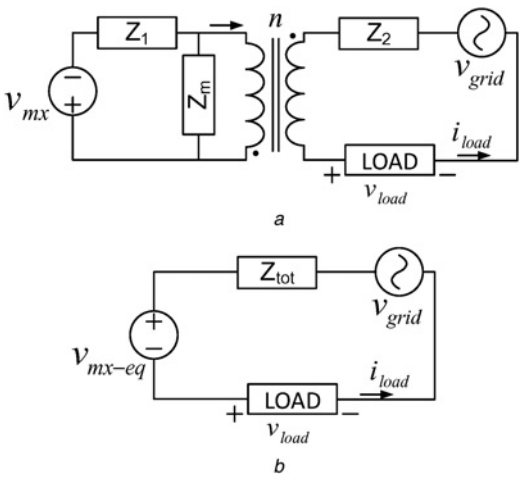

Fig. 3 *Simplified system model and Thevenin equivalent circuit of the system*

a Simplified system model
b Thevenin equivalent of the system at the low-voltage side of the transformer

and Z_2 mainly represents the transformer leakage inductance at the low-voltage side (grid side). For the analysis, the output filter capacitor and the transformer capacitance were not taken into account, since only the low-frequency behaviour of the circuit was considered. The equivalent Thevenin circuit of the system, at the low-voltage side of the transformer, is depicted in Fig. 3*b* and the system equations are given in the following equation

$$\begin{cases} v_{\mathrm{m-eq}} = \dfrac{v_{\mathrm{mx}} Z_{\mathrm{m}}}{n(Z_1 + Z_{\mathrm{m}})} \\ Z_{\mathrm{eq}} = \dfrac{Z_1 // Z_{\mathrm{m}}}{n^2} \\ Z_1 = R_{\mathrm{f}} + s(L_{\mathrm{f}} + L_1) \\ Z_2 = R_2 + sL_2 \\ Z_{\mathrm{m}} = sL_{\mathrm{m}} \\ Z_{\mathrm{tot}} = Z_2 + Z_{\mathrm{eq}} \\ I_{\mathrm{load}} = \dfrac{V_{\mathrm{load}}}{R_{\mathrm{l}}} \\ V_{\mathrm{load}} = (V_{\mathrm{grid}} - v_{\mathrm{m-eq}}) \dfrac{R_{\mathrm{l}}}{(R_{\mathrm{l}} + Z_{\mathrm{tot}})} \end{cases} \tag{1}$$

In the RDFT scheme, the harmonics of v_{load} are isolated by DFTs tuned at different frequencies. PI controllers on the in-phase and quadrature components of the DFT allow infinite gain at the harmonic frequencies (Fig. 4). It is important to note that in Fig. 4 the

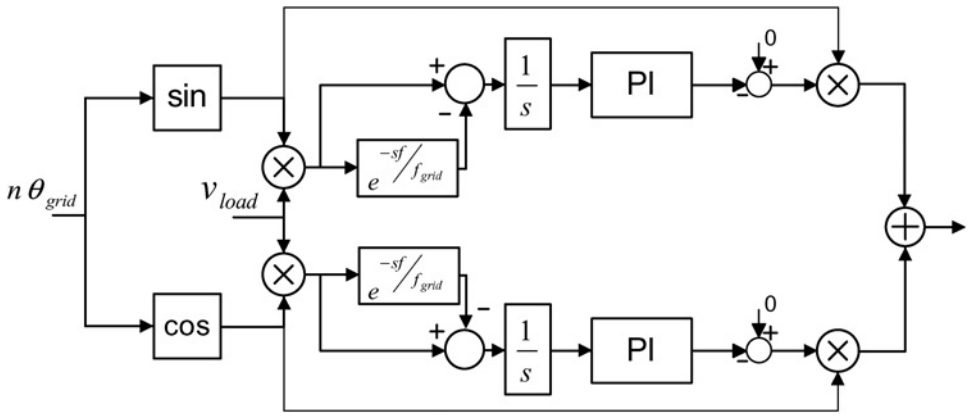

Fig. 4 *Block scheme of the RDFT harmonic compensator*

implementation of the RDFT window can be realised in a computational-efficient way with circular buffers. For completeness, it should be said that the scheme is very similar to a PI in a synchronous reference frame (with poles on the imaginary axis). The use of the moving average allows to completely decouple the different harmonics. In this case, H_f can be expressed as in (2), where a is the ratio between the proportional and integral gains of the controller

$$H_f = \sum_{n=3,5,7} K\left(\frac{2as}{s^2+(n\omega_0)^2} + \frac{2(s^2-(n\omega_0)^2)}{(s^2+(n\omega_0)^2)^2}\right) \quad (1/T_s(1-e^{-sT_s})) \tag{2}$$

Considering that the active filter must have satisfactory performance with arbitrary load, it must be made sure that particular load conditions do not cause resonance problems. While the non-linear and resistive/inductive load does not present particular challenges for the harmonic compensator, as will be shown in the simulations, a capacitive load can resonate with the converter's output filter. In this case, considering a purely capacitive load C_{load}, the transfer function of the output filter (from the output of the converter to v_{mx}) can be written as

$$H_{out} = \frac{L_m}{s^2 L_m L_f C_{load}/n^2 + L_f + L_m} \tag{3}$$

Obviously, considering that the transformer magnetising inductance is much larger than the output filter one, resonance between the filter inductors and the load can happen. A simple method to damp this resonance (and obtain a flatter filter output response) is simply to add a virtual resistor in series with the filter inductance (active damping), as in Fig. 2.

3 PWM and zero-crossing compensation strategies

As mentioned previously, single-phase MCs are particularly appealing for the possibility to downsize power electronics in AC/AC applications, due to the absence of DC bus capacitors. Nevertheless, they inherit some issues from their three-phase counterparts. In fact, the proper commutation of the bidirectional switches requires particular care, since no free-wheeling paths exist in a MC for the load currents. This means that the commutation from one bidirectional switch to another must happen avoiding both short circuiting the input voltages and opening the loads. Since this is a notorious problem also for three-phase MCs, many works exist in literature proposing different approaches to achieve safe commutations.

Furthermore, SPMCs are affected by another major issue: during the input voltage zero crossings the output voltage is inherently limited. This limitation leads to voltage distortion if the output voltage desired by the control is different from zero during the grid voltage crossover. The zero-crossing limitation affects only single-phase MCs; multiphase MCs are intrinsically immune [37, 38].

These two problems represent key issues for the control of single-phase MCs. They often occur simultaneously, but they are addressed separately in the following for clearer presentation.

3.1 Bidirectional switches commutation strategy

Different approaches are viable in order to achieve safe commutations of the bidirectional switches. With the knowledge of the voltage across the bidirectional switch or the direction of the current, specific switches can be appropriately gated in sequence to avoid dangerous situations.

The four-step current commutation is one of the most widely adopted solutions for three-phase MCs. With this scheme, information about the current flowing through the bidirectional switches is used to turn off the transistor whose antiparallel diode is conducting, thus preventing input short circuits [25].

In [39], an evolution of this technique is adopted for a SPMC operating as an AC/DC converter. Instead of the current through each bidirectional switch, the output current of the converter is used to choose the adequate switching sequence. This method can still lead to open load conditions in proximity of the current zero crossing, since errors in the sampled signals can always be present. This issue is normally addressed by a specific clamp circuit offering a free-wheeling path for the output current.

A similar four-step switching sequence can be realised with the information of the voltage across the bidirectional switches. Differently from the previous case, three devices are gated in specific time intervals. The short circuit is avoided by gating devices with a series diode that cannot be turned on. This is the method used in [28], where the sign of the input voltage (i.e. the grid voltage) is taken as reference for the commutation sequences. It is worth to be noted that in [28] all the driving signals are disabled during a narrow window around the input voltage zero crossings, in order to avoid possible short circuits due to measurement errors or to a change of the input polarity.

A hybrid approach was pursued in [29]. If the information of the grid voltage is considered reliable, i.e. above a certain threshold, voltage-based commutation is used. Otherwise, the bidirectional switches commutate with the current sequence. Due to the fact that the SPMC feeds a transformer, the magnetising current should create a sufficient phase displacement between voltage and current to allow proper commutation. If both the current and the voltage are below the threshold that allows a safe commutation, current commutation is preferred. Open load situations are then addressed by the use of small RC snubbers. The presence of the snubbers is justified also by the fact that they prevent overvoltages due to the stray inductance of the tracks. The principal drawback with respect to [28, 39] is the need for two sensors: one for the input voltage and one for the SPMC output current.

In this work, the PWM strategy is further simplified by using a different approach when the voltage measurement is unreliable. When the input voltage is very low, the output voltage capability of the MC is obviously limited; for this reason, as a simplification, the MC can be driven in order to generate a null voltage output by turning on S1A-S1B-S3A-S3B (or S2A-S2B-S4A-S4B), as in Fig. 1*b*, thus short circuiting the output. The MC remains in this state as long as the modulus of the measured input voltage stays below a certain threshold (e.g. the maximum variation of the input voltage that can happen over a switching cycle).

The above strategy is shown in Fig. 5*a* that reports the gate signals of one leg during a transition of the input voltage with negative derivative. The other leg behaves in a similar way. The four-step commutation restarts when the input voltage reaches the threshold again.

To evenly distribute the commutation stress among the devices, during the positive derivative intervals of the input voltage zero crossing the low-side devices can be used instead of the high-side ones. In this way, the PMW control sequence technique requires only one sensor, as in [28, 39]. It is worth to be noted that this method appears similar to that proposed in [23], but differs from it in a key point. In [23], a bidirectional switch was driven by only one signal, and no information was reported about how to avoid short circuits.

3.2 Input voltage zero-crossing compensation strategy

Differently from a three-phase MC, in a SPMC during input voltage zero crossings the output voltage is inherently limited. This limitation results in load voltage distortion if the SPMC output voltage needed for harmonic compensation is different from zero during the grid voltage zero crossing. The converter simply cannot synthesise the desired output voltage around v_{grid} zero crossings.

A possible solution is proposed in this paper. Under the hypothesis of odd harmonics compensation, a suitable signal can be added to v^*_{mx}, in order to make its zero crossings coincide with the input voltage zero crossings. If the operating voltage of the load can be moved around a sufficiently wide window of rms value, a first harmonic can be added to v^*_{mx}, slightly modifying the amplitude of the first harmonic of v_{load}.

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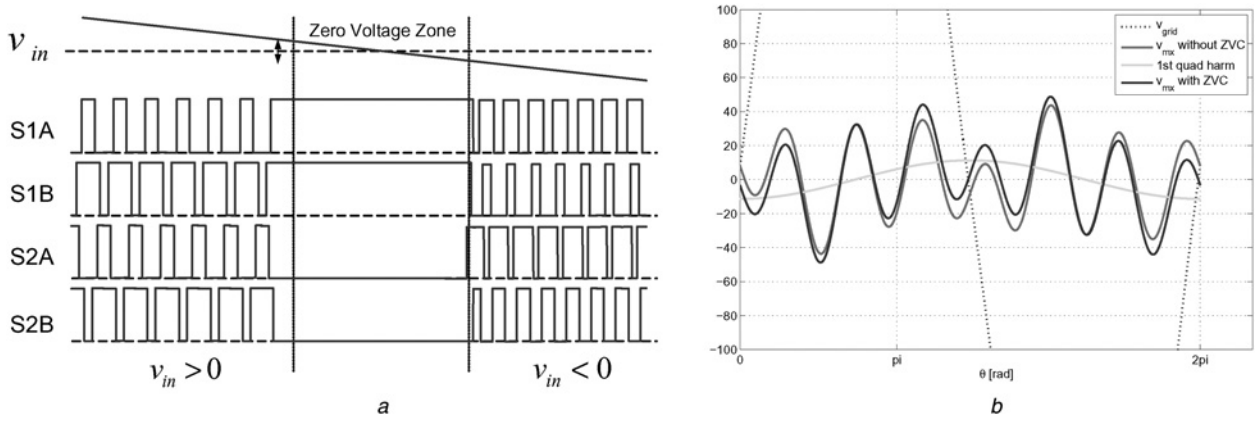

Fig. 5 *Zero-crossing issue*

a Modified PWM strategy during the zero crossing of the input voltage
b Waveforms of the zero-voltage compensation

A serious drawback of this solution is that the load voltage amplitude and phase are modified, limiting its applicability to phase sensitive loads. The quadrature signal is the one that allows to partially compensate the zero-crossing distortion with the minimum change to the rms value of the fundamental. Considering that the SPMC's output is constrained to the input voltage, it must be considered if the benefits of a better total harmonic distortion (THD) overcome the phase displacement issues.

If it is known that the most important operating point coincides with a condition where the SPMC must output a voltage different from zero at the input voltage zero crossing, a specific tuning of the LC filter can be used to prevent the intervention of the zero-voltage compensation (ZVC).

The block scheme of Fig. 2 shows that the output of the harmonic compensator is sampled at one of the zero crossings of the grid voltage. This value is then fed through a LPF with a very slow time constant. The output of the filter is the amplitude of the first harmonic in quadrature with the grid voltage which is then added to the harmonic compensator's output v^*_{mx}. If only the odd harmonics need to be compensated, the resulting v^*_{mx} is zero at both zero crossings of the grid voltage. This is illustrated in Fig. 5*b*, where the system behaviour is shown with and without the zero-crossing compensation strategy.

4 Stability analysis

Stability and robustness analyses were performed in order to prove the correct operation of the proposed control strategy. The virtual resistor effect is taken into account in the stability analysis. To this aim, it is important to note that the virtual resistor contribution is affected by a delay due to the sampling. This actually modifies the equation of Z_1.

The effect of the ZVC is more complex because it is heavily non-linear. To simplify the analysis it can be observed that the procedure of sampling the regulator's output and adding a sinusoidal signal can be modelled as a low-pass filtering discretised at the grid frequency (ZVC(s)). As a consequence, the closed-loop transfer function of the SPMC acts as a high-pass filter. The equations are reported in (4).

For $a = K_p/K_I = 1/6$, $K = 15$ the system is stable and presents an infinite gain at the selected harmonics

$$\begin{cases} Z_1 = R_f + s(L_f + L_1) + \dfrac{R_v}{1.5s/f_{sw} + 1} \\ \text{ZVC}(s) = \dfrac{1}{1.5s/(f_{grid}) + 1} \dfrac{1}{s/(2\pi f_{cut}) + 1} \\ v'_{mx(s)} = v_{mx} \dfrac{1}{1 + \text{ZVC}(s)} \end{cases} \quad (4)$$

Fig. 6 shows the Nyquist diagram results for the RDFT harmonic compensator in the different conditions. In Fig. 6*a*, the diagram is shown for the nominal conditions without the ZVC. The converter is considered ideal, i.e. the voltage limitations are neglected. In Fig. 6*b*, the ZVC and virtual resistor are added. As a matter of fact, for a resistive load, the addition of the virtual resistor has no effect. Even the introduction of the ZVC, despite its slow dynamic behaviour, has no effect on system stability.

The robustness analysis was conducted by changing the output inductance (half the nominal value). As can be seen from Fig. 6*c*, with the chosen parameters the effect on the stability is negligible. Other parameters were also changed with very little effect. It should be said that a big difference of the SPMC with respect to the back-to-back inverter is that no current loops are present, because the SPMC acts intrinsically as a voltage generator. For this reason, parameters like the filter inductance and the load have little effect on the system stability.

To show the limits of the control, the value of K was increased in Fig. 6*d*. This modification heavily affects the phase margin and brings the system very close to instability.

5 Simulation results

The active filter and the proposed control strategies were simulated in the MATLAB/Simulink environment with the PLECS toolbox. The circuit in Fig. 1*b* was implemented with the simulation parameters of Table 1. Third, fifth and seventh harmonics were added to the 50 Hz fundamental component of the grid voltage, obtaining the expression (5). The resulting input THD was 5.3%. The load was represented by a resistor R_l

$$v_{grid} = 230\sqrt{2}\sin(\omega t) + 10\sin(3\omega t + 3\pi/10) + 10\sin(5\omega t) - 10\sin(7\omega t) \quad (5)$$

Several simulations were performed in order to study the performance of the MC and the control strategy. In particular, the harmonic rejection capabilities of the RDFT controller were examined with and without the zero-voltage compensation strategy. The following simulation result figures show the grid voltage v_{grid}, the output voltage and current v_{load} and i_{load}, and the MC output voltage v_{mx}.

From Fig. 7 it is obvious that, without the ZVC, v_{mx} cannot follow the reference in proximity of the grid voltage zero crossing, deteriorating the harmonic rejection as a consequence. The simulated THD reaches the almost ideal value of 0.3% with the ZVC, while without the compensation the THD is 0.6%.

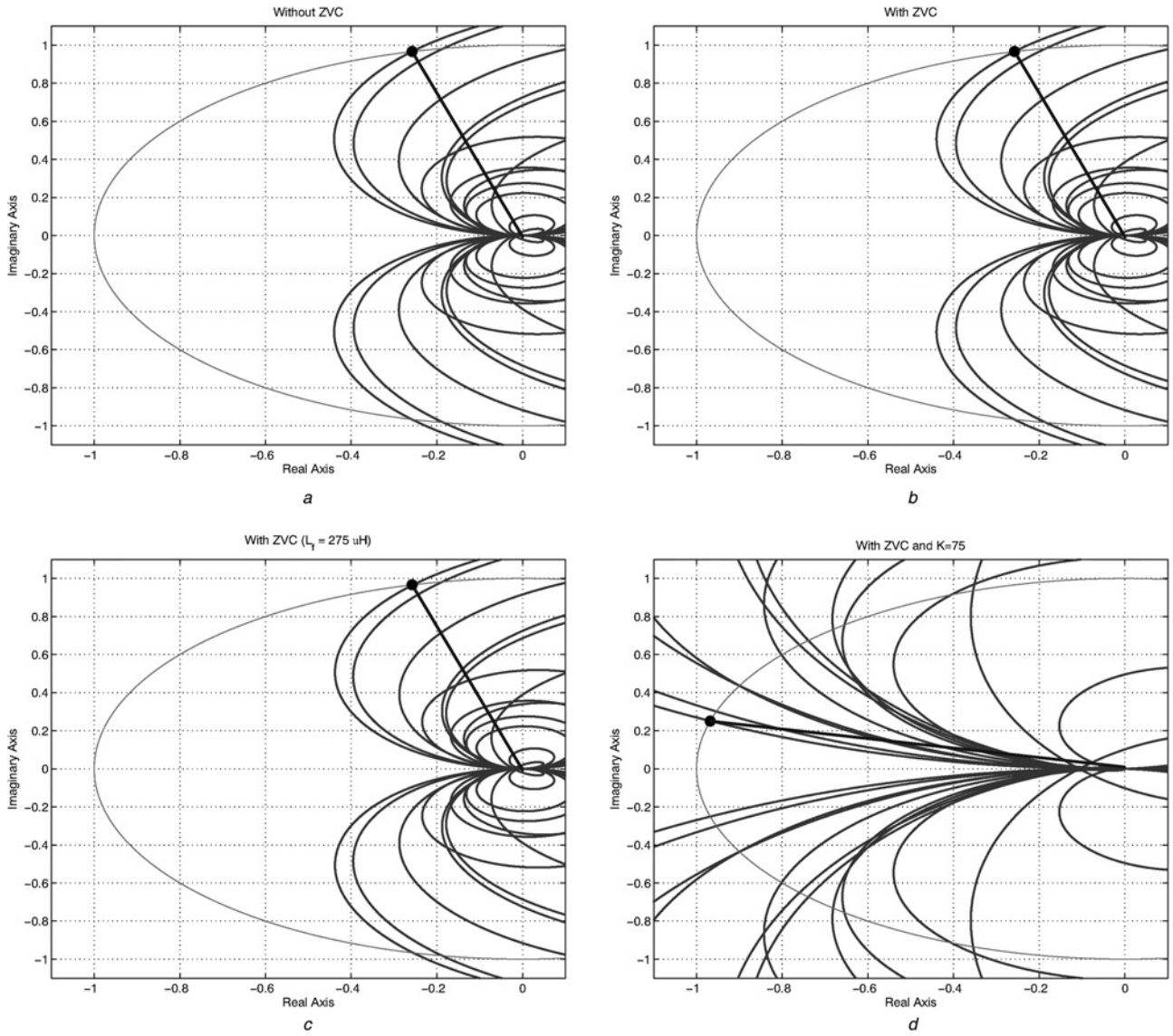

Fig. 6 *Stability analysis with RDFT harmonic compensator*

a H_{OL} without ZVC and virtual R, phase margin (PM) = 75°
b H_{OL} with ZVC and virtual R
c H_{OL} with ZVC, virtual R and low load
d H_{OL} with ZVC, virtual R and higher gain K, PM = 14°

Table 1 Simulation parameters

Name	Description	Value
v_{grid}	grid voltage	230 V rms
f_{grid}	grid frequency	50 Hz
f_{sw}	switching frequency	10 kHz
L_f	AC inductor filter	0.75 mH
L_m	Transformer magnetising inductance	120 mH
C_f	AC output capacitor filter	2.2 μF
C_{in}	AC input capacitor filter	2.2 μF
n	transformer turn ratio	2.8
R_l	load resistor	17 Ω

The simulations were repeated with different loads, with the same input harmonic distortion and ZVC enabled.

Fig. 7*c* shows the simulation results when a diode is inserted in series with the resistor $R_l = 17\ \Omega$. The performance still remains good, with a THD of 0.4%. It is worth noting that resonance problems of the LCL output filter can happen due to the current harmonics of the non-linear load. In this case, a simple solution, that does not require additional current sensors, is to put a resistor in series with the filter capacitor to passively damp the oscillations. From the simulations, values in the order of 1–2 Ω are enough to damp the resonance without implying excessive power losses (<1 W).

As explained in Section 2, a virtual resistor is added to damp the resonance with capacitive loads. The bode diagram of the output transfer function with the simulation parameters is shown in Fig. 8*a*, where a 3 kVAR load capacitor and a 2 Ω virtual resistor were employed. To implement this solution, however, a current sensor is needed at the output of the MC, increasing cost and complexity. The simulation results with this purely capacitive load are reported in Fig. 8*b*, where the output THD equals 0.6%. If the load is not purely capacitive, the intrinsic damping of the circuit should be enough to allow the operation of the active filter even without the active damping.

6 Experimental results

A prototype of the active filter was built to test the modulation strategy and the harmonic compensators. It includes the power devices, the gate drivers power supply, the signal conditioners and

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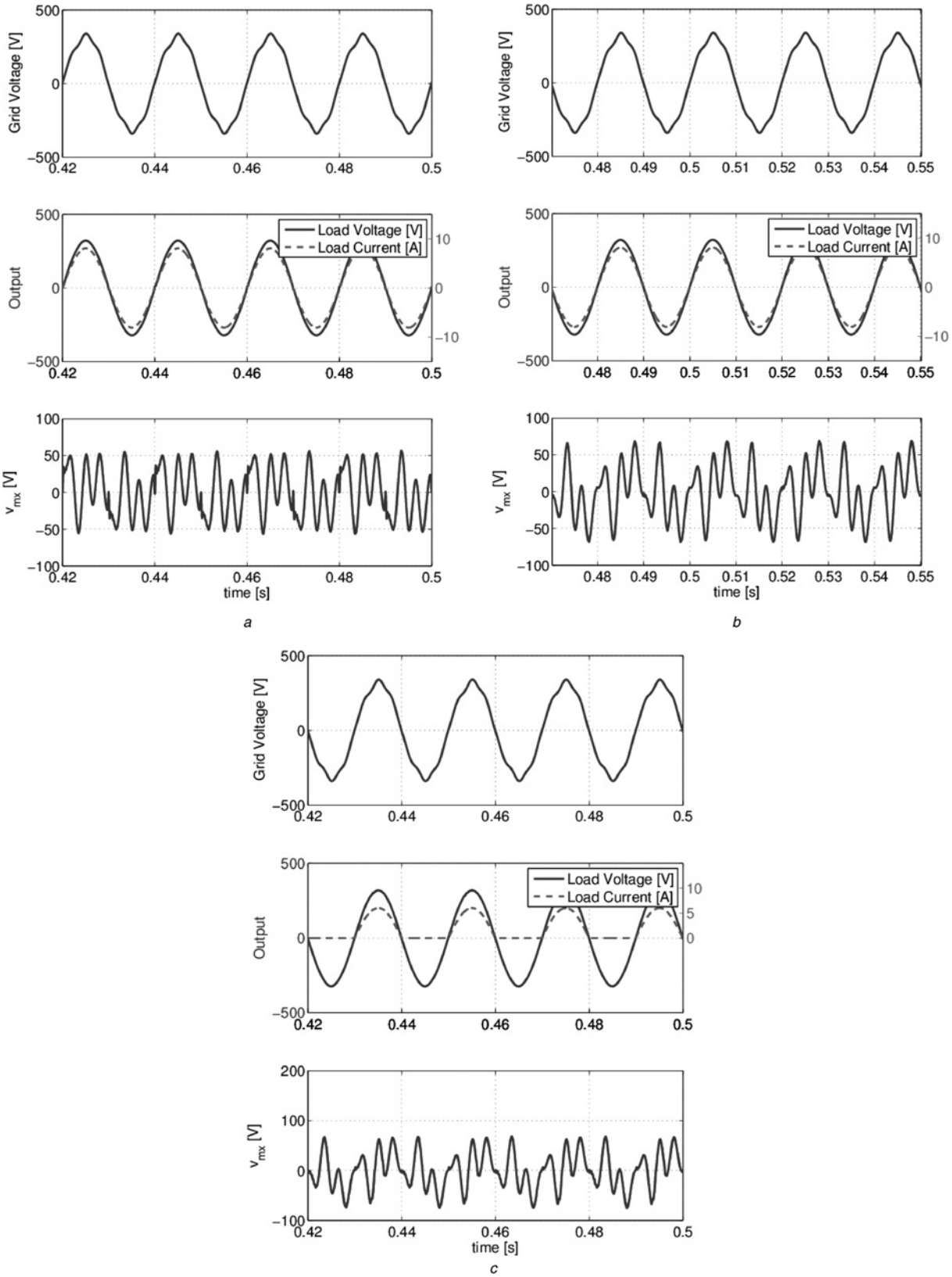

Fig. 7 *Simulation results with RDFT harmonic compensator*

a No ZVC
b ZVC
c Simulation results with non-linear load

a Freescale MPXS2010VLQ120 microcontroller performing signal processing and generating the PWM signals. The test bed was set up in accordance with the schematic of Fig. 1*b*. The circuit parameters were the same used for the simulations (Table 1) but with reduced power ($R_l = 150\ \Omega$). A picture of the test bed is shown in Fig. 9.

Data were acquired with a Lecroy HDO 6054 digital storage oscilloscope through ADP305 (differential voltage) and AP015

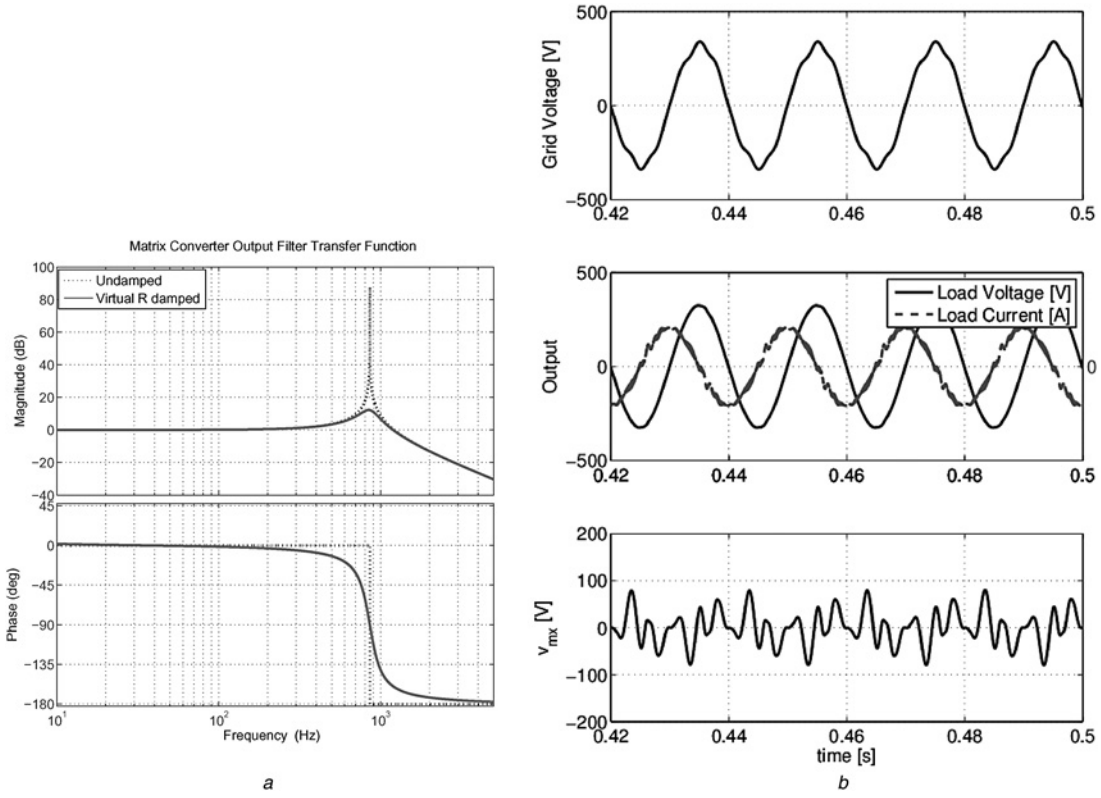

Fig. 8 *Operation with capacitive load*

a Undamped and damped output transfer functions of the MC
b Simulation results for pure capacitive load

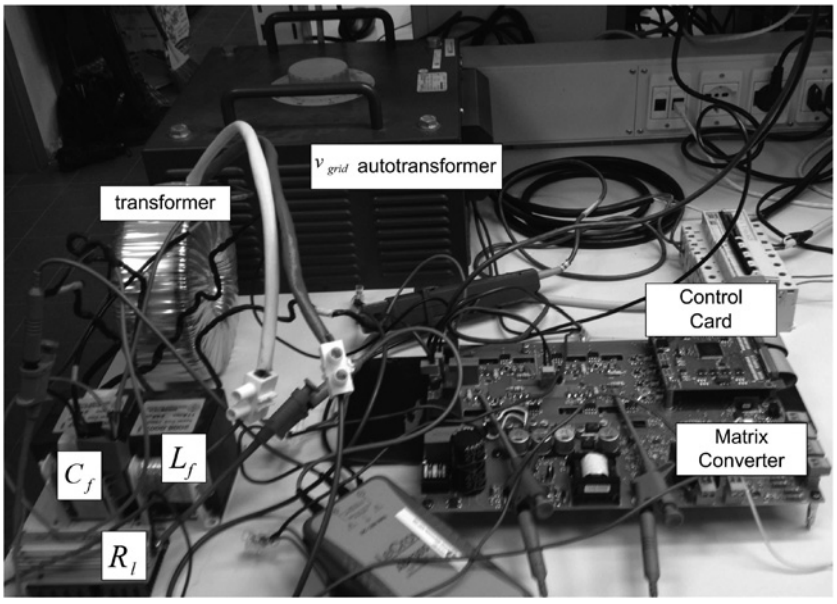

Fig. 9 *Picture of the test bed*

(current) probes. The samples were then imported in MATLAB in order to calculate the spectra and plot the figures.

The same distorted input waveform was used as in the simulations, with the actual resulting rms value slightly lower due to limitations of the converter used to generate the distorted grid voltage. Fig. 10 shows the results. The same layout of Fig. 7 was kept even for the sampled data in order to facilitate the comparison, and a very good agreement with the simulations can be seen. Again, distortion of the MC output and voltage oscillations in proximity of the zero crossings are present when the ZVC is not employed. A zoomed version of the MC output and load voltage in proximity of a zero crossing is also reported in Fig. 10*c*. As can be seen, without ZVC the MC output is forced to go to zero, causing a distortion of the output voltage. With ZVC, this effect is highly mitigated.

Fig. 11 shows further details of the experiments. In particular, the input current is reported in Fig. 11*a*. It is evident that further

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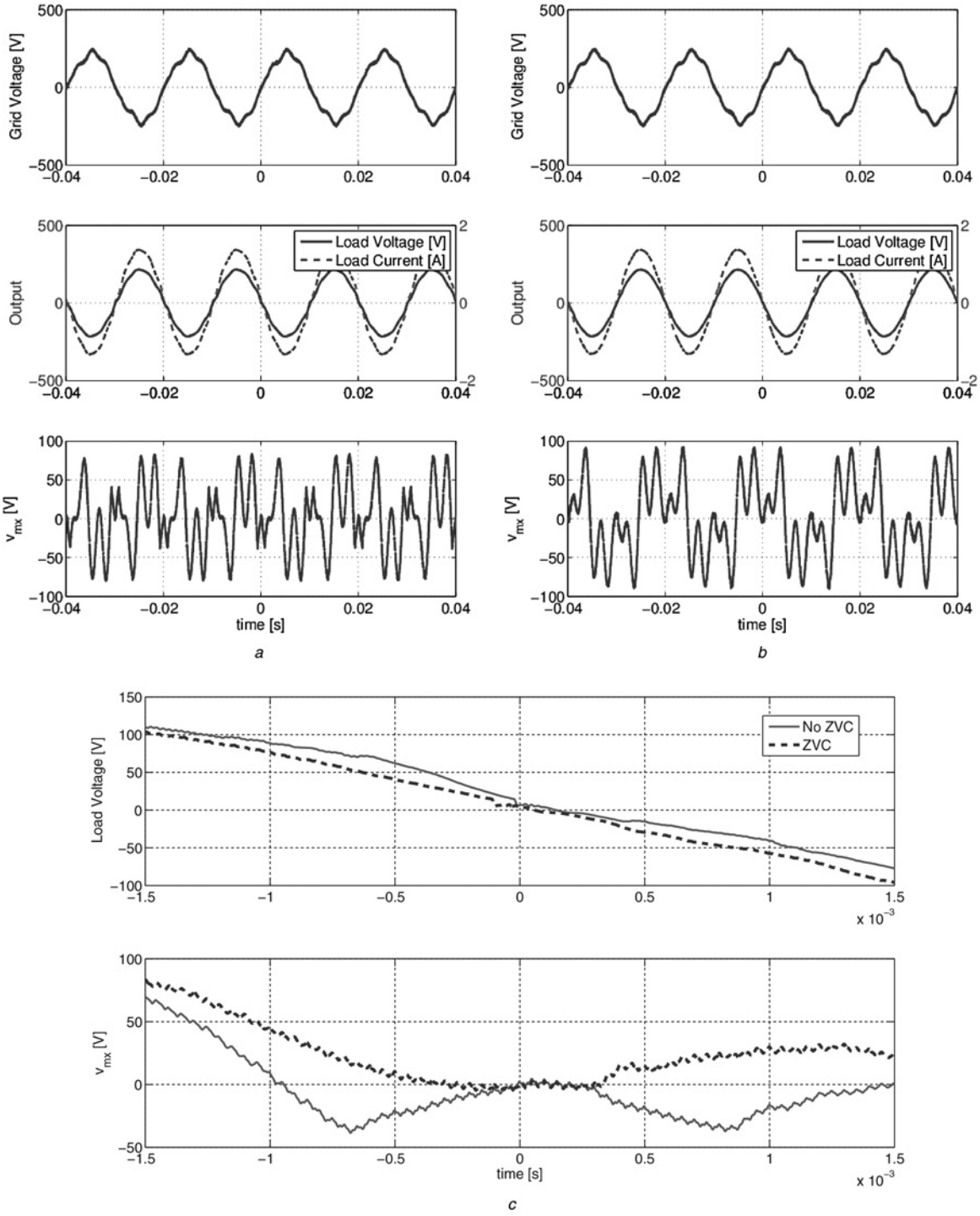

Fig. 10 *Experimental results with RDFT harmonic compensator (sampled data acquired by Lecroy HDO6054 DSO)*

a No ZVC
b ZVC
c Zoomed waveform in proximity of the zero crossing

harmonics are produced, but the SPMC is operating as expected. During the peaks of the input voltage the input current decreases (in order to have fundamental current at the output).

Fig. 11*b* shows the start-up transient with the RDFT compensator. The bandwidth of the controller is limited by the RDFT calculation (that introduces a delay of one grid voltage period), but the accuracy is greater than with the other compensator [29].

For completeness, the spectra of the input and output voltages are reported in Fig. 11*c* with their peak values highlighted. As can be seen, the compensation of the fifth and seventh harmonics is almost perfect, while some third harmonic distortion remains. This can be explained with the fact that non-linearities that were not modelled in the simulations, such as the on-state voltage drop of the devices, cannot be compensated by the controllers, and as a consequence a small third harmonic distortion remains.

The fact that a small third harmonic remains does not constitute a stability issue. Theoretically, if a constant third harmonic remained in the output voltage, the infinite gain of the RDFT compensator could lead to numerical instability problem. What actually happens is that the input of the PI regulators (see Fig. 4) oscillates around the zero value. As a matter of fact, the phase of the residual third harmonic is not constant, but changes continually.

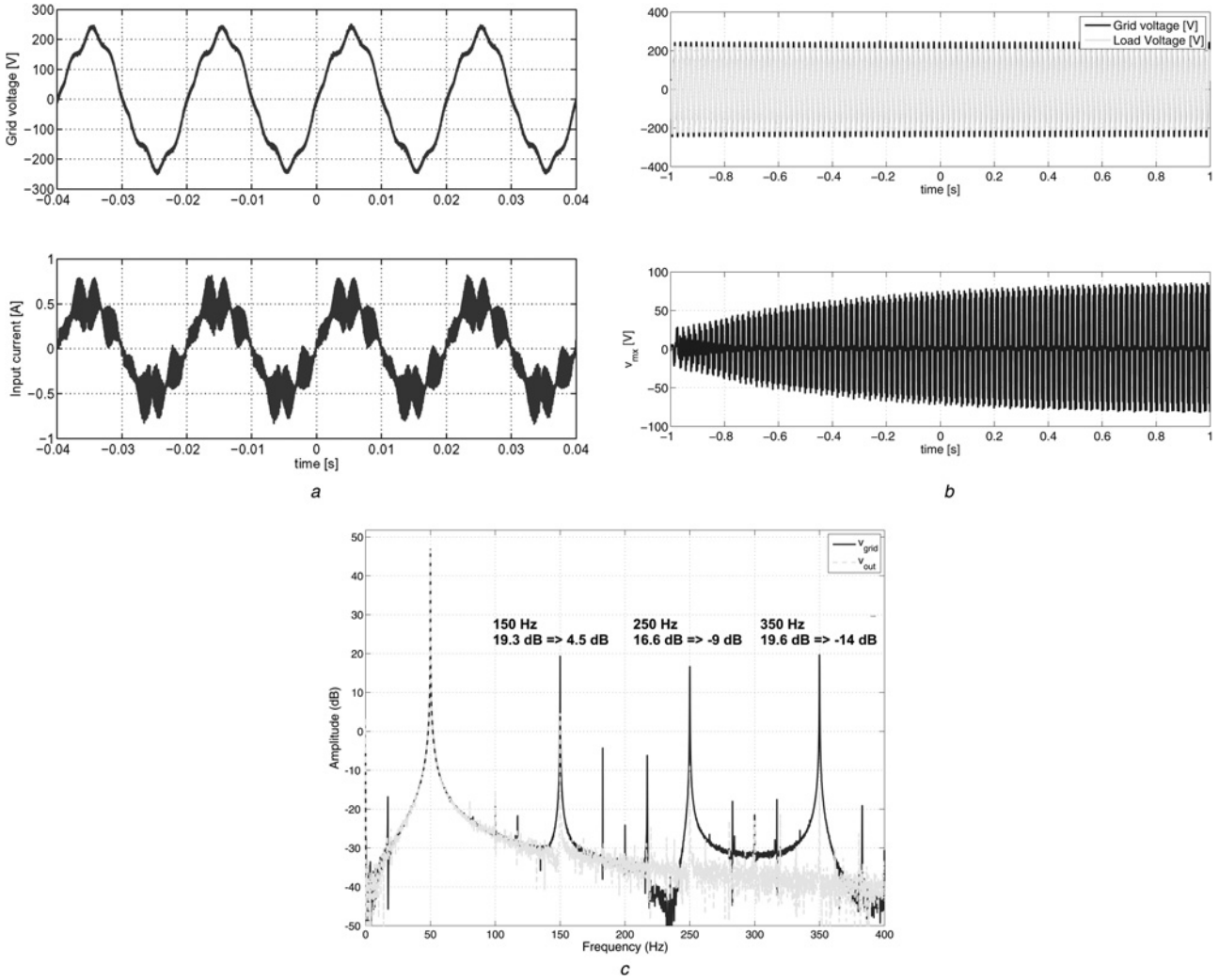

Fig. 11 *Detail of the experiments with the RDFT compensator*

a SPMC input current
b Transient response
c Spectra of input and output voltages

7 Conclusion

A single-phase series APF was developed based on a SPMC. The proposed system can operate bidirectionally and needs no DC capacitor. A four-step voltage commutation technique that employs a single sensor was used, and a particular switching strategy that implies short circuiting the output terminals was proposed to prevent output open-circuit conditions. The control requirements are strongly reduced relative to a standard back-to-back inverter (no need to control the DC link), as well as the number of required sensors (only two voltage sensors) and passive components (no DC-link capacitors nor input inductances).

A drawback of the MC relative to a back-to-back solution is that the output voltage is not perfectly controllable when the input voltage is close to zero. To mitigate this problem, a zero-voltage compensation technique based on a time shift of the output voltage zero crossing was proposed and tested. This strategy should be used when slight changes in the output rms voltage and phase are allowed. In fact, the first harmonic introduced by the ZVC may limit the remaining voltage available for harmonic compensation.

The main drawback is that, differently from a three-phase matrix converter, even if a transformer with unity turn ratio is chosen, the output voltage can never exceed the input voltage. Because of this, particular combinations of harmonics, that need a compensating voltage higher than is available near the input voltage zero crossing, cannot be fully compensated.

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