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Coexistence of Grain-Boundaries-Assisted Bipolar and Threshold Resistive Switching in Multilayer Hexagonal Boron Nitride

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Abstract

The use of two dimensional (2D) materials to improve the capabilities of electronic devices is a promising strategy that has recently gained much interest in both academy and industry. While the research on 2D metallic and semiconducting materials is well established, the knowledge and

applications of 2D insulators are still very scarce. In this report we study the presence of resistive switching (RS) in multilayer hexagonal boron nitride (*h*-BN) using different electrode materials, and we engineer a family of *h*-BN based resistive random access memories with tunable capabilities. The devices show the coexistence of forming-free bipolar and threshold type RS with low operation voltages down to 0.4 V, high current on/off ratios up to 10^6, long retention times above 10 hours, as well as low variability. The RS is driven by the grain boundaries (GBs) in the polycrystalline *h*-BN stack, which allow the penetration of metallic ions from adjacent electrodes. This reaction can be boosted by the generation of B vacancies, which is more abundant at the GBs. To the best of our knowledge, *h*-BN is the first 2D material showing the coexistance of bipolar and threshold RS, which may open the door to additional functionalities and applications.

1. Introduction

Storing digital information is one of the most demanded electronic applications in modern societies, as its capacity doubles every year and the total data storage capacity by 2020 is expected to reach 44 ZB.[1] Among all non-volatile memory (NVM) technologies invented, the resistive random access memory (RRAM) is one of the most promising due to its high performance and simple structure. The RRAM basically consists on a matrix of metal/insulator/metal (MIM) capacitors, in which the electrical resistance of the dielectric can be tuned by applying electrical stresses between the electrodes, allowing cyclical switching between a high resistive state (HRS) and a low resistive state (LRS).[2] These two states can be used to simulate the zeros and ones of the binary code, and therefore to store digital information. To date, RRAMs with high operation speeds (~ 300 ps/transition),[3] low power consumption (~ 0.1 pJ/transition),[4] good endurance (> 10^{12} cycles),[5] long data retention times (> 10 years),[6] small size (down to 10 nm × 10 nm),[7] and high integration capacity (> 1×10^{11} bits/cm^2) [2] have been developed. These performances have been

achieved using transition metal oxides (TMO) as dielectric in the MIM structure (mainly HfO_2,[8-11] Al_2O_3,[12-15] TiO_2 [16-19] and TaO_X.[20-21]); the metallic electrodes most commonly used in MIM cells for RRAMs are Ti, Pt, Ag, Cu and Ni.[22] Unfortunately, to date no RRAM device has shown all these performances simultaneously, which is strongly hindering its mass production. Some commercial developments can be found in the market,[23-24] but their capacities are still very limited (*i.e.* they are just recommended for controlling sensors). Moreover, cycle-to-cycle and device-to-device variability is still a recognized problem of RRAM technologies. [25-26]

To solve these problems, one promising methodology is to replace the metallic or insulating films in the MIM cells by other materials with advanced capabilities. In this context, the use of two dimensional (2D) materials has been very successful to develop field effect transistors and capacitors,[27-28] providing additional capabilities to the devices, such as flexibility and transparency. Several 2D materials including graphene, graphene oxide, MoS_2, $MoSe_2$ and even black phosphorous have been introduced in RRAM prototypes with the aim of enhancing their switching characteristics and providing additional functionalities. [29-34] However, graphene is conductive and needs to be complemented by an insulator (with which it usually forms a poor interface),[35] plus it requires an annoying transfer process; graphene oxide is not an excellent insulator (*i.e.* it can be easily degraded with the time, and for this reason GO-based RRAMs showed a poor endurance <100 cycles)[36-37] and its synthesis process (usually Hummers method and liquid phase exfoliation) is not compatible with the semiconductor industry; [38] and the same happens for MoS_2, $MoSe_2$ and BP, which furthermore are not insulators, meaning that they are not able to provide large current on/off ratios in RRAM devices.[32]

Hexagonal boron nitride (*h*-BN) may be a good solution enabling the fabrication of RRAMs and other logic devices given its insulating properties (its band gap is ~ 5.5 eV [39-40] and its dielectric constant is ~ 3), [41] which can generate essential device functionalities, including the generation of electrical fields and capacitance effects. On one hand, compared to other 2D

conductive and semiconducting materials, *h*-BN doesn't require any transfer process to build an RRAM, as it can be grown on a metallic substrate (which acts as bottom electrode) using scalable chemical vapour deposition (CVD) technique, and the top electrodes can be easily evaporated on it to form the MIM cells. This strongly simplifies the fabrication process, as well as it avoids the generation of cracks during 2D material manipulation [42] and the presence of contaminants from polymer scaffolds.[43] Moreover, the insulating nature of *h*-BN should result in a larger current on/off ratio in RRAMs. And on the other hand, compared to traditional dielectrics like SiO_2 or TMOs, *h*-BN can be prepared with a very flat/uniform surface that may reduce variability effects, [44] its superior chemical stability may inhibit interaction with adjacent layers, and its large thermal conductivity could favour heat dissipation in electronic devices.[41] Moreover, *h*-BN shows better reliability than HfO_2 when exposed to electrical stresses,[45] and at the same time it is known that the grain boundaries (GBs) in polycrystalline CVD-grown *h*-BN sheets can serve as leaky paths. [46-47] The local generation of hot spots in a robust dielectric is a very interesting behaviour in the field of resistive switching (RS), as that may limit dielectric breakdown (BD) lateral propagation, which should enhance the endurance of the RRAMs.

In this work we investigate the presence of RS in multilayer *h*-BN stacks using different top electrodes, and we develop a complete family of scalable RRAM devices using multilayer *h*-BN as active RS medium. The devices show forming-free bipolar and threshold RS depending on the current limitation used, which is driven by the GBs in *h*-BN, as they allow easy B vacancies generation and metallic ion penetration. We achieve good control of the device properties by tuning the thickness and grain size of the *h*-BN stack, as well as by inserting interfacial graphene electrodes. The use of an entirely scalable fabrication process (*i.e.* mechanical exfoliation and electron beam lithography are avoided, and 2D material transfer is not required) is an important added value towards industry-compatible applications. We also demonstrate stable RS operation in

flexible/transparent RRAM devices under bending. These results may represent an important milestone towards the use of 2D dielectrics in logic devices.

2. Results and discussion

Multilayer *h*-BN stacks of different thicknesses (*thin* 5-7 layers and *thick* 15-20 layers) have been grown by chemical vapour deposition (CVD) on Cu and Ni-doped Cu substrates (which also served as bottom electrode), and top squared electrodes of different sizes and materials have been evaporated on top using a shadow mask (see experimental section and Figs. S1 and S2 in the Supporting Information, SI). In total six different types of RRAM devices have been fabricated (see **Table 1** and experimental section) and more than 300 cells have been characterized. **Fig. 1**a shows the schematic representation of a Ti/thin *h*-BN/Cu device. Fig. 1b displays the typical current vs. voltage (*I-V*) curves collected in this device, which show forming-free bipolar RS with very low set and reset voltages (V_{SET} and V_{RESET}) below 0.4V and -0.8V (respectively), and current on/off ratios of more than one order of magnitude. The cycle-to-cycle variability is very small, as corroborated in the Weibull plot of the resistance read at 0.1V during more than 350 cycles (see Fig. 1c). The reset process takes place in two phases: *i)* first, a sudden current decrease occurs at ~ -0.28 V, and *ii)* from that point until ~ -0.8 V the resistivity increases progressively. This is indeed indicating that the charge transport is governed by one completely formed conductive filament (CF) that coexists with several partially formed CFs. It should be highlighted that in some cycles (<25% of the total) we have observed several small sudden jumps that fit different levels of conductance during the reset process (see Fig. S3 in SI), indicating the presence and sequential disruption of multiple partially/completely formed CFs. More information about the current fittings using the quantum point contact (QPC) model can be found in the Supporting Information (SI). In any case, the most repetitive reset behaviour was the presence of a sudden initial current decrease followed by a

progressive resistivity increase (as shown in Fig. 1b), indicating the presence of a dominant CF; this observation is supported by the negligible area dependency observed in these devices (see Fig. S4b in SI) —this feature shows an important downscaling potential—. It is worth noting that, despite the amount of partially/completely formed CFs may by vary during some (<25%) cycles, the currents in HRS and LRS showed low cycle-to-cycle variability (see Fig. 1c).

Cross sectional transmission electron microscope (XTEM) images collected in the fresh devices (Fig. 1d) reveal the presence of many atomically thin defective paths formed across the layered *h*-BN stack, which are related to the well known formation of defective GBs during the CVD growth process. [47] This is in good agreement with the observation of forming-free RS (Fig. 1b). Fig. 1d further confirms that the GBs of each layer within the *h*-BN stack vertically align. In order to find out the chemical species involved in the switching, XTEM analyses coupled with electron energy loss spectroscopy (EELS) have been conducted. The typical EELS profiles at both non-defective (layered) and GB/CF locations of a Ti/thin *h*-BN/Cu device in LRS are plotted in Figs. 1e and 1f (respectively). As it can be observed, at non-defective locations (Fig. 1e) the B and N signals are quasi symmetric respect to their maximum, overlap, and appear confined between the Cu and Ti profiles, *i.e.* no metallic impurities at the *h*-BN region have been observed. On the contrary, the EELS profiles collected at the GB/CF locations of the sample in LRS (Fig. 1f) show clear migration of B towards the Ti electrode (the shape of the B profile is asymmetric), and at the same time penetration of Ti into the *h*-BN can be observed. It should be highlighted that the EELS cross sections (Figs. 1e and 1f) overestimate the thickness of the layers compared to TEM images (Fig. 1d); this was an expected behaviour related to the lower accuracy and resolution to EELS compared to TEM. Therefore, the horizontal scales in Figs. 1e and 1f should be qualitatively interpreted: *i.e.* the signals in Fig. 1f spread in depth due to severe B and Ti migration.

The migration of B towards the Ti electrode is consistent with the lower activation energy calculated for B ion/vacancy diffusion,[46] which could be even lower at the GBs. The ability of Ti

to react with other species (*e.g.* O atoms in TMOs) and its capacity to migrate in/out of a dielectric to form/disrupt CFs have been already observed in other RRAM devices. [48-49] Under top electrode positive polarization, Ti^{X+} ions may move towards the cathode across the RRAM cell,[50] leading to the formation of a Ti or TiN based CF through the *h*-BN stack. This observation is in agreement with the lack of temperature dependence displayed in Fig. S4a. The Ti^{X+} ions are expected to diffuse preferentially at GB locations, where the lower density of the material and the larger density of B and N vacancies favour their migration. It is worth noting that GBs-free exfoliated *h*-BN does not exhibit RS, as corroborated by Hattori *et al.*,[51] thus confirming the key role played by GBs in the RS. The presence of GBs in the dielectric reduces the energy-to-breakdown and the overall assertiveness of the whole BD process, allowing its reversibility.[52] It is worth noting that the GB-to-GB distance observed in *h*-BN (between 2 and 8 nm in Fig. 1d) is much smaller than that observed in polycrystalline TMOs (>60 nm in Al_2O_3).[53] Therefore, while the need for a GB may represent a concern when building nanosized TMO based RRAMs, this is not a problem in *h*-BN based RRAMs. Furthermore, note that (unlike in TMOs) the size of the grains can be easily controlled with the CVD growth parameters (as it will be explained later), making possible tuning the amount of GBs per cell.

The switching mechanism observed in Ti/*h*-BN/Cu devices is different than those observed in TMO based ones, in which the charge transport is governed either by O vacancies or metal ions movement. [54-55] The Ti/thin *h*-BN/Cu RRAM devices here presented show a combination of both phenomena: B vacancies migration and mobile Ti^{X+} ions penetration in the *h*-BN stack may occur simultaneously (see Fig. 1f). Despite O vacancies migration in TMOs and B vacancies migration in *h*-BN may present certain parallelism, we are not aware of other works reporting RS based on B vacancies migration in *h*-BN. The large density of Ti at the CF region and the unaltered N profile, indicate the formation of a TiN-based CF, although this hypothesis should be confirmed by *ab initio* calculations (which is out of the scope of this report). Then, under negative top electrode

polarization the B ions and Ti^{X+} ions may diffuse back to their original positions (*h*-BN stack and Ti electrode respectively), disrupting the CFs created across the *h*-BN and increasing the overall resistance of the Ti/thin *h*-BN/Cu cell (reset process). The importance of Ti/*h*-BN interactions for the RS is supported by the absence of RS when using top Pt or Au electrodes (see Fig. S5a in SI) because noble metals with lower diffusivity don't allow interaction with other species. On the contrary, when the set event is induced using negative polarity, none of the Ti/thin *h*-BN/Cu RRAM devices showed bipolar RS (see Fig. S5b), *e.g.* the subsequent positive top electrode biasing didn't produce the reset of the devices. We also used different current limitations (CL) ranging from 10^{-6} to 10^{-1} A, but no bipolar RS was observed under negative set in any Ti/thin *h*-BN/Cu device. This is surprising because Cu^{X+} ions movement is known to be the driving force behind bipolar RS in electrochemical metallization (ECM) cells using TMO dielectrics and Cu electrodes. [56] This observation may be related to the large diffusivity of Cu^{+} ions, which may massively penetrate in the *h*-BN stack during the negative BD event, leading to irreversible BD. This rules out the involvement of Cu^{+} ions in the bipolar RS observed in Fig. 1b, and further supports that B and Ti^{X+} ions migration are the atomic rearrangements behind the switching in Ti/thin *h*-BN/Cu RRAM devices.

The involvement of oxygen in the switching has been discarded through ionic liquid gating experiments, [57] which reveal no remarkable conductivity changes when *h*-BN stacks are exposed to air after ionic liquid gating experiments. Similar experiments performed in TiO_2 and other oxides [58] revealed dramatic conductivity decrease after exposure to room environment due to the absorption of oxygen. Such phenomenon didn't take place in *h*-BN stacks. The influence of oxygen in RRAM devices capped with (60 nm thick) metallic top electrodes should be even lower (i.e. negligible).

With the aim of increasing the current on/off ratio, we follow three strategies: *i)* use *h*-BN stacks with different thicknesses, *ii)* reduce the amounts of defects by increasing the *h*-BN grain

size, and *iii)* use of graphene interface electrodes. First, the thickness of the *h*-BN stack grown on Cu was increased by just enlarging the CVD growth time. The resulting Ti/thick *h*-BN/Cu devices show bipolar RS with enhanced current on/off ratios up to 10^4 (see Fig. 2a). Interestingly, this behaviour is not accompanied by the need of a forming process, and the device-to-device variability is very small (see Fig. S6 in SI). The pronounced sharp shape of the reset and the lower currents in HRS (compared to the thin *h*-BN sample, Fig. 1b) indicate the presence of less totally/partially formed CFs in the *h*-BN stack, as well as that the BD recovery may have a different physical origin most probably related to thermal heat.[59] The small current decrease at ~ -0.4V right before the sudden reset indicates filament thinning before the complete disruption. Interestingly, unlike thin *h*-BN cells, Ti/thick *h*-BN/Cu devices showed bipolar RS when the set was induced under negative top electrode polarization (see Fig. 2b), but only under lower CLs, *e.g.* 70 μA for negative set (Fig. 2b) and 10 mA for positive set (Fig. 2a). The explanation behind this observation may be as follows: when the thin *h*-BN, is subjected to negative top electrode bias the large diffusivity of Cu may produce severe contamination of the thin *h*-BN, leading to an irreversible BD, as seen in Fig. S5b. On the contrary, similar electrical stresses applied to thick *h*-BN produce less damage. The fact that bipolar RS using negative set is only observed under CLs smaller than those used under positive set is consistent with this hypothesis: under same CL (10 mA) the large diffusivity of Cu produces irreversible BD.

We further explore the RS capabilities of Ti/thick *h*-BN/Cu RRAM devices by tuning the current limitation, which revealed interesting additional performances. When the current compliance is lowered to values between 10^{-6} and 10^{-4} A, threshold-type RS [60] with current on/off ratios up to 3 orders of magnitude has been observed (see Fig. 2c). For all current levels, the voltage windows are enough large and ensure no data mismatch. Larger CLs induce smaller V_{SET} and V_{RESET}, indicating good tunability of the CF size. The recovery of the HRS in the absence of bias indicates that *h*-BN is a stable and reliable dielectric, which may be related to the enhanced chemical stability

of the *h*-BN stack. To the best of our knowledge, this is the first 2D material based RRAM device showing threshold RS; probably, previous devices made using graphene, MoS_2, $MoSe_2$ and BP didn't show this capability because they are not insulators, and graphene oxide may not be enough robust to restore its resistivity when the bias is switched off. The observation of threshold type RS in *h*-BN opens the door to its use as selector in RRAM devices.

As an strategy to further reduce the currents in HRS, the multilayer *h*-BN stacks have been grown on Ni-doped Cu substrates, which increases the size of the domains and reduces the amount of defective GBs per unit area (see Fig. 3a).[61] All the devices fabricated with this substrate required a forming process (see Fig. S7a in SI), and the forming voltage increased with the *h*-BN stack thickness. It is worth noting that the forming process in layered 2D insulators differs from that of 3D insulators, as the layered material shows novel anisotropic speed for defect formation,[51] due to the different type of spatial interactions (covalent bonding in-plane and van der Waals interactions out-of-plane). The pre-BD currents show clear area dependence (see Fig. S7b in SI), indicating that no completely formed CFs are created during the CVD growth. The post-BD *I-V* curves show bipolar RS behaviour (see Figs. 3b and 3c), and the devices using thicker *h*-BN stacks show higher V_{SET} and V_{RESET} voltages (2V and -1.5V respectively), as well as larger current on/off ratios (up to 6 orders of magnitude). Compared to the *h*-BN/Cu counterparts, the devices using bottom Ni-doped Cu electrodes show lower currents in HRS (I_{HRS}), probably due to the lower amount of partially formed CFs (and GBs, see Fig. S8 in SI).

The ability of *h*-BN to build flexible and transparent RRAM devices has been proved by using ITO/PET substrates. These devices have been fabricated transferring thin *h*-BN (grown by CVD on Cu) onto flexible PET polymer with a ~ 185 nm thick film of ITO on top, followed by electrodes evaporation (see experimental section). Then, the devices have been tested in the probestation under different bending radius (see Fig. 4a). For all tests, the Ti/*h*-BN/ITO devices showed reproducible bipolar RS during more than 180 cycles (see Fig. 4b), and no RS degradation

was observed. The progressive reset is similar to the one observed in Ti/*h*-BN/Cu devices (Fig. 1b). The observation of RS in Cu-free Ti/*h*-BN/ITO devices supports that Cu is not necessary for inducing state transitions, in agreement with the EELS profiles (Fig. 1f). After more than 180 cycles, the cumulative probability plot of the resistance in HRS and LRS measured at 0.1V shows acceptable variability without resistance mismatch in both states (Fig. 4c).

Finally, the RS phenomenon has been studied by inserting a sheet of multilayer graphene (MLG) between the *h*-BN and the metallic electrodes. Graphene interfacial electrodes have demonstrated to reduce the power consumption of RRAM devices thanks to graphene's high out-of-plane electronic resistance, stabilize the RS response by blocking oxygen diffusion, protect the dielectric from environmental moisture, provide superb transparency, and allow mechanical bending without performance degradation.[29-30, 62] Ti/MLG/*h*-BN/MLG/Au RRAM devices have been fabricated with assistance of standard transfer process.[63] The entire fabrication process is schematically described in Fig. S9. Basically, a wafer of 300 nm SiO_2/Si has been coated with 10 nm Ti (first) and 50 nm Au (second). Then, the surface of the Au has been functionalized via oxygen plasma etching process for 1.5 minutes in O_2 atmosphere using a power of 200 W to increase the roughness of the substrate, which favours the adhesion of the 2D material and reduces the amount of wrinkles. [64] Then, first a MLG sheet, second a thin *h*-BN sheet (previously grown on Ni-doped Cu), and third another MLG sheet have been sequentially transferred, and Au/Ti electrodes have been evaporated on top by shadow mask and e-beam evaporator (as in previous devices). More details can be found in the experimental section and Fig. S9. At this step, the samples have been characterized via optical microscope (not shown) SEM (Fig. S10) and AFM (Fig. S11), which reveal smooth surface of each layer. In the AFM topographic maps, we intentionally displayed some areas where wrinkles were formed to demonstrate the presence of 2D material. The XTEM images (Fig. 5a) show the thick 2D layered (van der Waals) heterogeneous stack. By means of EELS cross sections (Fig. 5b) we prove the correct fabrication of the Ti/MLG/*h*-BN/MLG/Au

devices. As it can be observed, the B and N signals are confined between the two C peaks corresponding to MLG electrodes. After this, the top MLG sheet has been removed by plasma etching to isolate all the MIM cells (keeping top MLG only under the top metallic electrodes, see Fig. S9) and the resulting devices have been tested in the probestation.

From an electrical point of view, compared to metal/*h*-BN/metal counter devices (Fig. 3b), the use of MLG interfacial electrodes increased the forming voltage up to ~8 V (see Fig. 5c), and the reset process turned into sharp. More information about the size of the partially formed CF (constriction) before and after the forming is given in the SI. In the following cycles, the devices showed improved current on/off ratios up to 4 orders of magnitude with low cycle-to-cycle variability (no HRS/LRS data overlap, see Fig. 5d), as well as long state retention times (Fig. 5e). The device-to-device variability is also very small, as these results have been successfully reproduced in more than 35 devices (see Fig. S12 in SI). It is worth noting that V_{SET} is larger and I_{HRS} is lower than in graphene-free devices using the same type of *h*-BN (see Fig. 3b). These observations could be explained as follows: the MLG film acts as blocking layer that difficult atomic diffusions though it, [65] *i.e.* B migration towards the Ti electrode and Ti^{X+} ions penetration in the *h*-BN stack (see Fig. 1f). Nevertheless, at graphene point defects the penetration of Ti^{X+} ions is possible. Lübben *et al*.[62] observed that, in both Ta/graphene/TaO_X/Pt and Pt/graphene/TaO_X/Pt devices, the interactions between Ta ions and the TaO_X film can take place during the RS process (even with the presence of interfacial graphene). This larger difficulty for metal ions migration into the *h*-BN film results in a larger forming voltage (up to ~8V) compared to graphene-free devices (in which $V_{FORMING}$ was below 3V, as shown in Fig. S7a). The sharper nature of the reset process and the lower I_{HRS} in Ti/MLG/*h*-BN/MLG/Au devices can be easily explained by the lower amount of filaments through the *h*-BN stack; [66] the larger V_{SET} currents compared to graphene-free cells may also be related to the well known higher out-of-plane resistance offered by the graphene film, [30, 62] which should be also a factor contributing to lower I_{HRS}. These hypotheses have been confirmed by

XTEM and EELS. After the electrical stresses, almost all locations of the sample showed undamaged structure (similar to that displayed in Fig. 5b). However, at some spots of the sample, partial *h*-BN degradation was observed (Fig. 5f), and just a few locations revealed complete CF formation (Fig. 5g). The EELS profiles collected at the partially degraded and CF locations reveal clear penetration of Ti into the *h*-BN stack (Fig. 5h) which reaches the bottom MLG layer (Fig. 5i), as well as the complete dissolution of the graphene layer at the Ti/*h*-BN interface, consistent with the penetration of Ti^{X+} ions (the C peak related to the MLG stack between the Ti and *h*-BN is missing, see Fig. 5b for comparison). It should be highlighted that the shifts of the B and N signals observed in Figs. 5h and 5i are not representative, as important variability from one CF to another has been observed. The only repetitive and meaningful atomic rearrangement in all the EELS profiles collected for the Ti/MLG/*h*-BN/MLG/Au samples is the penetration of Ti^{X+} ions into the *h*-BN. Probably the more abrupt HRS/LRS/HRS state transitions (driven by the Ti^{X+} ions migration) lead to more uncontrollable rearrangements in the B and N signals. Interestingly, the shape of the filament is conical with the narrower end at the anode side, indicating the migration of Ti^{X+} ions (or clusters of ions) towards the cathode under positive set biasing (see Fig. 5g), in agreement with the EELS profile.[67] This is indeed indicating that the Ti diffusivity in the bulk *h*-BN is larger than at the top MLG/*h*-BN interface, otherwise the Ti^{X+} ions would accumulate at the MLG/*h*-BN interface, moving slowly towards the bottom *h*-BN/MLG interface and producing a filament with opposed shape (narrower end at the cathode). This is consistent with the blocking nature of the MLG stack, and further explains the small migration of B towards the top Ti electrode observed in Fig. 5i. Interestingly, when the set is induced under negative top electrode polarization, the Ti/MLG/*h*-BN/MLG/Au RRAM devices don't show stable RS (just 3 cycles, not shown); this should be related to the poorer mobility of Au ions in the *h*-BN stack, and further supports that the RS observed in Fig. 5c is related to the migration of Ti^{X+} ions. In the case of metal/*h*-BN/metal devices, metallic ion migration is always accompanied by B vacancies movement, while the devices using graphene

interfacial electrodes show RS even without the diffusion of B towards the electrodes. As in the flexible/transparent device (Fig. 4) the absence of Cu in these devices indicates that this element is not necessary for observing RS.

Until today no RRAM device using 2D materials has achieved a performance comparable to that of the TMO-based technology.[68-69] Nevertheless, the extraordinary properties of 2D materials make them very promising in the field of RRAMs. Compared to 2D metals and semiconductors, in RRAM technology *h*-BN shows the advantage of no need of a transfer process, as well as higher current on/off ratios (as demonstrated above). Ref. [70] observed unipolar RS transitions in planar nanogap-based *h*-BN nanosheets obtained by mechanical exfoliation, but these devices are not scalable and no endurance tests were shown; moreover exfoliated nanosheets are not polycrystalline, which implies a different mechanism. Ref. [71] observed bipolar resistive switching in amorphous boron nitride,[71] but the absence of a layered structure (like the one we show in Figs. 1d and 3a) may jeopardize the chemical stability and thermal heat dissipation in the *h*-BN film. Compared to Ref. [71], our devices show forming-free bipolar RS, which coexists with threshold type RS in some devices. We also include additional information about the effect of *h*-BN thickness, *h*-BN grain sizes and interfacial MLG electrodes in the performance of the devices. The novel switching mechanisms here reported seem to be different to that observed in Ref. [71], as in that work the migration of B and the key role of the GBs is not demonstrated. The performances of all *h*-BN based RRAM devices here reported have been summarized in Table 1. Future works in this field should concentrate on the development of 2D materials based RRAM devices on metal coated wafers.

3. Conclusion

Multilayer *h*-BN stacks grown by CVD have been used for engineering a new class of two dimensional RRAM devices. The fabrication of the metal/*h*-BN/metal devices involved only

scalable techniques and didn't require 2D material transfer, *i.e.* the *h*-BN was grown by CVD on Cu (which served as bottom electrode) and top electrodes were patterned on top via shadow mask and e-beam evaporator. The resulting *h*-BN based RRAM devices show coexistence of forming-free bipolar and threshold type RS, which is a local phenomenon related to the formation of CFs at the GBs of the *h*-BN stack. By using different electrode materials we conclude that the RS is assisted by metallic ion penetration in the *h*-BN stack, which can be boosted by the generation of B vacancies. We developed three different strategies to tune the properties of the devices: *i) h*-BN stack thickness modification, *ii)* GBs density adjustment by substrate doping, and *iii)* insertion of interfacial graphene electrodes. As a result, the RRAM cells exhibited forming-free RS, low V_{SET} and V_{RESET} down to 0.4V and 0.8V (respectively), high current on/off ratios up to 6 orders of magnitude, long retention times above 10 hours and low device-to-device variability. The possibility of building flexible and transparent devices, as well as the fabrication of the first RRAM devices based on graphene/*h*-BN/graphene van der Waals structures have been also demonstrated. The observation of threshold type RS in *h*-BN may enable its use as selection in RRAM devices.

Experimental Section

Material synthesis. The *h*-BN/Cu samples were grown at the company Graphene Supermarket using borazine as precursor and a 20 μm thick Cu foil as substrate, following the procedures detailed in reference [41]. We bought two different items (no. A121913 and no. A120415) and, upon close inspection by XTEM we determined that their thicknesses are between 5 and 7 layers and 15-20 layers. In both cases the *h*-BN contains large amounts of GBs (see Fig. 1d). The *h*-BN/CuNi samples were grown by us using Ni doped Cu substrates, following the methodologies reported in our previous work.[61] This type of *h*-BN contains a very low amount of defects due to the larger size of its grains (less amount of GBs per unit area or device). In total, we

used two different batches of *h*-BN/Cu. The first batch had a thickness of 15-20 layers, and the second one between 5-7 layers. The materials sources were purchased in Resemi Co. Ltd.

Device assembly. After material growth, a matrix of top squared electrodes consisting of 40 nm Au (top) on 20 nm Ti (bottom), and with sizes ranging from 100 µm × 100 µm down to 10 µm × 10 µm, were deposited using an electron beam evaporator (Kurt J Lesker Company, PVD75) and a laser-patterned shadow mask (from Tecan, UK). The deposition rate in the evaporator was 0.5Å/s. Some MIM structures using Pt or Au electrodes (without Ti) have been also fabricated. In this investigation, six different sets of RRAM devices using two different types of *h*-BN were fabricated (see Table 1). No transfer process was required for devices type 1-4, while devices type 5 and 6 required transfer. The *h*-BN used for devices type 5 and 6 was the 5-7 layers thick (*thin*) grown on CuNi. For the fabrication of devices type 6, a substrate consisting of 300 nm SiO_2 on Si was covered with 20 nm Ti (first) and 40 nm Au (second). After that, the surface of the Au/Ti/SiO_2/Si wafer was exposed to oxygen plasma treatment (200 W during 1.5 min) to increase the roughness of the surface, which remarkably reduces the amount of wrinkles in subsequently transferred 2D films.[64] Then, a 8-12 layers thick MLG sheet grown at Hangzhou Gelafeng Nanotechnology has been transferred on the Au/Ti/SiO_2/Si sample using PMMA as rigid media. First, the liquid PMMA was spin-coated on the surface of the multilayer graphene with a two-step spin-coating process, 500 rpm for 6 s and 4500 rpm for 1 min. After that, the Cu foil was etched in $FeCL_3$ (0.1g/ml) and the PMMA/MLG stack was washed in HCL (2 wt%) and pure water. The PMMA/MLG stack was picked up with the target substrate, and it was dried at 50 ºC for 3 hours. Finally, the whole sample was immersed in the acetone for 24 hours to remove the PMMA. For the transfer of the successive *h*-BN and MLG, a similar process was followed. The size of each transferred 2D material was smaller than that of the previous one, so that the interfaces can be characterized (as shown in Figs. S10 and S11). Top Au/Ti electrodes similar to those of devices type 1-5 were evaporated on the top graphene layer to allow a good connection to the probestation. Finally, the capacitors were isolated

from each other by etching the top MLG between them using oxygen plasma at 200 W during 1 minute. The whole fabrication process is indicated in Fig. S9.

Device characterization. The devices were analyzed with two different scanning electron microscopes (SEM), the Carl Zeiss Supra 55 and the Quanta 200 FEG. The atomic force microscope (AFM) characterization was conducted using a Bruker Dimension Icon and a Multimode V AFM from Veeco. The topographic characterization was done in tapping mode using standard silicon tips from Nanoworld (item no. 78131F6L965), and the nanoscale electrical characterization was carried out in the Multimode V AFM using the CAFM module using Pt-Ir coated tips from Bruker (model SCM-PIC, item no. A008/01). The optical microscope pictures were collected with a Leica DM4000M. The cross-sectional transition electron microscopy (TEM) was done in two steps. First, thin lamellas were fabricated with a focus ion beam (FIB) from FEI (model: HELIOS NANOLAB 450S), which were placed on a copper grid for TEM inspection. After that, the lamellas were scanned with the high resolution TEM (JEOL JEM-2100 with a working voltage of 200 kV). The chemical composition of the samples was analyzed by electron energy loss spectroscopy (EELS) tool integrated in the TEM. The correct structure of both the *h*-BN and the multilayer graphene was corroborated by Raman Spectroscopy (not shown). The electrical properties of the devices were measured in a Cascade probe station using a Keithley 4200 semiconductor parameter analyzer. In this investigation more than 300 devices have been characterized.

Supporting Information

Supporting Information about the fabrication process and additional device level and nano/atomic scale characterization is available from the Wiley Online Library.

Acknowledgements

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List of figures

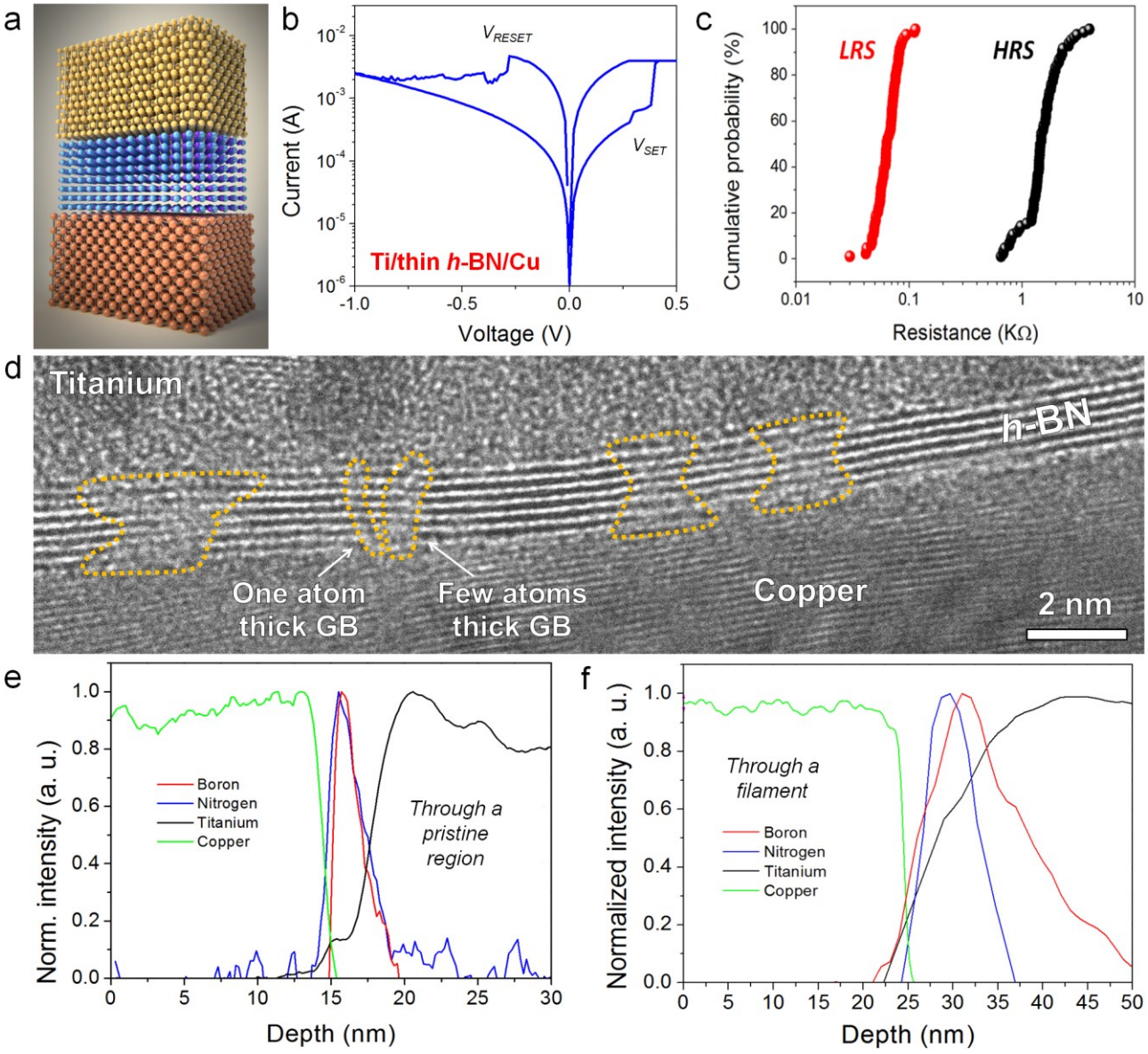

Figure 1: (a) Schematic of a Ti/thin *h*-BN/Cu RRAM device. (b) Typical *I-V* curves in a 100 µm x 100 µm device showing bipolar RS. (c) Cumulative distribution of the resistance per cycle in HRS and LRS read at 0.1V. (d) Cross-sectional TEM image showing defective paths (GBs) through the *h*-BN. (e) and (f) EELS cross-sectional analyses of a pristine and GB/CF locations (respectively) for a device in LRS.

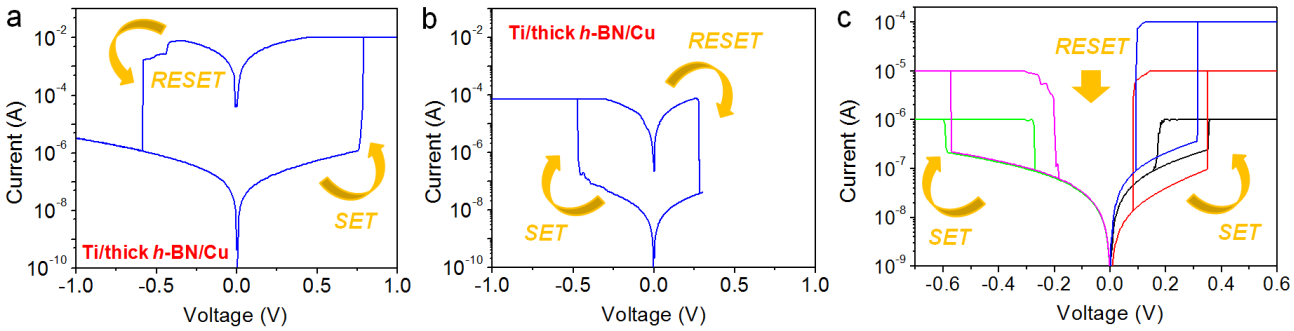

Figure 2: Typical RS behaviour observed for the Ti/thick *h*-BN/Cu when inducing the set process under positive (a) and negative (b) top electrode polarization. (c) Typical threshold-type RS measured in Ti/thick *h*-BN/Cu devices under positive and negative top electrode polarization using current limitations of 10^{-6} A, 10^{-5} A and 10^{-4} A. For negative top electrode biasing the plot at 10^{-4} A is missing because at such CL the devices don't show RS (the BD event becomes irreversible).

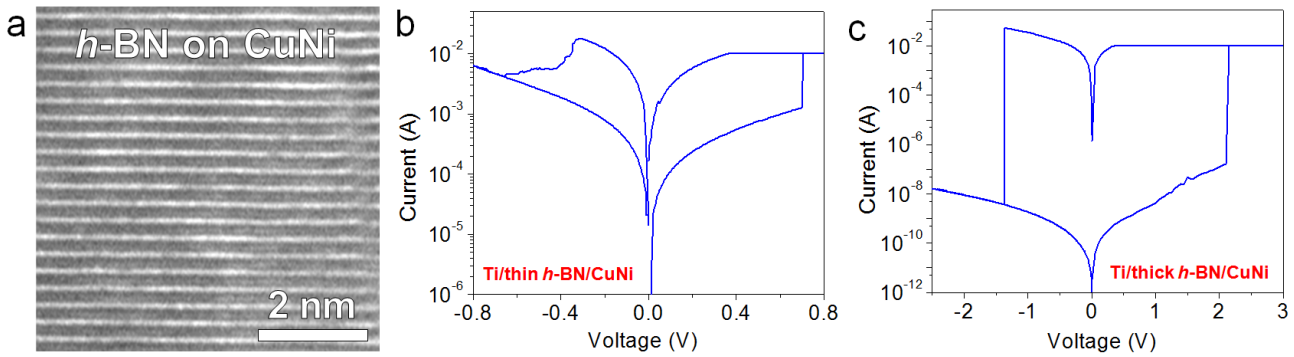

Figure 3: (a) Cross-sectional TEM image showing the improved structure of the *h*-BN stack grown on CuNi. Typical RS behaviour observed in (b) Ti/thin *h*-BN/CuNi and (c) Ti/thick *h*-BN/CuNi RRAM devices.

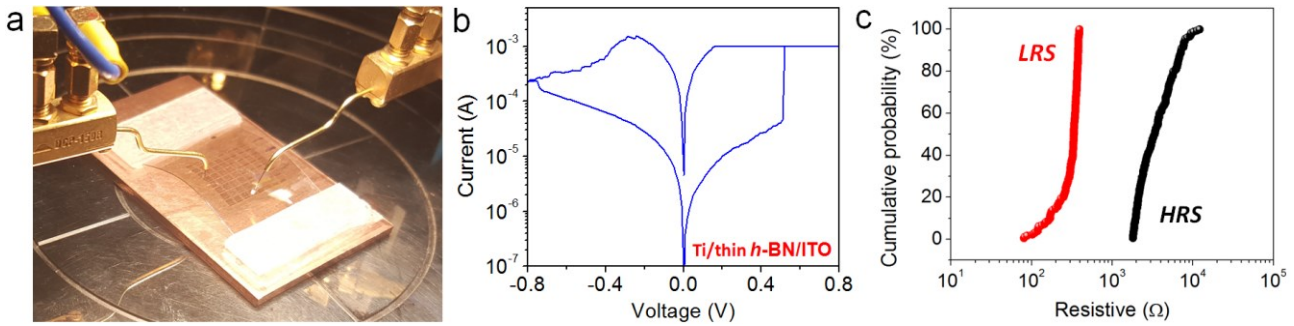

Figure 4: (a) Photograph of the Ti/thin *h*-BN/ITO devices during probestation test. (b) Typical RS behaviour observed in these cells under a curvature radius of 4 cm. (c) Cumulative distribution of the resistance during HRS and LRS during 180 cycles (read at 0.1V).

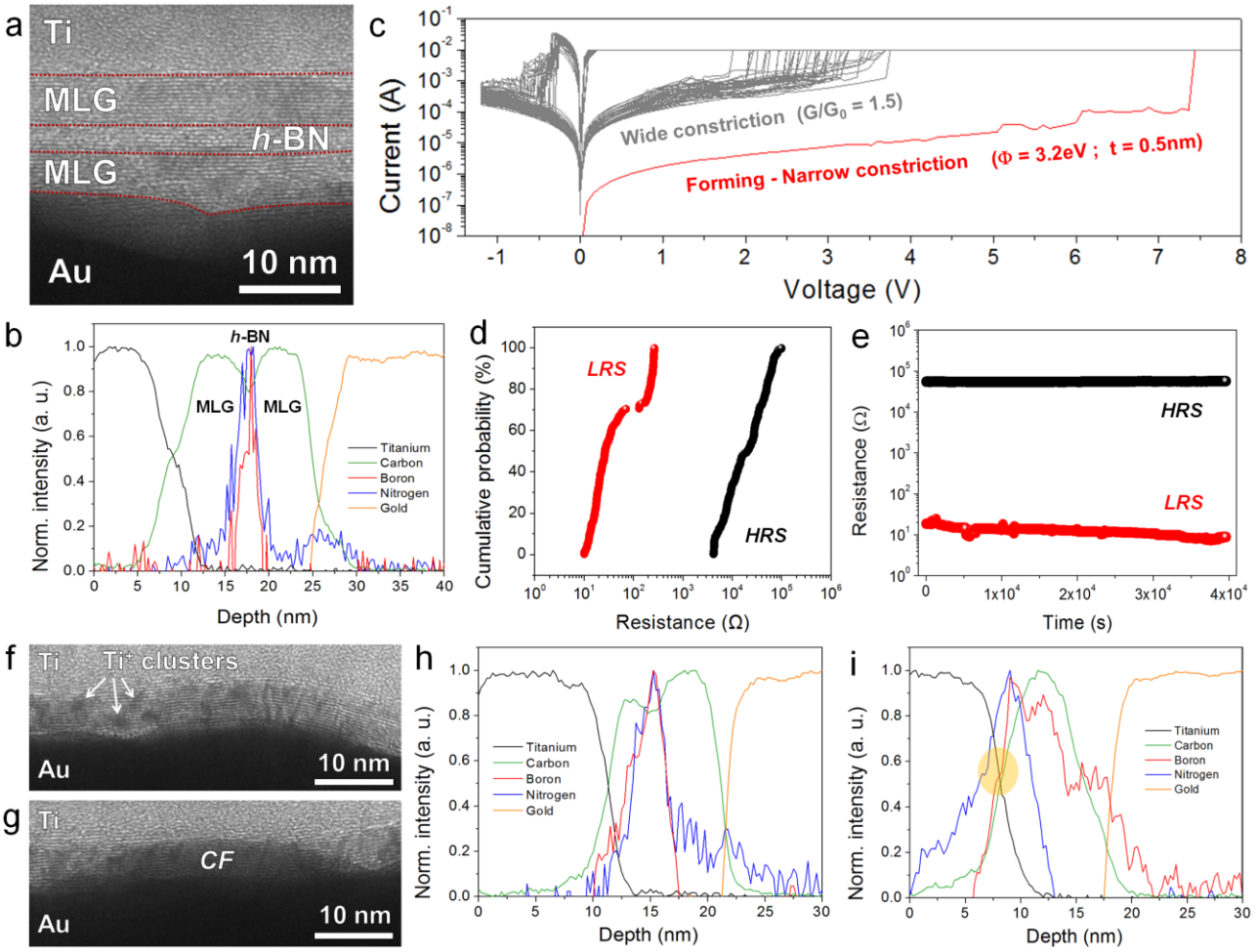

Figure 5: (a) XTEM image and (b) EELS cross sectional analyses of a Ti/MGL/*h*-BN/MLG/Au RRAM device demonstrating the correct fabrication (respectively). (c) Typical *I-V* curves collected in a 100 µm x 100 µm Ti/MLG/*h*-BN/MLG/Au RRAM showing set and reset transitions. More than 450 cycles have been collected, but here we only plot 50 cycles for clarity. The currents before and after the forming event have been fitted to the QPC model (details on the fitting parameters can be found in SI); (d) Cumulative distribution of the resistance per cycle in HRS and LRS during 400 cycles (read at 0.1V). (e) Current vs. time curves measured at 0.1V in HRS and LRS proving long state (data) retention. (f) and (g) XTEM images of a partially and completely formed CF though the 2D materials (respectively). (h) and (i) EELS profiles collected at the same locations than (g) and (h) respectively, showing clear Ti penetration into the *h*-BN until reaching the bottom graphene electrode (orange circle).

Row	Structure	Transfer needed	Bipolar RS under positive set	Forming process needed	V_{SET} I_{SET}	V_{RESET} I_{RESET}	I_{ON}/I_{OFF}	Endurance cycles	Retention time	Bipolar RS under negative set	Threshold RS
1	Ti/thin *h*-BN/Cu	NO	YES	NO	0.4V 4×10^{-4}A	-0.3V 4×10^{-3}A	10	> 350	-	NO	YES
2	Ti/thick *h*-BN/Cu	NO	YES	NO	0.7V 4×10^{-6}A	-0.7V 10^{-2}A	10^4	> 600	-	YES	YES
3	Ti/thin *h*-BN/CuNi	NO	YES	YES	0.7V 4×10^{-3}A	-0.4V 2×10^{-2}A	15	-	-	NO	NO
4	Ti/thick *h*-BN/CuNi	NO	YES	YES	6V 10^{-3}A	-2V 10^{-1}A	10^6	-	-	YES	NO
5	Ti/thin *h*-BN/ITO	YES	YES	NO	0.4V 2×10^{-4}A	-0.3V 10^{-3}A	10	> 180	-	NO	NO
6	Ti/MLG/thin *h*-BN/ MLG/Au	YES	YES	YES	2.3V 10^{-3}A	-0.6V 4×10^{-2}A	10^3	> 450	4×10^4 s	NO	NO

Table 1: Comparison of the performances observed for all the *h*-BN based RRAM devices here studied. The devices in rows 5-6 were fabricated by transferring thin *h*-BN previously grown by CVD on CuNi substrates, the devices in rows 1-5 are flexible, and the devices in row 5 are also transparent. The symbol "-" indicates that this property has not been investigated. The endurance column shows the maximum number of cycles measured, and it does not represents the lifetime of the devices, as degradation was not observed. In general, very good correlation between fabrication parameters and device properties can be observed: *i)* the need of forming and the presence of threshold RS can be controlled by using Cu or CuNi substrates, and *ii)* the presence of high current on/off ratios and bipolar RS under negative set can be enabled using thick *h*-BN stacks.

Supporting Information

Coexistence of Grain-Boundaries-Assisted Bipolar and Threshold Resistive Switching in Multilayer Hexagonal Boron Nitride Coupled with Solid and Liquid Electrodes

Chengbin Pan, Yanfeng Ji, Na Xiao, Fei Hui, Kechao Tang, Yuzheng Guo, Xiaoming Xie, Francesco M. Puglisi, Luca Larcher, Enrique Miranda, Lanlan Jiang, Yuanyuan Shi, Ilia Valov, Paul C. McIntyre, Rainer Waser and *Mario Lanza**

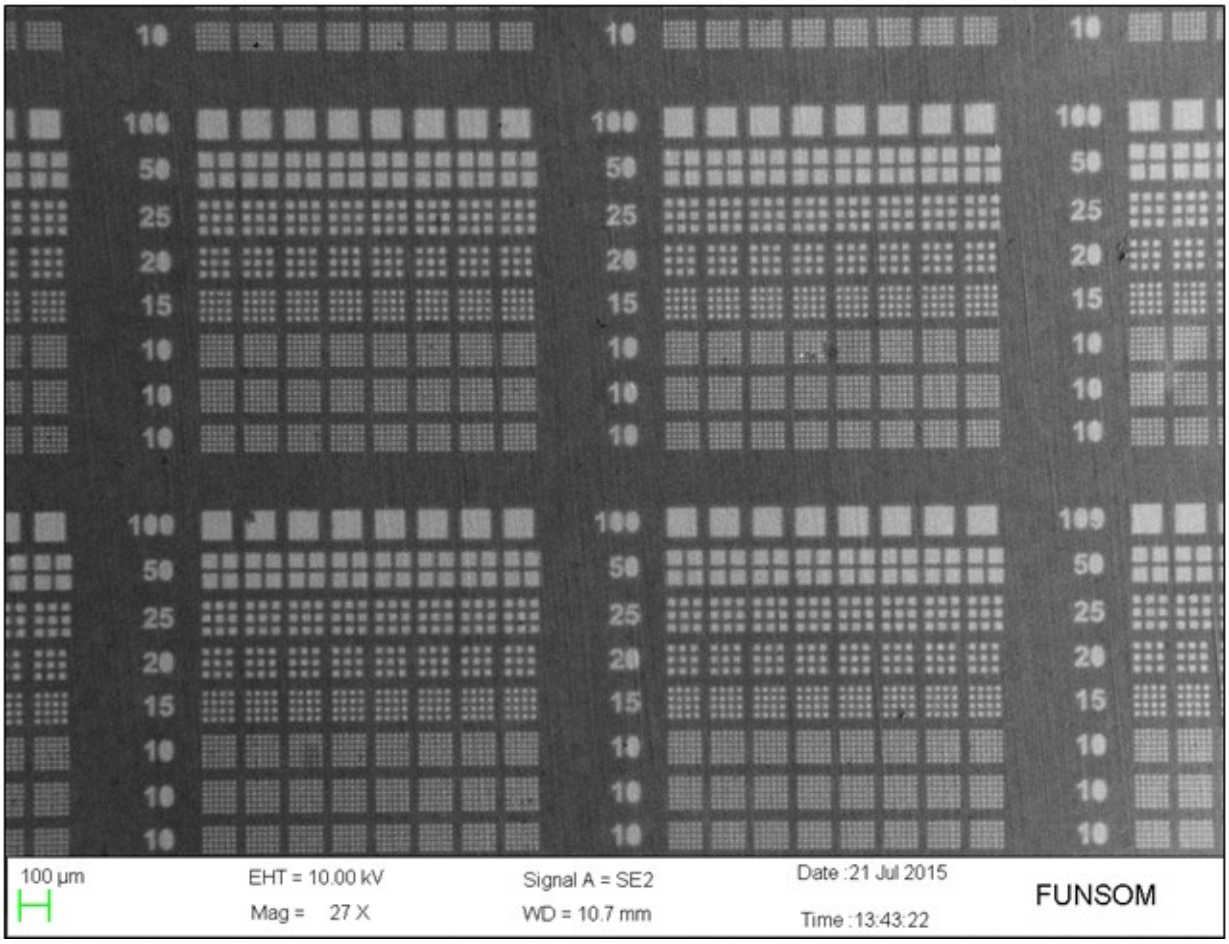

Fig. S1: SEM image of the matrixes of electrodes patterned on the Ti/thin *h*-BN/Cu sample. The same pattern has been used for all the samples studied in this investigation.

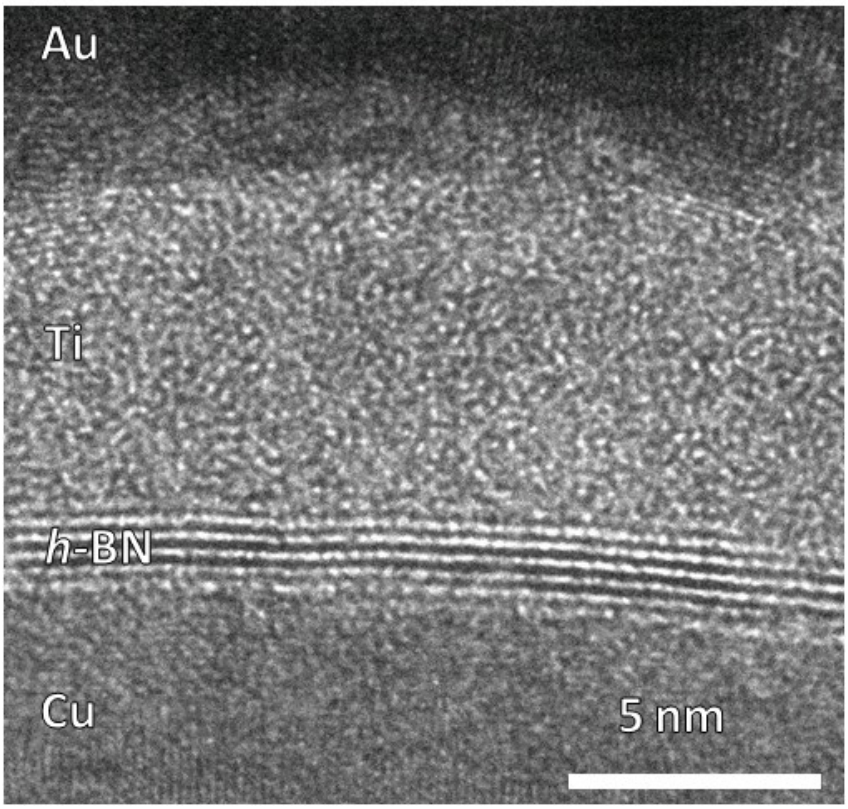

Fig. S2: Cross sectional TEM image of the fresh Ti/thin *h*-BN/Cu RRAM cell proving the thickness of the *h*-BN stack. For the thin *h*-BN grown on Cu, more than 25 TEM images at different locations were collected, and the thickness always ranged between 5 and 7 layers.

Electronic transport based on the Landauer approach

According to the Landauer formula for mesoscopic conductors,[S1] the current in atom-sized filamentary structures can be expressed as:

$$I = NG_0V \quad \text{(Eq.1)}$$

N is the number of conducting channels, *V* is the applied voltage and $G_0=2e^2/h$ is the quantum conductance unit. *e* is the electron charge and *h* is the Planck's constant. *N* can be interpreted as the combination of the number of sub-bands in a single filament and the number of parallel conducting filaments that effectively contribute to the total current. The linear *I-V* relationship obtained from Eq.1 is represented in Fig. S3a for different values of *N* (solid lines). The steps correspond to the partial or total dissolution of filaments caused by atomic rearrangements during the reset process. Figs. S3b and S3c illustrates the set and reset processes for a single device. The lowest experimental conductance values detected correspond to G/G_0 . 1 which is the conductance value for a monomode ballistic conductor. G_0 is the quantum conductance unit. The upper *I-V* characteristics in HRS in Figs. S3b and S3c indicate that some filaments cannot be turned off and remain activated during the whole switching process. These conductance values are consistent with electron transport through atom-sized constrictions.[S2]

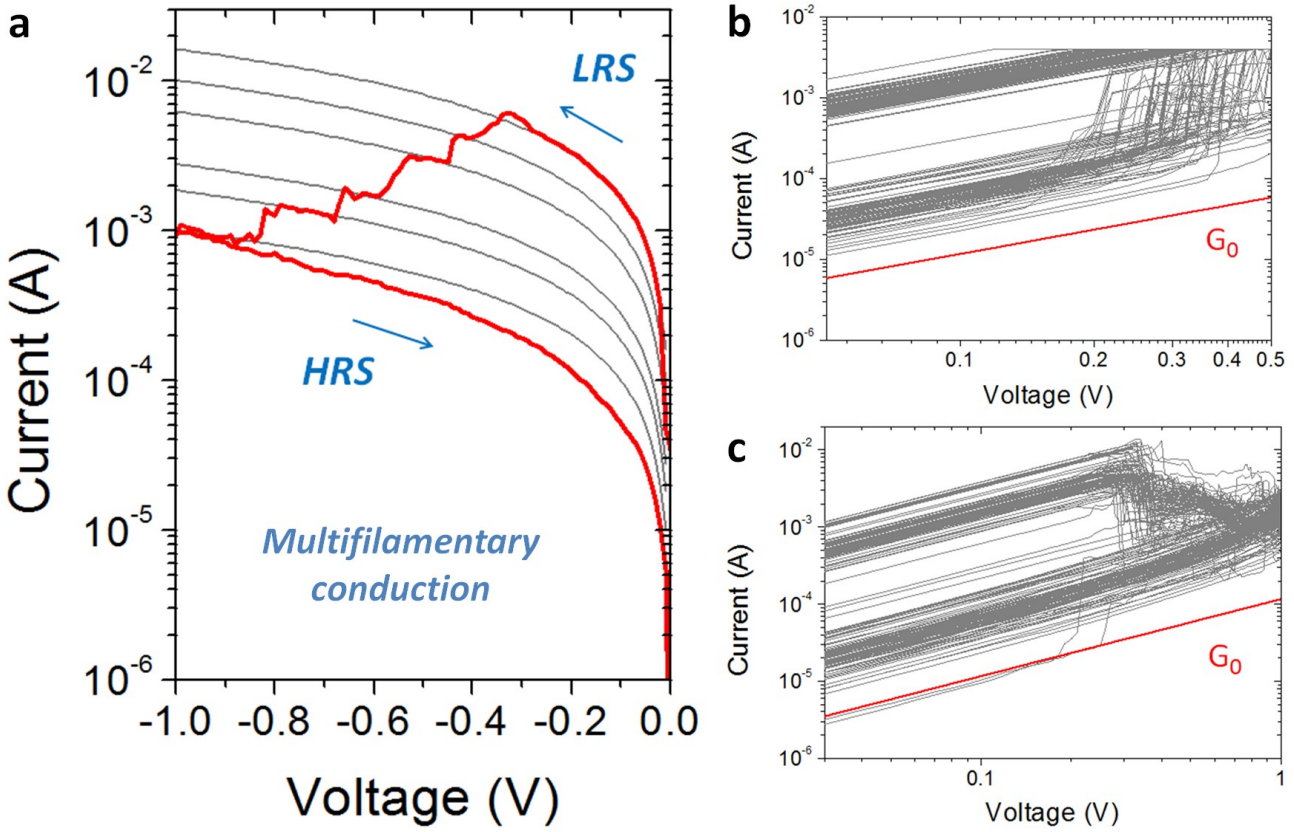

Fig. S3: (a) Reset process in the Ti/thin *h*-BN/Cu sample displaying the progressive rupture of many filaments in the sample (red line). The grey lines are fittings calculated using the QPC model. (b) and (c) show the log-log plot for the set (left) and reset (right) processes (respectively) of more than 100 *I-V* curves. The proximity of the HRS currents to the value of the quantum conductance (G_0) indicates that the percolation paths have diameters of few atoms, in agreement with Fig. 1c of the main text.

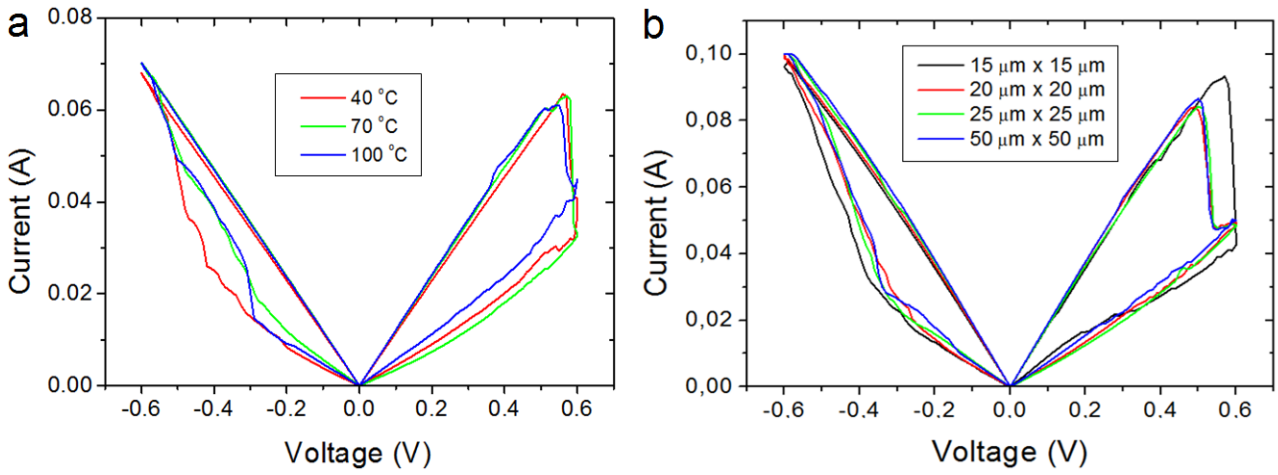

Fig. S4: (a) Typical *I-V* curves collected in a 100 µm x 100 µm cell at different temperatures. (b) Typical *I-V* curves collected in devices with different areas. The images show no temperature/area dependences, as the differences in the currents are very small and within the intrinsic cell-to-cell deviations.

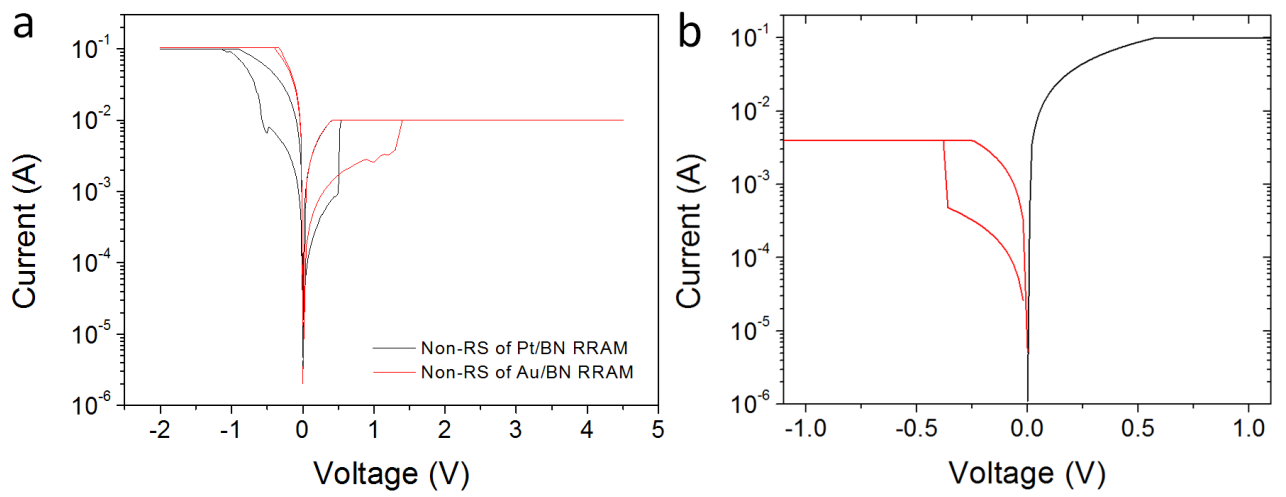

Fig. S5: (a) Typical *I-V* curves observed when applying ramped voltage stresses with different polarities to *h*-BN based devices using top Pt or Au electrodes (single metal, without Ti). In both cases no reset process has been observed. (b) Typical *I-V* curves observed when applying ramped voltage stresses with different polarities (starting with a negative ramp) to the Ti/thin *h*-BN/Cu ReRAM devices (similar to those in Fig. 1a of the main text). It can be observed that after negative set, the device cannot be reset.

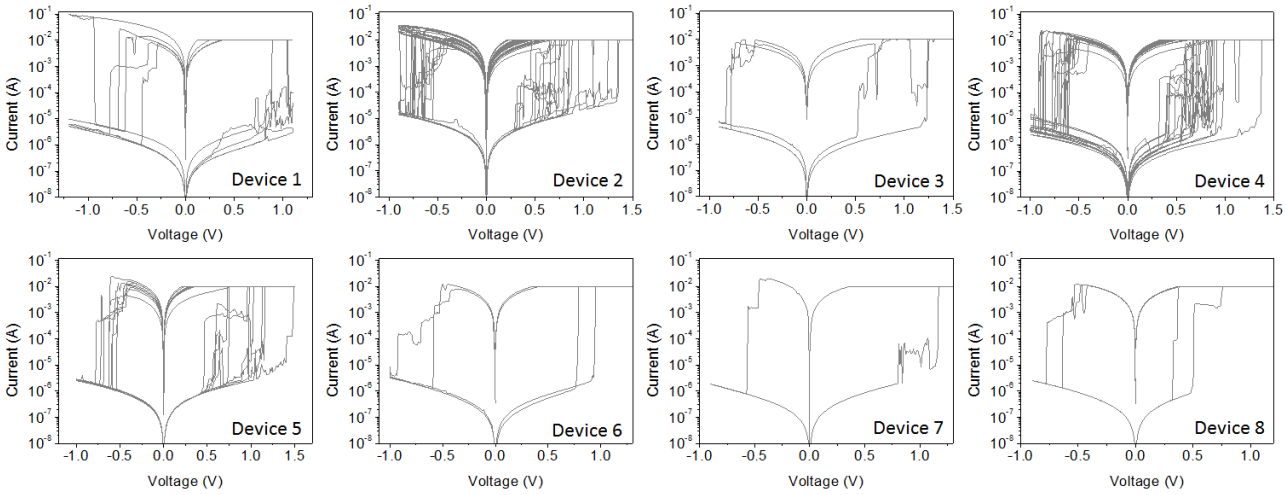

Fig. S6: Typical RS behaviour observed in eight different Cu/thick *h*-BN/Cu RRAM devices similar to those in Fig. 3 of the main text. For clarity only few cycles are shown. The absolute value and the device-to-device variability of V_{SET} and V_{RESET} is in all cases below 1V and the deviations of I_{SET} and I_{RESET} are always below one order of magnitude.

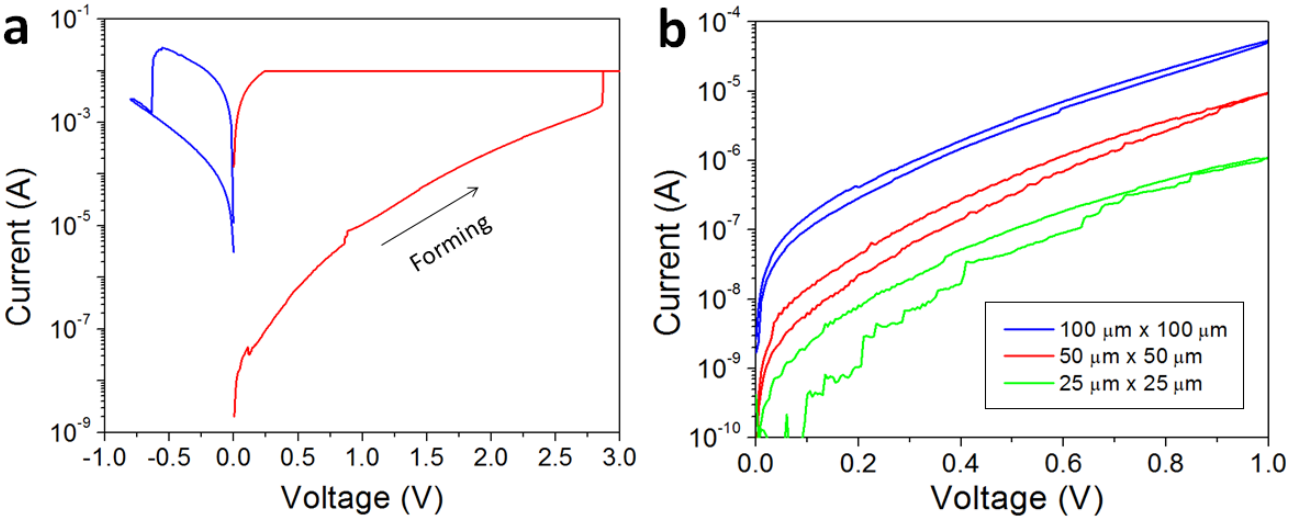

Fig. S7: (a) Typical forming process observed in Ti/thin *h*-BN/CuNi devices. (b) *I-V* curves collected in Ti/thin *h*-BN/CuNi devices showing the pre-breakdown area dependence.

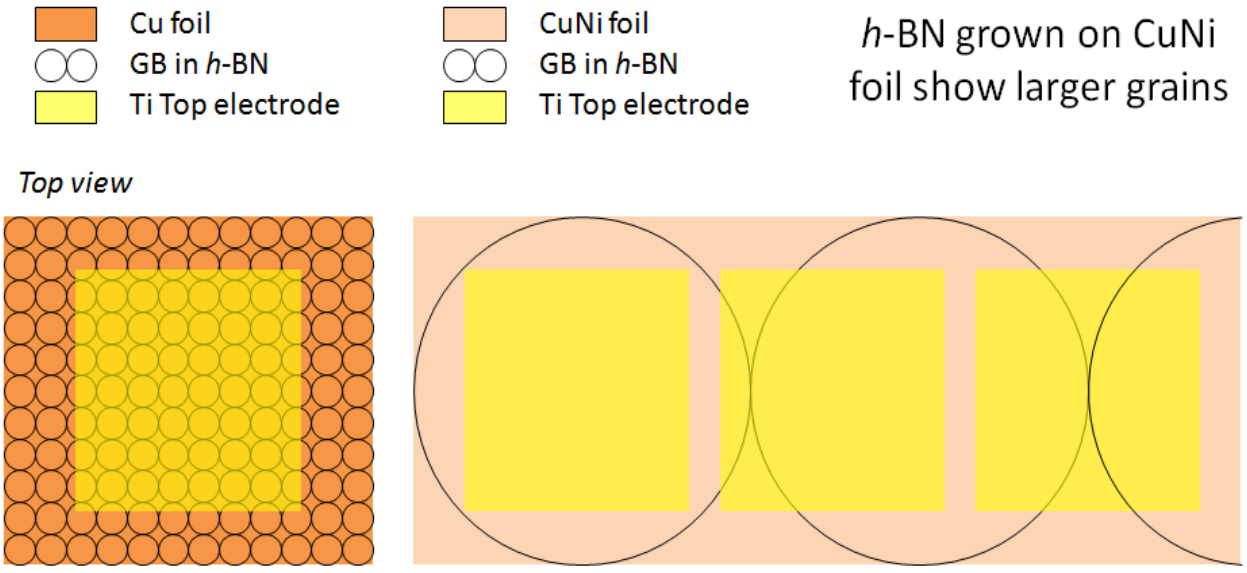

Fig. S8: Schematic explanation for the lower HRS currents observed in the devices fabricated using CuNi as bottom electrode. The lower density of GBs within the capacitor area, and therefore the lower density of partially formed CFs, reduces the total current in HRS.

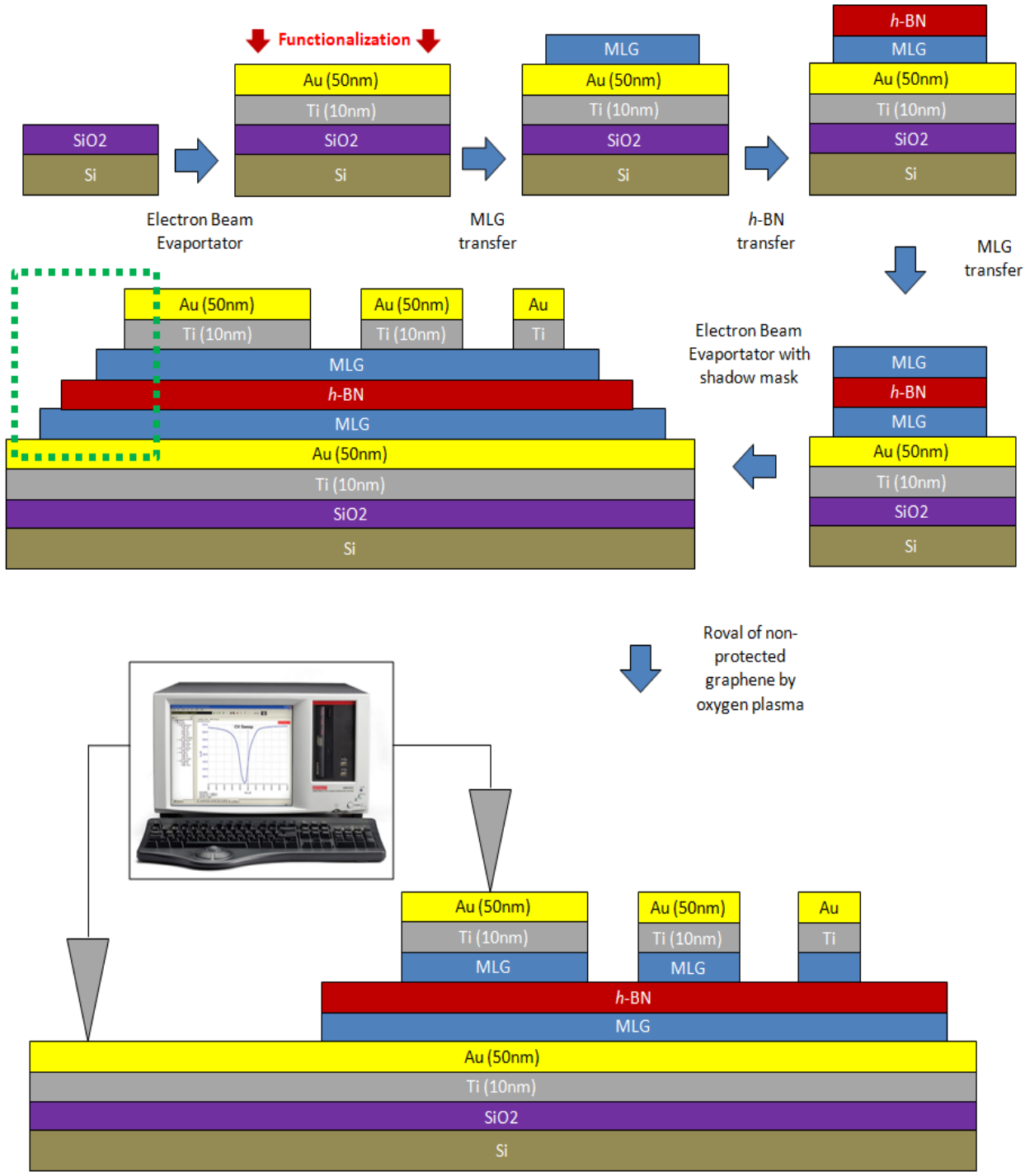

Fig. S9: Schematic displaying the fabrication of Ti/MLG/thin *h*-BN/MLG/Au devices. The area highlighted with a green dotted square is characterized in Fig. 6 of the main text.

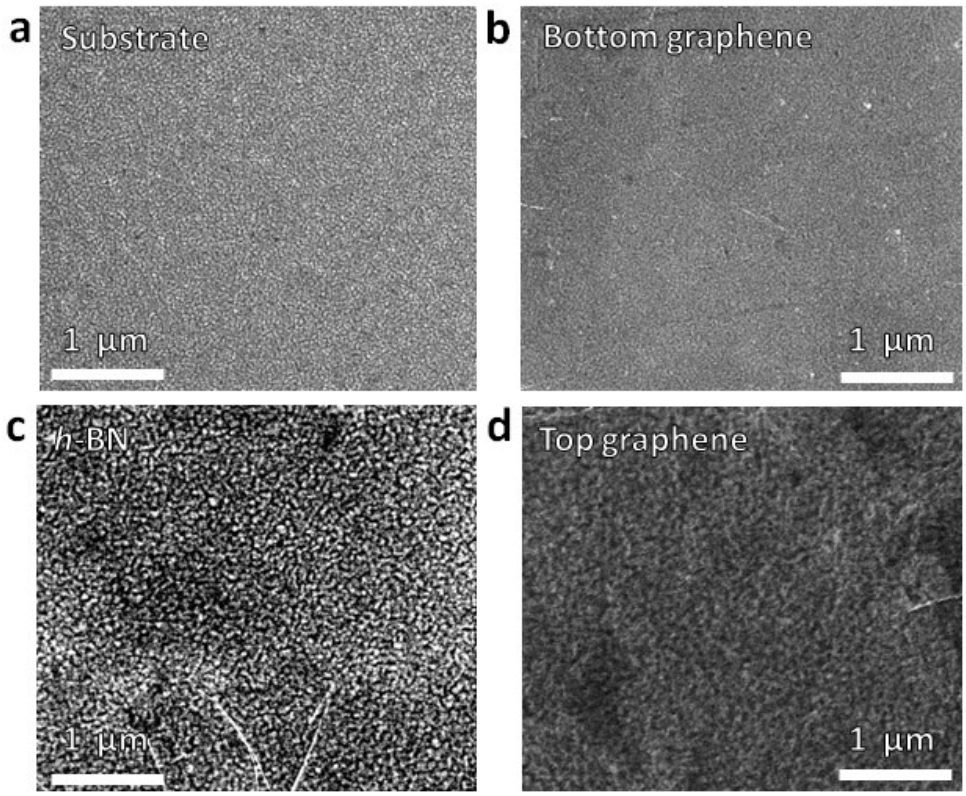

Fig. S10: SEM characterization of Ti/MLG/thin *h*-BN/MLG/Au RRAM devices on the different layers, including the substrate (a), bottom MLG (b), h-BN (c) and top MLG (d).

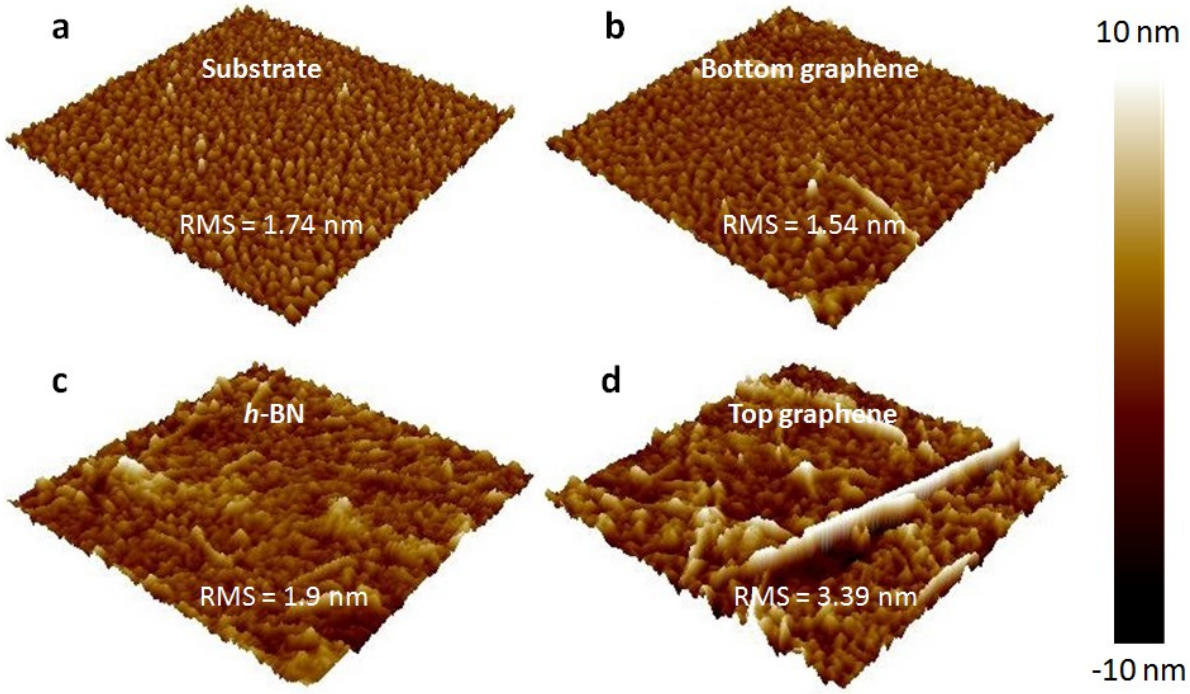

Fig. S11: Topographic AFM characterization of Ti/MLG/thin *h*-BN/MLG/Au RRAM devices on the different layers, including the substrate (a), bottom MLG (b), h-BN (c) and top MLG (d).

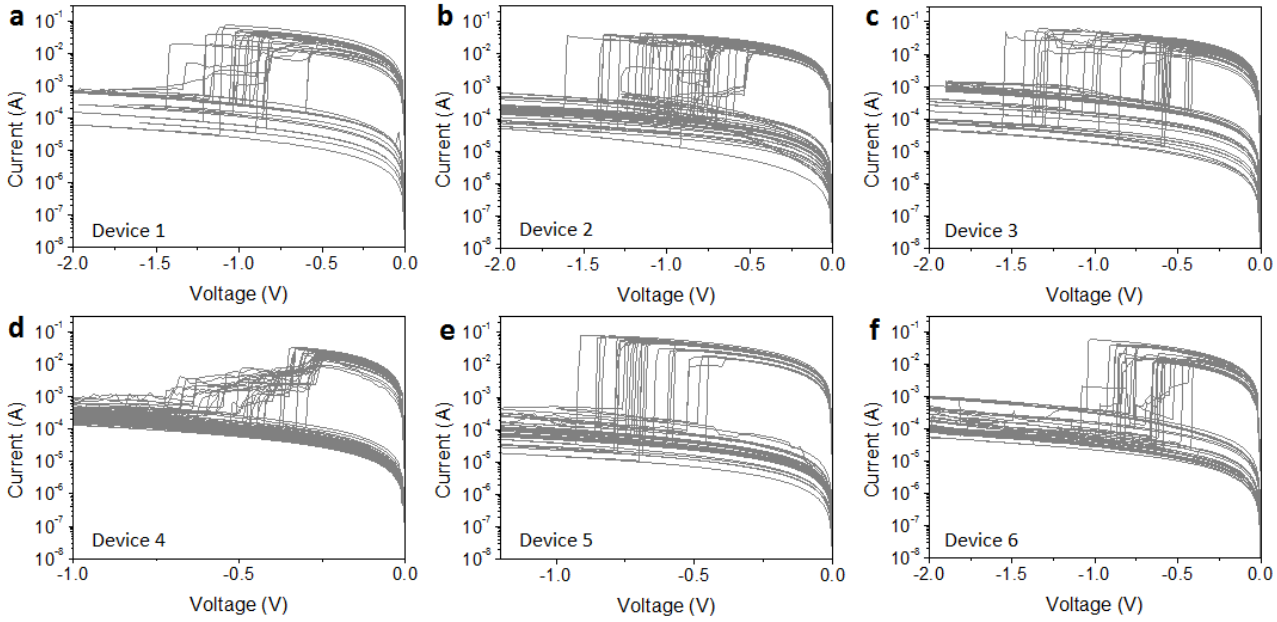

Fig. S12: Typical reset process observed in six different Ti/MLG/thick *h*-BN/MLG/Au RRAM devices. The devices mainly show a reset process much sharper than the metal/*h*-BN/metal ones. The device-to-device variability of V_{RESET} is very small, and in all cases it is below 1V.

Fitting of the *I-V* curves collected in graphene/*h*-BN/graphene RRAM cells

As illustrated in Fig. 6d of the main text, the initial *I-V* characteristic collected (forming process) in the Ti/MLG/thin *h*-BN/MLG/Au RRAM devices has been fitted to the QPC model equation:[S2]

$$I = \frac{4e}{\alpha h} e^{-\alpha\Phi} sinh\left(\frac{\alpha eV}{2}\right) \qquad \text{(Eq. 2)}$$

, where *e* is the electron charge, *h* the Planck's constant, α a parameter related to the longitudinal shape of the confinement barrier, and Φ the confinement barrier height measured from the equilibrium Fermi energy. Equation (2) assumes symmetrical potential drops at the two ends of the constriction (which is consistent with the symmetry of the experimental *I-V* curves) and indicates the presence of some kind of local barrier in the forming process (confinement barrier or material barrier). Notice also that when the barrier vanishes ($\alpha \rightarrow 0$ in Eq. 2), the current reads:

$$I = \frac{2e^2}{h} V \qquad \text{(Eq. 3)}$$

which is nothing but the standard Landauer formula (Eq. 1) for a monomode ballistic conductor. In this case, the fitting parameters (green line) correspond to a confinement barrier of 0.5 nm width (which is consistent with the distance between the *h-BN* planes) and height of 3.2 eV (which is very similar to the values in reference S3). As in the previous cases, the HRS as well as the LRS *I-V* curves are above the quantum conductance unit limit G_0. The minimum conductance value detected

above this limit is G/G_0=1.5. The red solid line was obtained using Eq. 1 (in this Supplementary Information document), with N=1.5. Notice that N does not need to be necessarily an integer number for atom-sized constrictions.[S3]

Supplementary References

[S1] Datta, S. Electronic transport in mesoscopic systems, cambridge studies in emiconductor physics and microelectronic engineering. Cambridge University Press (1997).

[S2] Ruitenbeek, J. v., Masis, M. M. & Miranda, E. in Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications, Chapter 7: Quantum Point Contact Conduction. (2016).

[S3] Pauly, F. *et al.* Theoretical analysis of the conductance histograms and structural properties of Ag, Pt, and Ni nanocontacts. *Phys. Rev. B* **74,** 235106 (2006).