ISSN 0005–1144
ATKAAF 36(1–2), 35–40 (1995)

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Computer-aided Time-Domain Analysis of Switched Networks

UDK 621.314.57.012.6:519.688
IFAC IA 4.0.5.4; 2.6

Preliminary communication

A new computer-oriented method for an efficient and accurate large-signal time-domain analysis of switched networks is presented. Switched networks consisting of strictly linear elements and of a wide class of switches can be investigated. An ideal switch model is assumed and the state equation method is adopted for the network analysis. When a network topology changes, state equations are derived systematically by means of a generalized formulation of p-port constraint matrices. Each set of equations holds from a switching instant to the next one which is calculated through a Newton-type algorithm. Numerical results are compared with experimental data and SPICE simulations.

Key words: Circuit analysis, static converters, switched networks

1. INTRODUCTION

Switched linear networks consist of linear elements and switches that may be externally controlled or may change states at times which must be determined as the analysis progresses. In this paper networks with both type of switches are considered. Such networks are referred to as »internally controlled switched networks«. The importance of these networks is due to their technical applications that include switching power converters, nonideal switched-capacitor filters, analog-to-digital converters, etc.

Modelling and analysis of switched networks can be developed through two different approaches: small-signal analysis and large-signal analysis. Small-signal analysis techniques are not applicable when a network experiences large-signal changes. For instance, a step change in the supply voltage or load impedance can involve a crossover between distinct modes of operation. In these cases a large-signal analysis is required.

Large-signal time-domain analysis methods based either on the state variable formulation [1–3], or on a nodal analysis technique [4] have been proposed for internally controlled switched networks. The aim of this paper is to describe a general analysis method based on the state variable formulation with the following features:

- State equations are derived systematically. The method is not topology specific and does not require prior knowledge of the circuit operation to be used effectively.
- There is no restriction on the circuits that can be analysed as far as the number of switches (and hence topologies) is concerned.
- Both constant and sinusoidal input sources are considered.

In Section 2 the method of analysis is highlighted. Examples of application of the proposed method to the analysis of a rectifier and a dc–dc converter are discussed. Numerical results are compared with experimental data and SPICE simulations.

2. METHOD OF ANALYSIS

Switched networks contain energy-storage elements, controlled switches (SCR, MOSFET, BJT, GTO, etc.), diodes and a control system.

All switching elements are assumed to be ideal, i.e. with zero impedance (a short circuit) when ON and zero admittance (an open circuit) when OFF. Switching from one state to another is instantaneous. A switch can be driven by voltages and/or currents in the circuit or by a control system. During operation the state of a switch changes in time so that the network is time-varying and can be modelled as a sequence of linear circuit topologies.

The analysis proceeds as follows. At any given time, each switch is in a particular state (ON or OFF), and the circuit contains only linear elements arranged in a corresponding topology. The first issue is to obtain the state equations and the output equations for the topology under consideration. Such equations are integrated until cir-

cumstances cause one or more switches to change states. The accurate calculation of the switching instants is required to determine the correct topology after switching (multiple switching must be permitted). The topology is updated and the procedure has to be repeated.

2.1. Formulation of state equations and output equations

For each topology the following set of state equations and output equations must be obtained

$$\begin{aligned} \dot{\bar{x}} &= \bar{A}_i \bar{x} + \bar{B}_i \bar{u} \\ \bar{y} &= \bar{C}_i \bar{x} + \bar{D}_i \bar{u} + \left(\bar{D}_{1i} \dot{\bar{u}} + \ldots\right) \end{aligned} \tag{1}$$

where $\bar{x}$ is the vector of the state variables, $\bar{A}_i$, $\bar{B}_i$, $\bar{C}_i$, $\bar{D}_i$, $\bar{D}_{1i}$,... are matrices the elements of which are real constants derived from the ith circuit topology and the circuit parameters, $\bar{u}$ is the vector of the input variables and $\bar{y}$ the vector of the output variables of interest [5].

In order to obtain (1) for a switched network, a generalized formulation of p-port constraint matrices is introduced [6]. For a given p-port, the constraint equations are the maximum number of independent equations relating the port variables in the form

$$\bar{K} \begin{bmatrix} \bar{i}_p \\ \bar{v}_p \end{bmatrix} = \bar{0} \tag{2}$$

where $\bar{K}$ is called a *constraint matrix* for the p-port [5].

For a switched network it is considered the p-port obtained by extracting:

- All energy-storage reactive elements.
- All independent sources.
- All branches which contain switches.
- A short circuit in series with each branch the current of which either controls a switch or must be calculated as output variable.
- An open circuit in parallel with each branch the voltage of which either controls a switch or must be calculated as output variable.

The resulting p-port, consisting of only linear resistors, does not vary when the network topology changes. Consequently a constraint matrix must be calculated only once at the initial stage of the procedure.

Ports connected to independent voltage sources, capacitors, ON-state switches and short circuits are said to be voltage ports, whereas ports connected to independent current sources, inductors, OFF-state switches and open circuits are said to be current ports. For convenience, the port variables are ordered and grouped as follows

$$\begin{bmatrix} \bar{i}_p \\ \bar{v}_p \end{bmatrix} = \left[\tilde{\bar{u}} \quad \bar{y} \quad \tilde{\bar{x}} \quad \bar{u} \quad \bar{0} \quad \bar{x}\right]^T \tag{3}$$

where

$$\begin{aligned} \tilde{\bar{u}} &= \left[\bar{i}_{vs} \quad \bar{v}_{cs} \quad \bar{i}_{ON} \quad \bar{v}_{OFF}\right]^T \\ \bar{y} &= \left[\bar{i}_{sc} \quad \bar{v}_{oc}\right]^T \\ \tilde{\bar{x}} &= \left[\bar{i}_C \quad \bar{v}_L\right]^T \\ \bar{u} &= \left[\bar{i}_{cs} \quad \bar{v}_{vs}\right]^T \\ \bar{0} &= \left[\bar{i}_{OFF} \quad \bar{v}_{ON} \quad \bar{i}_{oc} \quad \bar{v}_{sc}\right]^T \\ \bar{x} &= \left[\bar{i}_L \quad \bar{v}_C\right]^T \end{aligned} \tag{4}$$

The subscripts vs, cs, ON, OFF, sc, oc, C and L, indicate independent voltage sources, independent current sources, ON-state switches, OFF-state switches, short-circuit elements, open-circuit elements, capacitors and inductors, respectively.

From (4) one can observe that the currents of the current ports other than those connected to inductors, and the voltages of the voltage ports other than those connected to capacitors, are either known–valued variables or zero-valued variables.

The constraint matrix $\bar{K}_i$, corresponding to the ith circuit topology and the order of the port variables stated in (3), is calculated by the procedure described in [5].

It is noteworthy to observe that when the state of a switch (for instance, the kth switch) changes, the nature of its corresponding port varies from a current port to a voltage port or vice versa. In this case in the vector $\tilde{\bar{u}}$ the current (voltage) of the kth switch is replaced by the corresponding voltage (current) and in the vector $\bar{0}$ the opposite replacement is made. As a consequence, the arrays of the $\bar{K}_i$ matrices for different topologies, differ only for the exchange of columns that correspond to ports connected to switches.

The $\bar{K}_i$ matrices can be reduced by means of elementary row operations to echelon form [5] and it is possible to obtain from (2) and (3) for the ith circuit topology

$$\begin{bmatrix} \bar{I} & \cdots & \cdots & \cdots & \cdots & \cdots \\ \bar{0} & \bar{I} & -\bar{C}^{*}_{1i} & -\bar{D}'_{i} & \cdots & -\bar{C}'_{i} \\ \bar{0} & \bar{0} & \bar{M}^{*}_{i} & -\bar{B}'_{i} & \cdots & -\bar{A}'_{i} \end{bmatrix} \begin{bmatrix} \dot{\bar{u}} \\ \bar{y} \\ \dot{\bar{x}} \\ \bar{u} \\ \bar{0} \\ \bar{x} \end{bmatrix} = \bar{0} \qquad (5)$$

In (5) the submatrices of interest are indicated.

Substituting into (5) the element constitutive relations for all energy-storage reactive elements

$$\bar{i}_C = \bar{C}\frac{\mathrm{d}\bar{v}_C}{\mathrm{d}t}, \quad \bar{v}_L = \bar{L}\frac{\mathrm{d}\bar{i}_L}{\mathrm{d}t} \qquad (6)$$

and indicating the $\bar{C}_{1i}{}^{*}$ and $\bar{M}_i{}^{*}$ submatrices as $\bar{C}'_{1i}$ and $\bar{M}_i$ after such substitutions, (5) can be rewritten in the form

$$\begin{bmatrix} \bar{I} & \cdots & \cdots & \cdots & \cdots & \cdots \\ \bar{0} & \bar{I} & -\bar{C}'_{1i} & -\bar{D}'_{i} & \cdots & -\bar{C}'_{i} \\ \bar{0} & \bar{0} & \bar{M}'_{i} & -\bar{B}'_{i} & \cdots & -\bar{A}'_{i} \end{bmatrix} \begin{bmatrix} \dot{\bar{u}} \\ \bar{y} \\ \dot{\bar{x}} \\ \bar{u} \\ \bar{0} \\ \bar{x} \end{bmatrix} = \bar{0} \qquad (7)$$

where $\dot{\bar{x}}$ is the vector of the time derivatives of $\bar{v}_C$ and $\bar{i}_L$.

From (7) the following equations can be obtained

$$\bar{M}_i\dot{\bar{x}} = \bar{A}'_i\bar{x} + \bar{B}'_i\bar{u}$$

$$\bar{y} = \bar{C}'_{1i}\dot{\bar{x}} + \bar{C}'_i\bar{x} + \bar{D}'_i\bar{u} \qquad (8)$$

In (8) the vector $\bar{x}$ consists of all capacitor voltages and inductor currents, which are not necessarily linearly independent. The next task is to uncover possible dependent variables in $\bar{x}$, to eliminate them and to reduce (8) to the form (1). One procedure for achieving this goal is a recursive process illustrated in [5].

The described procedure is efficiently adaptable for a digital computer. Furthermore the matrices required during the analysis are calculated once and stored for later use. In this way the computational effort is reduced and the fastness of the procedure increased.

2.2. Integration methods

Particular attention must be paid to the integration procedure. Methods that perform well for time-invariant networks, may fail or may be unreliable when used for time-varying ones. The major problem is the choice of the integration time step which cannot be either too large to include several switching events or too small. In the former case the analysis may fail in the prediction of the correct evolution of the network, in the latter an excessively high computational effort, especially for high switching frequencies, is to be expected. Three different numerical algorithms have been implemented:

- Evaluation of the state transition matrix by means of truncated expansions.
- Fourth-order Runge-Kutta algorithm with error control.
- Variable-order, variable-step Gear's stiffly stable algorithm.

The procedures 1 and 2 are fixed step algorithms and, to be used effectively, a very careful choice of the time step is required. For well chosen time steps both algorithms are very fast when compared with SPICE simulations. On the other hand they present a narrow range of suitable time steps. Gear's algorithm needs somewhat longer CPU times than the others (from twice to four times as much) but it gives always a solution provided that the starting time step is not too large.

2.3. Switching instant calculation

After each time step the vector $\bar{y}'$, the elements of which are the output variables influencing the state of the switches, is compared with the vector of the corresponding threshold values $\bar{h}$. When a crossover of the threshold value occurs for one or more variables, the corresponding swit-ches change their states at instants which satisfy the following set of equations

$$\bar{y}'(t) = \bar{h} \qquad (9)$$

Equation (9) is generally nonlinear and is solved through a Newton-type algorithm coupled with a binary search strategy.

3. NUMERICAL AND EXPERIMENTAL RESULTS

The described method has been implemented in a computer code and the results of the analysis for two simple switched networks are here reported.

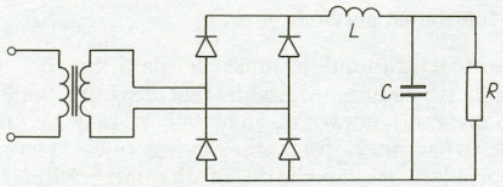

Fig. 1. Shematic of ac–dc converter

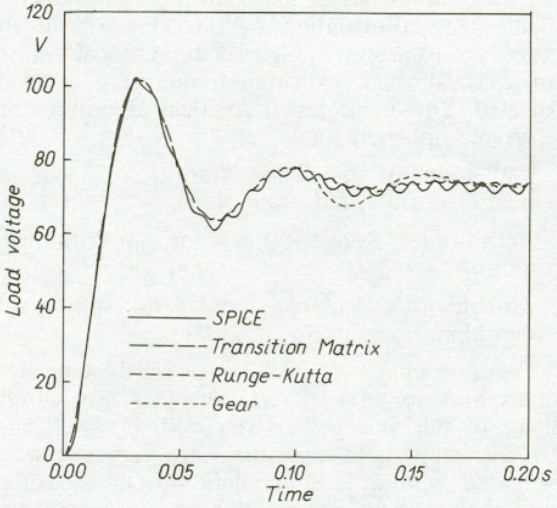

Fig. 2. Calculated load voltage waveform of the ac–dc converter of Fig. 1.

The single-phase ac–dc converter in Fig. 1 is one of the two examined networks. Fig. 2 shows the load voltage vs. time curves calculated by SPICE and by solving the equations of the proposed method of analysis through the integration algorithms considered in 2.2. In the simulation it has been assumed that, at the starting time $t = 0$, the circuit is in the zero-state and the sinusoidal supply voltage is equal to zero. The responses obtained by the transition matrix evaluation and the Runge-Kutta algorithm, with the same time step and numerical accuracy, are practically coinciding. Gear's algorithm is less accurate mainly because it utilizes greater time steps in the calculation of the last part of the response. As a consequence, the numerical approximation of the sinusoidal supply voltage, which is kept constant during each time step, becomes less accurate. SPICE is not based on the ideal switch model and this can explain a different voltage ripple in the SPICE simulation. The CPU-time required by SPICE is about eight times the one required by Gear's algorithm which is the slowest in our approach.

The experimental load voltage waveform of the ac–dc converter is shown in Fig. 3. The difference between the calculated and measured curves

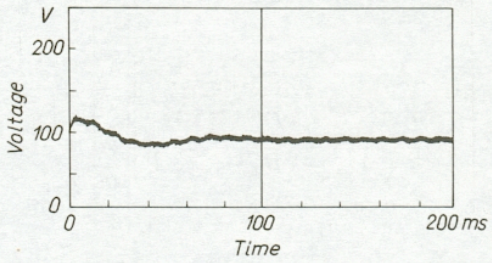

Fig. 3. Experimental load voltage waveform of the ac–dc converter of Fig. 1.

in the initial instants depends on the fact that the value of the supply voltage at $t=0$, has been assumed to be equal to zero in the numerical analysis, whereas the experimental equipment was not provided with a device capable of switching on the supply voltage when it crosses the zero-value. This implies a difference in the transient response.

The latter network is the dc–dc buck converter, with PWM control technique, shown in Fig. 4.

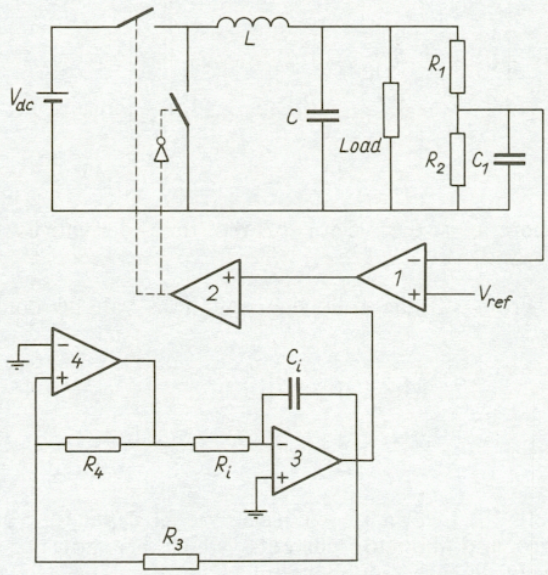

Fig. 4. Shematic of regulated dc–dc buck converter

The calculated load voltage waveform is plotted in Fig. 5. In this case the agreement between the results obtained by the different integration algorithms is very good. The converter shown in Fig. 4 has not been simulated with SPICE because it does not allow the PWM control system to be modelled by means of only basic circuit elements as it has been done with the proposed method. For this reason the comparison may have no significance.

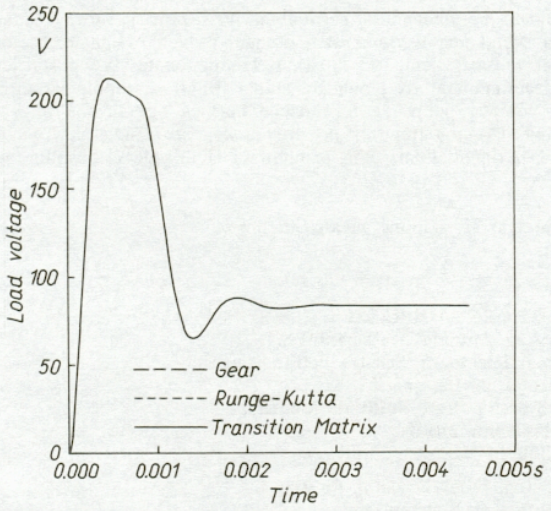

Fig. 5. Calculated load voltage waveform of the dc-dc converter of Fig. 4.

An experimental dc–dc buck converter with two MOSFET's (HEXFET n-channel IRF350) and the control system has been set up. The experimental load voltage waveform is shown in Fig. 6. A comparison between the curves of Figs. 5 and 6 shows a qualitative agreement. The discrepancies can be related to the difference between the real values and the rated ones of the component parameters, besides the approximations introduced into the control system model. The PWM control system has been modelled by means of simple circuit elements. In particular the comparators 2 and 4 in Fig. 4, are modelled as voltage-controlled switches, whereas the operational amplifier 1 as a voltage-controlled voltage source and the integrator 3 as a voltage-controlled current source. Nevertheless a peak value of about 210 V is calculated against a measured value of 180 V. Furthermore a better agreement is shown in the steady-state response where an average value of 83 V is calculated against a measured value of 78 V.

4. CONCLUSIONS

In this paper a method for the large-signal time-domain analysis of switched networks has been presented. All switches are assumed to be ideal and the analysis method is based on a state equation formulation for time-varying networks. When a topology occurs, state equations are derived systematically by means of a generalized formulation of p-port constraint matrices. Three different numerical integration algorithms have been successfully used and the results have been compared with experimental data and SPICE simulations.

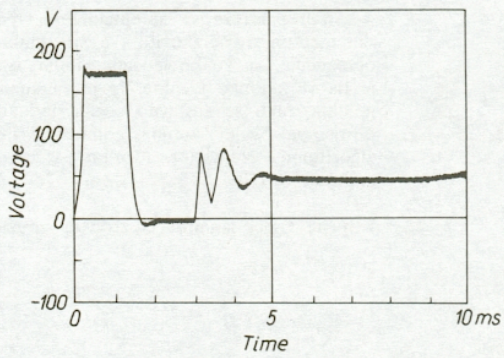

Fig. 6. Experimental load voltage waveform of the dc–dc converter of Fig. 4.

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Analiza mreža sa sklopkama u vremenskoj domeni potpomognuta računalom. Prikazana je nova računalska metoda za učinkovitu i točnu analizu mreža sa sklopkama u vremenskoj domeni za velike signale. Metoda omogućuje, za veliku lepezu sklopki, istraživanje mreža sastavljenih od linearnih komponenata. Predpostavljeno je da su sklopke idealne, te je za analizu mreže izabrana metoda jednadžbi stanja. Kako se topologija mreže mijenja, tako se sustavno izvode jednadžbe stanja pomoću poopćene formulacije matrica ograničenja mreža s p-pristupa. Svaka skupina jednadžbi vrijedi od jednog sklopnog trenutka do drugog koji se računa Newtonovim algoritmom. Numerički rezultati su uspoređeni s eksperimentalnim, te s rezultatima simulacije dobivenim programom SPICE.

Ključne riječi: analiza električkih mreža, statički pretvarači, sklopne električke mreže

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Primljeno: 1994–07–15

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