Electrical leakage phenomenon in heteroepitaxial cubic silicon carbide on silicon

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Abstract. Heteroepitaxial 3C-SiC films on silicon substrates are of technological interest as enablers to integrate the excellent electrical, electronic, mechanical, thermal and epitaxial properties of bulk silicon carbide into well-established silicon technologies. One critical bottleneck of this integration is the establishment of a stable and reliable electronic junction at the heteroepitaxial interface of the unintentionally n-type doped SiC with the silicon substrate. We have thus investigated into detail the electrical and transport properties of heteroepitaxial cubic silicon carbide films grown via different methods on low-doped and high-resistivity silicon substrates by using van der Pauw Hall and transfer length measurements as test vehicles. We have found that Si and C intermixing upon or after growth, particularly by the diffusion of carbon into the silicon matrix, creates extensive interstitial carbon traps and hampers the formation of a stable rectifying or insulating junction at the SiC/Si interface. Although a reliable p-n junction may be not realistic in the SiC/Si system, we can achieve, from a point of view of the electrical isolation of in-plane SiC structures, leakage suppression through the substrate by using a high-resistivity silicon substrate coupled with deep recess etching in between the SiC structures.

I. INTRODUCTION

Epitaxial cubic silicon carbide films on silicon (3C-SiC/Si and hereafter SiC/Si) have attracted extensive interest for semiconductor device applications such as high-voltage, high-frequency diodes, and heterojunction bipolar transistors.[1] This is because these structures offer access to the properties of SiC, such as its wide band gap and high thermal conductivity, on more conventional silicon substrates.[2] Despite these significant properties, no 3C-SiC based devices are currently commercially available[3] and this is likely due to problems associated with SiC/Si junctions.

We have recently shown that the expected p-n junction between a p-type silicon substrate to the 3C-SiC, naturally grown as unintentionally n-type, is either non-existing or

very unstable so that severe leakage or even plain shorting of the epitaxial silicon carbide to the underlying silicon substrate[1] is typically found.[4, 5] The absence of a stable p-n junction at the SiC/Si interface could pose important limitations to the applications of 3C-SiC in power electronics, harsh environment, MEMS, LEDs, graphene-based devices, etc.[2]

To date, a few studies have been conducted on the properties of SiC/Si junctions, however, electrical leakage is linked to stacking fault defects in 3C-SiC.[2] Moreover, studies of strained heterostructures have shown that the substantial tensile strain generated from the lattice and thermal expansion coefficient mismatch between 3C-SiC and silicon may reduce the band gap of the SiC.[6] Nevertheless, a detailed explanation of the leakage/shorting phenomenon, and the impact of this challenge on the electrical properties of 3C-SiC layers and are poorly documented in the literature.

Suemitsu *et al*. have attempted the growth of SiC onto an intermediate insulating 4H-AlN layer on silicon in order to avoid the leakage of silicon atoms from the substrate through the SiC layer, which also hampered the graphitization of the SiC surface.[7] This indicates that the instability of the SiC/Si interface affects potential applications in more than one way.

In this work, we develop a complete understanding of the historically overlooked leakage problem in 3C-SiC on Si heterojunction system, by studying in detail the electrical behaviour of SiC films epitaxially grown on different silicon substrates under different growth conditions. Based on the findings, we propose a model for the source of electrical and electronic instability of the p-n junction in SiC/Si. Also, based on our understanding of SiC/Si, this work demonstrates a method for solving the problem of in-plane shorting or leakage for isolated SiC mesas or interdigitated structures on silicon.

II. EXPERIMENT

In this work we use unintentionally doped (thus n-type), 500 nm thick, NOVASiC 3C-SiC(100) films epitaxially grown on 527 μm low-doped p-type Si(100) having resistivity ranging from 1 to 10 Ωcm as well as high-resistivity (typically n-type, > 10 kΩcm) Si(100) substrates.[8] A second partner, IMEM-CNR, supplied 3C-SiC(100) films grown on 279(25) μm p-type Si(100) with resistivity ranging from 1 to 5 mΩcm.[9] Additionally, we have also tested 5 μm thick SiC films from IMEM-CNR prepared on 0° and 6° off-cut towards (110) Si(100) substrates.[10] Note that the 3C-SiC(100) films from both NOVASiC and IMEM-CNR are grown at 1300-1400 °C. Table I summarizes the samples studied in this work.

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For electrical characterization, we diced the SiC/Si wafers into 1.1x1.1 cm^2 coupons, and sputtered 150 nm thick nickel contacts (not annealed) onto the four corners using a custom-made shadow mask (Fig. 1(a)). We estimated the electrical properties such as the carrier concentration, carrier mobility, and sheet resistance at room temperature by performing van der Pauw Hall measurements on the SiC/Si samples as well as on representative bare Si substrates using an Ecopia HMS 5300 Hall Effect Measurement System. Scanning Electron Microscopy (SEM) using Zeiss supra 55VP SEM system operating at 10 kV characterized the surface morphology of the epilayers. Moreover, we performed simulations to model the leakage phenomenon and its influence on the electrical conduction using the Synopsys Sentaurus Device^{TM} simulator for the 3C-SiC on low-doped silicon.

Van der Pauw structures of SiC on high-resistivity Si were exposed to Inductively Coupled Plasma (ICP) etching using SF_6 gas and oxygen to remove the SiC layer using the Ni contacts as a hard mask followed by an Energy Dispersive X-Ray Analysis, and the Hall measurements were repeated at room temperature. Furthermore, SiC on high-resistivity Si samples were patterned into transfer length measurement (TLM) structures consisting of 300 nm thick, 500 μm wide aluminium contacts deposited using e-beam evaporation (not annealed) followed by acid etching of aluminium and reactive-ion etching of SiC. Current-voltage at room temperature using HP4145B semiconductor parameter analyser measured the leakage resistances. Afterwards, the silicon in between the SiC pillars for both the van der Pauw and TLM structures of SiC on high-resistivity Si were subsequently etched using ICP, and all measurements were repeated.

TABLE I. Summary of the samples used.

Samples	Supplier	Si resistivity (Ωcm)	Si thickness (μm)	SiC thickness (μm)
SiC/p-Si	NOVASiC	1-10	527 (on-axis)	0.5
SiC/high-resistivity Si	NOVASiC	>10k	235 (on-axis)	0.5
SiC/p-Si	IMEM-CNR	1-5m	279(25) (on-axis)	0.5
SiC/p-Si	IMEM-CNR	1-5m	279(25) (on-axis)	5.0
SiC/p-Si	IMEM-CNR	1-5m	279(25) (6° off-axis (110))	5.0

III. RESULTS AND DISCUSSION

A. 3C-SiC on low-doped silicon

1. Results

TABLE II. Hall measured transport characteristics at room temperature. Results are the averaged values extracted from three samples for each type.

	***Bare p*-Si**	**3C-SiC/*p*-Si**
Carrier type	Holes	Holes
Sheet carrier concentration (cm^{-2})	1.0(2)x10^{14}	1.0(2)x10^{14}
Mobility ($cm^2V^{-1}s^{-1}$)	341(10)	357(10)
Sheet resistance (Ω/□)	173(10)	166(10)

Table II shows the room temperature Hall measurement results of the low-doped p-Si substrate and 3C-SiC on p-Si. The low-doped p-Si substrate has p-type conduction with sheet carrier concentration, mobility and sheet resistance of 1.0(2) x 10^{14} cm^{-2}, 341(10) $cm^2V^{-1}s^{-1}$, and 173(10) Ω/□, respectively. 3C-SiC grown on the low-doped p-Si also indicates p-type conduction with sheet carrier concentration of 1.0(2) x 10^{14} cm^{-2}, mobility of 357(10) $cm^2V^{-1}s^{-1}$, and sheet resistance of 166(10) Ω/□, comparable to the bare low doped p-Si substrate. This implies that the SiC films grown on low-doped Si substrates are typically shorted and the charge carriers in the thick silicon substrate with relatively high mobility dominate the electrical conduction, as shown in Fig. 1(b). The electrical shorting persists even if we etch deep into the substrate, as long as the silicon charge carriers exists.[5] Note that, we have systematically confirmed that the contacts are not shorting the substrate through the edges.[4, 5]

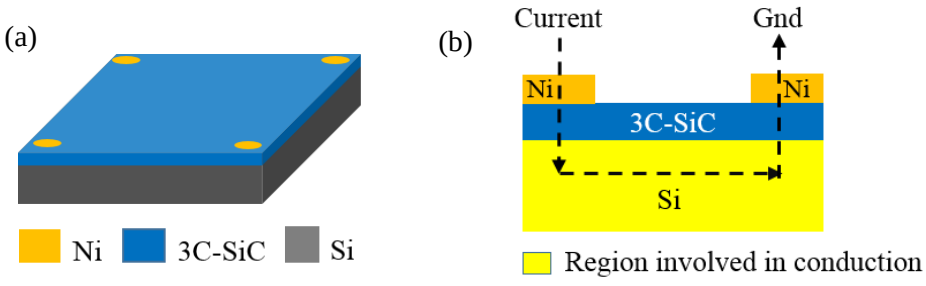

FIG. 1. (a) Layout of the van der Pauw structure on 3C-SiC/Si, (b) schematic of electrical conduction path in the SiC grown at 1300-1400 °C on low-doped p-Si substrate. The whole silicon substrate is involved in the conduction through the injection of holes into the SiC layer.

The electrical activity of the extended defects such as stacking faults (SF) and antiphase boundaries (APB) in SiC layers has been proposed in literature to explain the leakage in 3C-SiC devices.[2, 3, 11] In order to explore and potentially validate this hypothesis, we tested thicker films where the density of these defects are several orders of magnitude less than the thin films as reported by Song et al.[2].

Table III shows the room temperature Hall characteristics of IMEM-CNR 500 nm-thin SiC films on p-type Si (0°), 5 μm-thick SiC films on both on-axis (0°) and 6° off-axis p-Si as well as the bare on-axis and off-axis p-Si substrates. We find that, the IMEM-CNR 500 nm 3C-SiC films grown on on-axis p-Si are also shorted to the substrate similar to the NOVASiC 3C-SiC films. Moreover, Table III also clearly shows that the shorting is apparent even for the 5 μm thick SiC films grown on-axis p-Si as the transport characteristics match the underlying substrate. In addition, the transport characteristics of the 5 μm thick 3C-SiC on 6° off-axis p-Si, also exhibits electrical shorting with the substrate. If the extended defects in SiC layers were the main reason for the film-substrate shorting, the leakage would be reduced or absent in the thicker films.[2]

TABLE III. Hall measured transport characteristics at room temperature for IMEM-CNR thin 500 nm and thick 5 μm SiC films grown on the on-axis p-Si and 6° off-axis p-Si substrates. Results are the averaged values extracted from three samples for each type.

	SiC on on-axis p-Si			SiC on 6°off-axis p-Si	
	p-Si	500 nm SiC	5 μm SiC	p-Si	5 μm SiC
Carrier type	Holes	Holes	Holes	Holes	Holes
Sheet carrier concentration (cm^{-2})	$6.0(2)x10^{17}$	$8.0(2)x10^{17}$	$5.0(2)x10^{17}$	$6.0(2)x10^{17}$	$5.0(2)x10^{17}$
Mobility ($cm^2V^{-1}s^{-1}$)	70(10)	50(10)	65(10)	50(10)	50(10)
Sheet resistance (Ω/□)	0.17(1)	0.17(1)	0.17(1)	0.18(1)	0.18(1)

We performed SEM to determine the extent of extended defects in our samples. Fig. 2 shows an example SEM image of 500 nm thin SiC layers grown on on-axis p-Si and 5 μm thick SiC grow on 6° off-axis p-Si substrates. Fig. 2(a) shows that for thin epilayers, the stacking faults and antiphase boundaries are visible whereas, for the thick epilayers these defects are not visible, shown in Fig. 2(b). Thus, although the SEM evidence demonstrates fewer defects at the surface of the thick SiC layers, electrically there is no improvement in the shorting/leakage issue. This indicates that the extended defects in the SiC layers such as APB or SF probably do not substantially contribute to the leakage phenomenon.

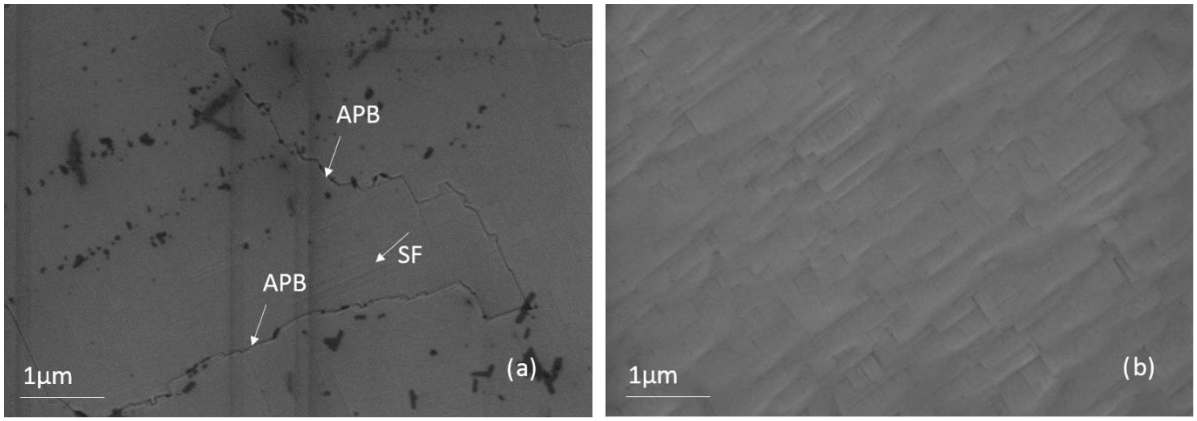

FIG. 2. Plane view SEM images for IMEM-CNR 3C-SiC (a) 500 nm-thin SiC(100) film on on-axis p-Si; where antiphase boundaries (denoted APB) and stacking faults (denoted SF) are visible; (b) 5 µm-thick SiC(100) films on 6° off-axis p-Si substrates; APBs and SFs are not visible

2. Discussion and model

In addition to the data presented here, indicating the electrical shorting of SiC/Si films grown at a temperature of 1350°C, we had also previously reported the occurrence of a similar phenomenon in SiC films grown at a lower temperature (~1000°C), after the samples were vacuum annealed at 1100°C.[4, 5] We noted that the electrical shorting was invariably accompanied by the relaxation of a considerable amount of compressive stress present at the SiC/Si heterointerface;[4] which was a consequence of the combination of high temperature and high stress at the SiC/Si interface enabling interatomic diffusions between SiC and Si.[12] Due to the stress relaxation at the SiC/Si interface, we observed plastic deformation of the silicon substrate leading to a permanent change in the wafer curvature, becoming more convex (after annealing), as illustrated in Fig. 3.

Zielinski *et al*. also observed the occurrence of plastic deformation of the silicon substrate upon film growth when growth temperatures of 1300-1400°C were used.[13, 14] In this case, a permanent change of substrate curvature towards a less concave curvature was found, which was used to minimize the total bowing of the substrate upon growth.[13, 14] This was an important technological advance, since the significant tensile stress due to the lattice and thermal mismatch of the SiC on silicon system, especially for micron thick SiC films, would lead to an excessively concave wafer curvature.[12] Such curvature would be particularly challenging for further wafer processing as well as device applications.

In addition, Anzalone *et al*., Camarda *et al*. and Watts *et al*., have reported for SiC grown at 1300°-1400°C an intense compressive stress generated within the substrate capable

of bowing the whole SiC/Si heterosystem downwards.[15-17] These authors also proposed the stress originated from the early stage of growth (i.e. at the carbonization step), where unspecified "defects" are generated in the silicon substrate.[15, 16]

Noting that the SiC/Si samples studied in this work were all grown at high temperatures, similar to that of Zielinski *et al.*, and that all of the samples have shown electrical shorting with the silicon substrate, it seems logical to expect that this phenomenon must be related to a permanent change (plastic deformation) of the substrate (convex) curvature. This permanent curvature change must occur whenever the top portion of the silicon substrate is driven into compression (see schematic in Fig.3). We propose that the compression in the top portion of the substrate is due to carbon diffusion into the silicon substrate matrix, as the carbon would expand the Si substrate lattice.

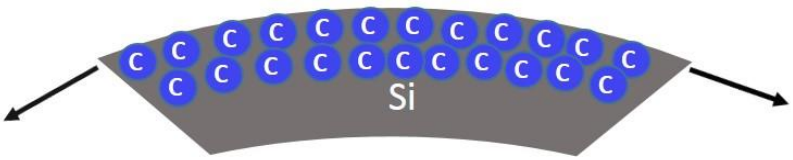

FIG. 3. Schematic of Si substrate bending into more convex due to the compressive stress exerted by the carbon interstitials within the top portion of silicon.

The guiding reasons for our hypothesis are that, due to the high stresses and high temperatures involved in SiC on Si heteroepitaxy, combined with a very high carbon-silicon miscibility (both elements are column IV), a considerable driving force for C and Si inter-diffusion is anticipated in the interfacial region. Indeed, an out-diffusion of silicon forming typical interfacial voids, has been reported extensively in the literature.[7, 13] However, the possibility for microscopic atomic carbon diffusion into the silicon matrix has been largely overlooked, as opposed to the macroscopically evident silicon voids. In fact, we note that in all samples used for this work the silicon voids were intentionally suppressed by the vendors through engineering of the heteroepitaxial process.

Moreover, we expect carbon interstitials to affect SiC/Si electrical junction properties. Note that when the carbon concentration in silicon exceeds the solubility of substitutional carbon (~10^{17} cm^{-3} at 1300°C),[18] interstitial carbon point defects are formed.[19] A vast extent of atomic diffusion of carbon into the silicon substrate, would therefore lead to a significant amount of interstitial carbon, which would in turn drive the top portion of the substrate into compression while also strongly affecting the SiC/Si electrical junction.

Interstitial carbon, complexes between the interstitial and substitutional carbons or carbon precipitates may be electrically active and negatively affect the electrical characteristics of p-n junctions[19, 20] resulting in substantial leakage, or even plain electrical shorting, since such defects act as an additional conduction path for charge carriers. The carbon interstitials can behave as deep acceptors in silicon with an activation energy of 0.35 eV from the valence band (hole traps)[20], and assist compensation of unintentional donors in the SiC film as well as hole injection from the Si substrate across the Si/SiC interface further reducing the effectiveness of p-n junction.

Hence, the generation of a considerable amount of interstitial carbon defects in the top portion of silicon upon high temperature epitaxy, would explain both the mechanical and the electrical behaviour observed in the SiC/Si system.

We simulated the effect of interstitial carbon on the junction between SiC and the low-doped p-Si substrate using Technology Computer-Aided Design (TCAD) simulations, performed at 1V bias, using the parameters summarized in Table IV.

The initial n-type doping concentration for the SiC films was set to $1x10^{19}$ cm^{-3} according to the value in Pradeepkumar *et al.*, measured prior to the degradation of the p-n junction (see Table IV and Fig. 4(a)).[4] Hole -type doping for the silicon was set at $1.3x10^{15}$ cm^{-3} as per Hall measurements of the bare p-Si in Table II (see Fig. 4(b)). The electronic defects in the silicon were subsequently introduced in the calculation, assuming an ionization energy of 0.35 eV from the valence band (hole traps, deep acceptors) as reported for interstitial carbon in silicon by Simoen *et al.*[20] The simulations accounting for the interstitial defects show that an acceptor density of about 10^{20} cm^{-3} in the silicon is sufficient in order to invert the conduction of the SiC film from n-type to p-type (Fig. 4(c) and 4(d)).

Table IV. Simulation parameters.

	Thickness (µm)	**Doping (cm^{-3})**	**Hole trap density (cm^{-3})**	**Ionization energy (eV)**
3C-SiC	0.5	$1x10^{19}$ (n)	-	-
Si	527	$1.3x10^{15}$(p)	$1x10^{20}$	0.35

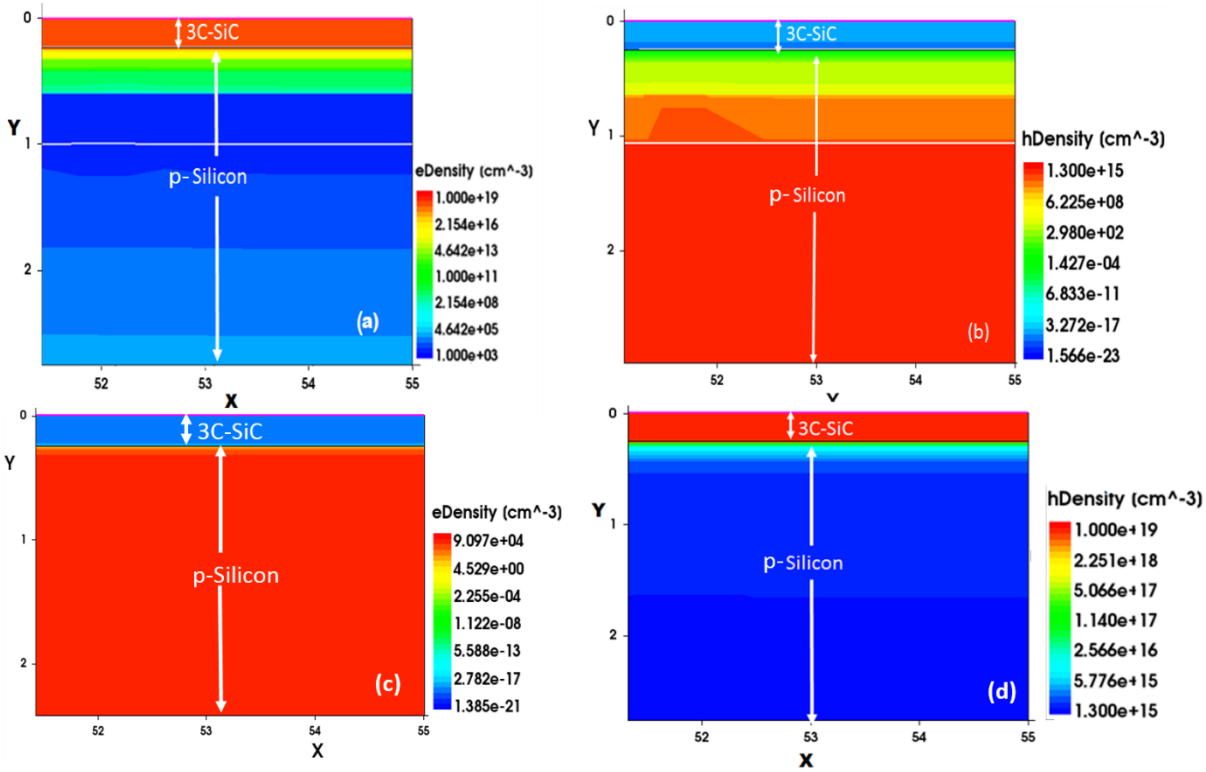

FIG. 4. TCAD simulation results of the 3C-SiC on low doped p-Si substrate (a) electron density and (b) hole density, in the SiC/Si system before junction degradation (no defects); (c) electron density and (d) hole density, in the SiC/Si system after incorporating interstitial carbon degradation within silicon.

Therefore, the degradation of the p-n junction at the interface of the n-SiC film on p-silicon (upon growth or high temperature annealing) can be fully explained by the presence of electrically active interstitial carbon acceptor traps in excess of 10^{20} cm^{-3} within the top portion of the substrate.

For completeness, we note that an additional potential reason for the degradation of the SiC/Si junction could be the reduced band gap arising from the residual tensile strain in the SiC epilayers.[6] That is, the band gap reduction results in a smaller valence band barrier and leads to increased hole current injection from the Si to the SiC.[6] To test the hypothesis of tensile strain-induced SiC band gap changes on the junction we simulated the SiC/Si system with the strained band gap and electron affinity values mentioned by Rahimi *et al*.[6] and found that even a large concentration of those acceptor traps (up to ~10^{20} cm^{-3}) in the film does not appreciably contribute to the degradation of the heterojunction between the SiC film and the substrate.

B. 3C-SiC on high-resistivity silicon

1. Results

In an attempt to electrically insulate the silicon carbide film from the silicon substrate, we have used a high-resistivity silicon as the substrate, as opposed to p-type doped silicon.

Table V shows the room temperature van der Pauw Hall measurement results of 3C-SiC grown on high-resistivity Si as well as the representative bare Si substrate. High-resistivity silicon shows n-type conduction, with a sheet carrier concentration of $1.0(2)\text{x}10^{10}$ cm^{-2}, mobility of 1220(10) $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, and sheet resistance of 500(3) kΩ/□.

After the SiC film growth on the high-resistivity Si, the transport characterisation showed a carrier concentration one order of magnitude higher, and the sheet resistance one order of magnitude smaller compared to the bare substrate. However, even after completely removing the SiC layer using ICP etching, the Hall measured characteristics remained largely unaffected and consistent with the values before the removal of the SiC layer. Note that the complete removal of SiC layer has been confirmed using an Energy Dispersive X-Ray Analysis after etching.

The similar transport characteristics before and after the removal of SiC layer clearly indicate that the SiC is not responsible for the measured electrical conduction. To clarify this and discern the origin of the conduction in SiC/high-resistivity Si, we measured the leakage resistances between SiC mesas on the high-resistivity Si using the TLM method as shown in Fig. 5.

Table V. Hall measured transport characteristics at room temperature. Results are the averaged values extracted from three samples for each type.

	High-resistivity Si	**SiC/high-resistivity Si**	**Removed SiC/high-resistivity Si**
Carrier type	Electrons	Electrons	Electrons
Carrier concentration (cm^{-2})	$1.0(2)\text{x}10^{10}$	$3.0(2)\text{x}10^{11}$	$4.0(2)\text{x}10^{11}$
Mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	1220(10)	1677(10)	1650(10)
Sheet resistance (kΩ/□)	500(3)	12(3)	12(3)

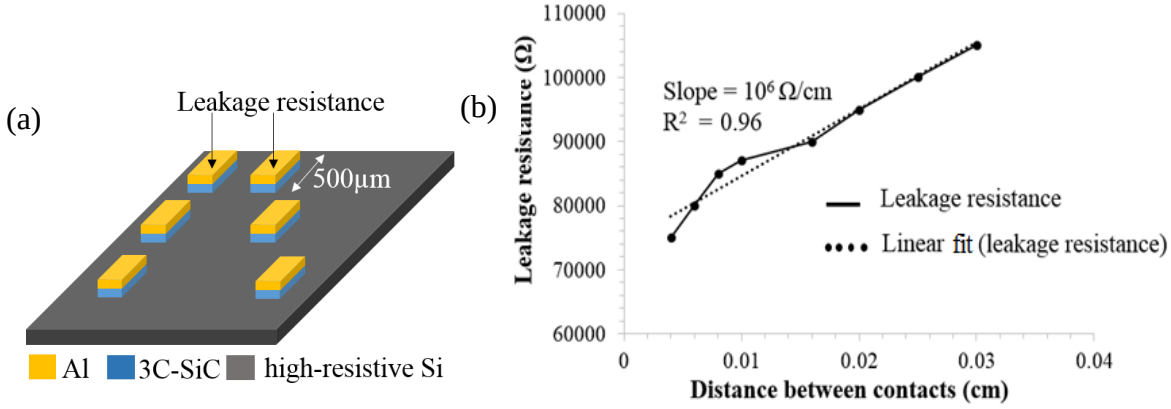

FIG. 5. a) TLM structures on the 3C-SiC/high-resistivity Si, b) Fitted TLM leakage resistances versus contact spacing for SiC on high-resistivity Si

Fig. 5b shows the fitted leakage resistances obtained using TLM structures on the SiC/high-resistivity Si as a function of different contact spacing with a slope of 10^6 Ωcm^{-1}. The sheet resistance obtained experimentally from slope and width of the contact is ~50 kΩ/□, about the same order of magnitude of the sheet resistance obtained from the Hall measurements in TABLE II after growth and/or removal of the SiC. Based on the specification of the high-resistivity substrate, we would expect a 500 kΩ/□ of sheet resistance for the TLM measurement. In conclusion, both van der Pauw and TLM measurements indicate that after the growth of SiC on the high-resistivity silicon, a leakage path is created in a region below the interface, which is not removed by the etching of the SiC.

We suggest that the presence of additional carriers in the order of ~10^{11} cm^{-2} within the high-resistivity silicon forming a leakage path below the interface can be attributed once again to the carbon out-diffusion into silicon forming interstitial carbon. Sze indicates that the interstitial carbon in an n-type silicon acts as a donor with a defect level of 0.25 eV from the conduction band, creating effectively an n-type doping.[21] The presence of interstitial carbon point defects within the silicon can thus form a leakage path within the top portion of the high-resistivity substrate. The schematic representation of the electrical conduction in 3C-SiC on high-resistivity silicon is given in Fig. 6.

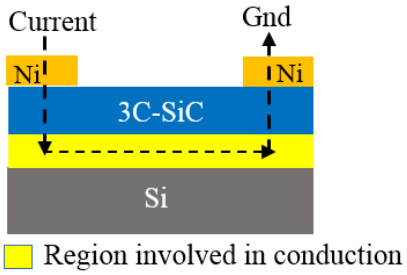

FIG. 6. Schematic of conduction path in 3C-SiC/high-resistivity Si grown at 1300 - 1400 °C -the conduction occurs within a region of a few micrometres thick below the interface.

C. Practical solution for the 3C-SiC/Si in-plane leakage

Based upon the conduction path sketched in Figure 6, we would expect that removing the conductive portion of the silicon could resolve the leakage problem in the SiC/high-resistivity Si system.

Table VI (a) shows that after etching away the conductive region in the silicon below the SiC/Si interface we obtain a van der Pauw sheet resistance of 492(2) kΩ/□ indicating an acceptable electrical isolation between the SiC mesas. The leakage resistances for the SiC/high-resistivity Si using TLM structures after the removal of the conductive region is ~10 MΩ, indicating that leakage is eliminated within the SiC/Si system, see Table VI (b).

Table VI. Electrical characteristics at room temperature for SiC/high-resistivity Si before and after ~20 µm deep etching of silicon between SiC pillars a) van der Pauw Hall measurement results b) TLM leakage resistance results. Results after etching are the averaged values of two samples each.

(a)	**SiC/high-resistivity Si (before etching)**	**SiC/high-resistivity Si (after 20 µm etch)**
Carrier type	Electrons	Electrons
Sheet carrier concentration (cm^{-2})	$3.0(2)x10^{11}$	$5.0(2)x10^{11}$
Mobility ($cm^2V^{-1}s^{-1}$)	1677(10)	34(10)
Sheet resistance (kΩ/□)	12(3)	492(2)

(b)

Contact spacing (µm)	TLM leakage resistance before etch (kΩ)	after 20 µm etch (MΩ)
40	75	8.5
60	80	8.5
80	85	9.5
100	87	10
160	90	-
200	95	10

From both the van der Pauw and TLM results we find that in order to completely isolate the SiC mesas, we need to etch at least 20 µm deep into the high-resistivity silicon between the SiC pillars, see Figures 7(a) and 7(b).

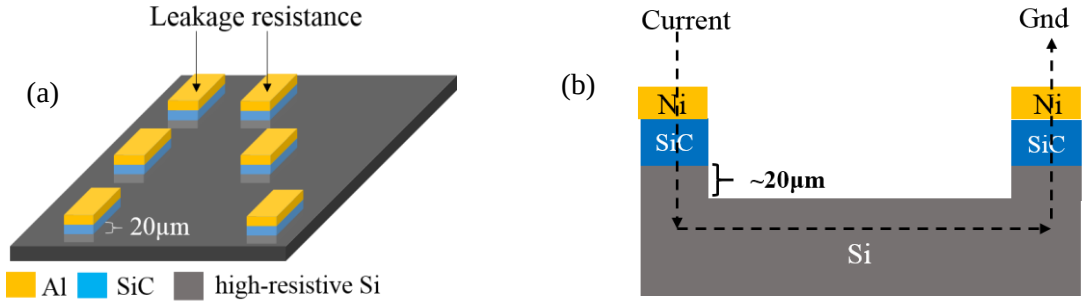

Fig. 7. SiC/high-resistivity Si after ~20 µm deep etching of Si (a) TLM structure, (b) electrical conduction

IV. CONCLUSION

The scope for application of heteroepitaxial 3C-SiC films grown on Si is typically limited by the electrical instability of the heterointerface. Although this limitation was already known in the scientific community, the reason for this instability had not been addressed. Here we show that, upon epitaxial growth at high temperature, this electrical instability is due to the diffusion of carbon atoms into the underlying silicon matrix forming electrically active interstitial carbon defects, which also results in strong compression for the top portion of the substrate.

When considering epitaxial SiC on a p-type silicon substrate, we have shown that an interstitial carbon concentration in silicon in excess of 10^{20} cm^{-3} can invert the conduction in the SiC from n-type to p-type due to the generated acceptor traps (interstitial carbon in silicon forming a mid- bandgap level at 0.35 eV), destroying the electrical junction. When a highly resistive silicon substrate is used instead, we have shown that atomic carbon diffusion within

the top portion of silicon generates a leakage path below the SiC/Si heterointerface. We can attribute this phenomenon again to the interstitial diffusion of carbon, generating additional n-type carriers in silicon due to the second type of electronic defect associated with interstitial carbon, which is a donor level 0.2 eV from the conduction band. Nevertheless, we have also demonstrated that we can achieve electrical isolation of SiC mesas on high-resistivity silicon substrates by etching away at least 20 μm into the silicon between the SiC structures.

We also conclude that the electrical instability of the SiC on silicon system is a universal underlying problem associated with direct epitaxial synthesis, no matter the epitaxial approach used, although certainly conditions such as temperature are expected to influence the extent of this phenomenon. Therefore, this work clarifies a long-standing issue in the SiC community.

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