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Impact of TFET Unidirectionality and Ambipolarity on the Performance of 6T SRAM Cells

SEBASTIANO STRANGIO[1,2], PIERPAOLO PALESTRI[1] (Senior Member, IEEE), DAVID ESSENI[1] (Fellow, IEEE), LUCA SELMI[1] (Fellow, IEEE), FELICE CRUPI[2] (Senior Member, IEEE), SIMON RICHTER[3], QING-TAI ZHAO[3] (Member, IEEE), AND SIEGFRIED MANTL[3] (Member, IEEE)

[1]Dipartimento di Ingegneria Elettrica, Gestionale e Meccanica, Università degli Studi di Udine, Udine 33100, Italy
[2]Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica, Università della Calabria, Arcavacata di Rende 87036, Italy
[3]Peter Grünberg Institute-9, JARA-FIT, Forschungszentrum Jülich, Jülich 52425, Germany

CORRESPONDING AUTHOR: S. STRANGIO (seb88str@gmail.com)

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ABSTRACT We use mixed device-circuit simulations to predict the performance of 6T static RAM (SRAM) cells implemented with tunnel-FETs (TFETs). Idealized template devices are used to assess the impact of device unidirectionality, which is inherent to TFETs and identify the most promising configuration for the access transistors. The same template devices are used to investigate the V_{DD} range, where TFETs may be advantageous compared to conventional CMOS. The impact of device ambipolarity on SRAM operation is also analyzed. Realistic device templates extracted from experimental data of fabricated state-of-the-art silicon pTFET are then used to estimate the performance gap between the simulation of idealized TFETs and the best experimental implementations.

INDEX TERMS SRAM, TFET, technology computer aided design (TCAD), VLSI.

I. INTRODUCTION

Tunnel-FET is one of the most promising candidates to complement or replace CMOS in ultra-low-power (ULP) applications [1]-[5], featuring a sub-threshold swing (SS) below the 60 mV/decade limit of metal-oxide-semiconductor field-effect transistor (MOSFET) at room temperature. Steep I_D-V_{GS} characteristics with a minimum SS of 30 mV/decade [6] or 21 mV/decade [7] have been demonstrated experimentally. However, since such low SS is achieved only over a small voltage range and for a drain current (I_D) in the order of pA/μm, there is a significant lag between modeling projections and experiments [1], [2].

Nowadays, the Static RAM (SRAM) cell is one of the most relevant digital building blocks largely deployed as on-board cache in processors (occupying up to the 70% of a processor area [8]). To estimate the impact of using TFETs on the performance of SRAM is thus an important step to assess their deployment in advanced digital circuits [9]-[17].

Since the availability of compact models for TFETs is limited, mixed device/circuit simulation decks [18], [19] are a powerful alternative to analyze simple circuits using a microscopic description of the devices.

We report here on TCAD mixed device-circuit simulations of TFET based SRAM cells, implemented with different TFETs structures with the aim of assessing the impact of some specific features of TFETs on the static and dynamic SRAM performance.

One of the main intrinsic limitations of TFETs stems from the asymmetry of drain (D) and source (S) regions that makes I_D inherently unidirectional. This is critical in SRAM cells since the access transistors should be bi-directional [8]-[17]. To this regard, we address in Section II the issues related to the current unidirectionality considering idealized template devices that are far from what can be fabricated now since they feature dimensions comparable to ultra-scaled MOSFETs and the Band-to-Band Tunneling (BtBT) rate is

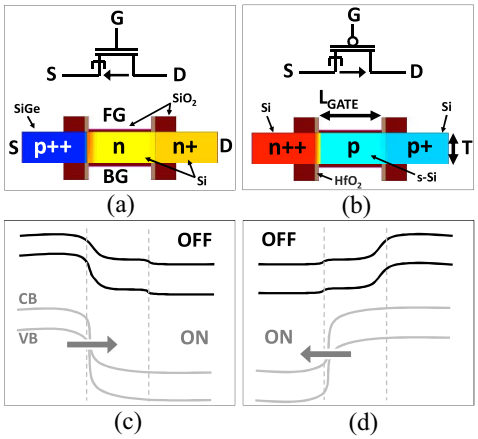

FIGURE 1. Symbols and structures of (a) SiGe/Si/Si NTFET and (b) Si/strained-Si/Si PTFET. L_{GATE} = 30 nm, T = 10 nm, EOT = 1.1 nm. Details of the device design are provided in [4]. Sketches of band diagrams along the device in both OFF and ON states for (c) NTFET and (d) PTFET.

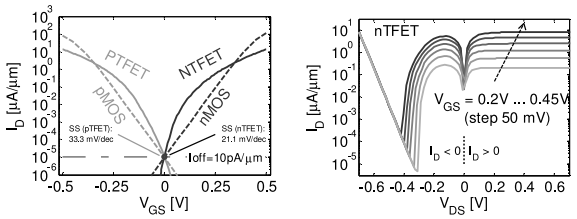

FIGURE 2. Left: simulated I_D-V_{GS} characteristics at $|V_{DS}|$= 0.5 V for the devices in Fig. 1. Right: I_D-V_{DS} characteristics for the NTFET in Fig. 1(a).

increased to provide drain currents comparable to CMOS. We use such idealized TFETs because they give us several opportunities: 1) exploring hybrid circuit topologies based on both TFETs (in the inverters) and conventional MOSFETs (as access transistor); 2) making a meaningful comparison between TFET and CMOS cells with comparable devices at different V_{DD}; 3) having an upper bound for the attainable performance, that can be used to benchmark more realistic simulations performed after calibration against experimental results.

In Section III we consider structures and model parameters calibrated on fabricated devices. We resort to a simulation deck [17] calibrated on ambipolar devices [6] to analyze the impact of TFET ambipolarity on SRAM cells. Then, we perform a new calibration on state-of-the-art experimental strained-Si pTFET nanowire to evaluate the performance mismatch between idealized and experimental devices.

II. EFFECT OF THE UNIDIRECTIONALITY CONSIDERING IDEALIZED TEMPLATE DEVICES

In this section we use idealized devices to analyze the impact of TFET unidirectionality on the performance of the cell and identify the best cell architecture. Realistic devices will be considered in the next section.

A. IDEALIZED TEMPLATE DESCRIPTION

The n-type SiGe/Si (Fig. 1(a)) and p-type strained-Si (Fig. 1(b)) TFETs considered in the mixed device/circuit simulations of this section have been designed in [4]. Fig. 1 shows also the corresponding band diagrams, highlighting the direction of electrons tunneling from the valence band (VB) of the source to the conduction band (CB) of channel region in the on-state NTFET (Fig. 1(c)), and from the channel region VB to the source CB in the on-state PTFET (Fig. 1(d)).

Tunneling conduction mechanisms are taken into account in the TCAD simulator by means of a (static) *non-local tunneling model*, activating the BtBT option [18]. The adjustable calibration parameters are the tunneling masses m_c and m_v and the scaling factors g_c and g_v for the generation/recombination terms that are added to the carrier continuity equations [18]. Even if a more physically accurate *dynamic non-local BtBT model* is available, we chose the static one since it is computationally more robust in the mixed device/circuit scheme.

The same base structure in Fig. 1, which is here interpreted as a 2D cut of a 3D nanowire (NW), has been used to implement also n- and p-type conventional MOSFETs for comparison purpose. The use of idealized models and templates for both TFETs and MOSFETs assures a fair comparison between these two competing technologies. In fact, due to poor maturity of fabricated TFETs, it would be unfair to benchmark experimental TFETs against experimental CMOS.

The I_D-V_{GS} and I_D-V_{DS} characteristics of the considered transistors are reported in Fig. 2. The gate work-functions have been adjusted to match the off-current LSTP (I_{OFF} = 10 pA/μm) [3], [4]. For such condition, the low SS value of the TFETs is confined at low current levels, and this would make them competitive over CMOS only for very low V_{DD} applications (below ∼300 mV), since for larger supply voltages their current drivability would become much lower than the one of CMOS.

Even if this choice meets the ITRS specifications, it makes it difficult to highlight the TFET potentialities because the steepest part of the simulated I_D-V_{GS} corresponds to negative V_{GS} and the crossover voltage at which the TFET on-current is surpassed by the CMOS one is very low. In fact, while the CMOS I_D-V_{GS} features an almost constant sub-threshold slope, the TFET I_D-V_{GS} characteristics takes full advantage of its steepest part when the target I_{OFF} is decreased. In this respect, Fig. 3 illustrates that the lower is the off-current, the larger is the voltage range where TFETs outperform CMOS. In the following of our analysis we will use I_{OFF} = 10 pA/μm (except for a more in detail discussion presented in Section II-G), because lower off-current would be difficult to achieve in real devices due to the presence of additional leakage paths such as gate leakage and trap-assisted-tunneling.

The I_D-V_{DS} characteristics in the right plot of Fig. 2 point out that the TFET current is essentially unidirectional.

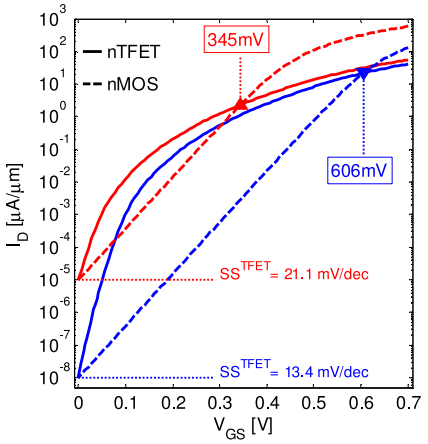

FIGURE 3. I_D–V_{GS} characteristics of the n-type TFET and MOSFET aligned at I_{OFF} = 10 pA/μm and at I_{OFF} = 10 fA/μm. V_{DS} = 0.5 V.

When a n-type TFET is biased with a negative V_{DS} there is only a small linear region where the current increases, but then it decreases quickly to zero. Furthermore, as the V_{DS} approaches −0.6 V, the current increases again due to forward biasing of the parasitic p-n diode. Since in such condition the drain current is not controlled by the V_{GS}, TFETs should not be used in circuit topologies enforcing these biasing conditions.

B. SRAM CELL DESCRIPTION

In the symmetric 6T SRAM cell sketched in Fig. 4 (6T), n-type and p-type TFETs are employed for the two cross-coupled inverters. M1 and M3 are the pull-down transistors (PD) whereas M2 and M4 are the pull-up transistors (PU).

Due to unidirectional current of TFETs, three alternatives are considered for the access transistors (AT) M5 and M6: the first two employing n-type TFETs, the last one employing n-type MOSFETs. The TFET ATs can be either (a) inward facing (I-AT), or (b) outward facing (O-AT) [9]-[17]. Since the two configurations with TFET-ATs suffer from the limitation of asymmetric current flow, we also investigate a hybrid TFET/CMOS SRAM cell using conventional MOSFETs as ATs (c) [16].

The impact of I_D unidirectionality on the I-AT and O-AT configurations has been already addressed by other groups [9]-[15], with a consensus on the fact that a full-TFET symmetric 6T SRAM is not properly working. Therefore, modified SRAM architectures have been proposed to overcome the unidirectionality issue: asymmetric 6T cell with one I-AT and one O-AT and write-assist technique (WA) [9], 7T cell with O-ATs and one additional transistor for the read [10], 6T cell with p-type I-AT and read-assist (RA) [11], 8T and 10T Schmitt-Trigger cells [12], [13], a 7T driver-less (DL) cell [14] and a 8T hybrid TFET/CMOS cell [15].

In [16] we have shown that a proper cell sizing and the BL pre-charge (Φ^{BL}) to $V_{DD}/2$ allows one to make the O-AT

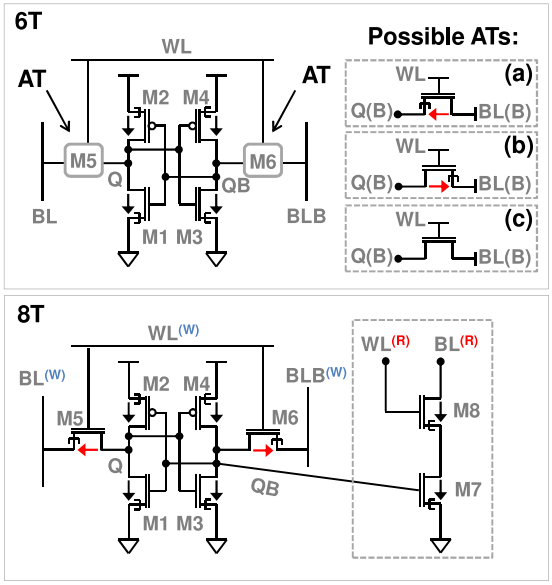

FIGURE 4. Top: symmetric 6T SRAM structures with (a) inward facing TFET ATs, (b) outward facing TFET ATs, and (c) nMOS ATs. Bottom: 8T TFET SRAM cell with outward-facing write-ATs and two additional nTFETs employed for the read.

configuration working. We extend here this analysis with the aim to compare such trade-off on the O-AT 6T cell with the 8T cell sketched in the lower plot of Fig. 4 (8T). The 8T configuration is basically a 6T topology with O-ATs employed only for the write, and with two more transistors to perform the read. As a result, the write and read operations are effectively decoupled leading to a robust solution to the unidirectional I_D issue. The 8T cell has been employed in other works as a reference topology to benchmark more innovative schemes [14], [15].

C. DEFINITION OF THE STATIC AND DYNAMIC FIGURES-OF-MERIT

The aim of this sub-section is to briefly review the write and read operations of a 6T SRAM cell to facilitate the forthcoming discussions.

The memorization element of a SRAM cell is represented by the two cross-coupled inverters storing the data as high and low voltage levels in the Q and QB nodes (see Fig. 4), while the two ATs allow to force or to access the stored data during the write and the read operations, respectively.

The symmetry of the 6T cells makes the write, read and hold operations symmetric with respect to the differential stored logic values: '0' (Q = 0 and QB = V_{DD}) and '1' (Q = V_{DD} and QB = 0). This is not the case of any fabricated SRAM cell, where variability leads to differences in the mirrored parts of the cell. However, since the implications of process variability are beyond the scope of this work, we consider here nominal devices and treat the cells as perfectly symmetric.

The static performances are evaluated by means of the half circuit voltage transfer-characteristics (VTC) method [8],

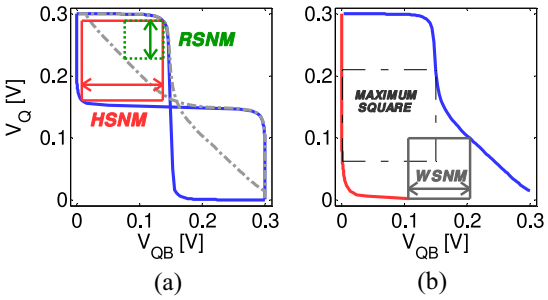

FIGURE 5. (a) Definition of HSNM and RSNM. The VTCs of the blue butterfly are obtained for WL = 0 and equals the inverter VTCs. The dash-dotted gray VTCs are taken by biasing with V_{DD} the WL and BL(B). (b) Definition of WSNM. The blue VTC is traced for WL = V_{DD} and BL = V_{DD}, the red one is traced for WL = V_{DD} and BLB = 0. Note that, the squares between the forced operating point ($V_{QB} = 0$, $V_Q = V_{DD}$) and the closest maximum square (thin dashed line) are not taken into account in the computation of the minimum square representing the WSNM square (a "minimum" square cannot be defined in this range since it would degenerate in a dot coinciding with the operating point).

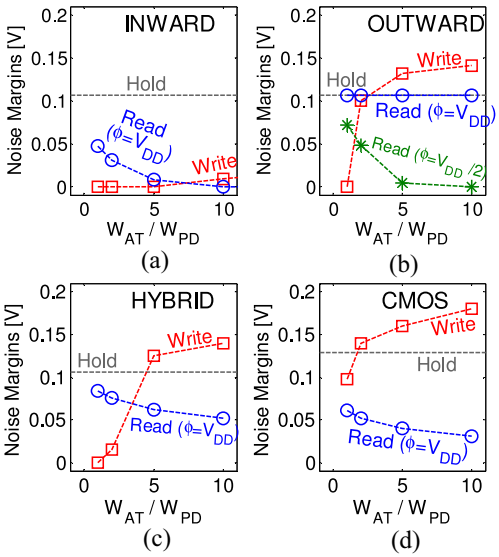

FIGURE 6. Hold, read, and write static noise margins (SNMs) of 6T SRAM cell with (a) inward-AT full-TFET, (b) outward-AT full-TFET, (c) hybrid nMOS/TFET, and (d) full CMOS cell. $V_{DD} = 0.3$ V. $W_{PU} = W_{PD}$.

which requires the $V_Q = f(V_{QB})$ static characteristic taken for various BL and WL voltage levels.

The Static Noise Margins in hold (HSNM) and read (RHSN) operations are calculated as in [8] (Fig 5(a)). To compute the write SNM (WSNM), the butterfly curves are obtained for two different conditions, that is for the two differential voltage levels of the BLs (0 and V_{DD}) when the WL is at V_{DD} (Fig. 5(b)). For bidirectional ATs, the deformation of these curves with respect to the inverter VTC is stronger for the inverter with the AT connected to the bit-line driven at low voltage level. In fact, even if both of them appear deformed due to on-state ATs, the drivability of the n-type AT is larger when BL is 0 V. It follows that the change of cell status is forced mainly by the side with the bit-line at low voltage level. The write butterfly graph of a well-sized cell features only one crossing point between the VTCs that coincides with the logic value to be written. The more deformed are the VTCs with respect to the butterfly of the inverter, the more robust is the write. Therefore, the WSNM is the size of the minimum square between the writing VTCs (Fig. 5(b)). Unidirectionality of the ATs severely limits their drivability when biased with a negative V_{DS} and this affects the time of the read and write operations. For this reason, beside the SNMs we compute also the write and read delays, defined respectively as the time needed by the storage node Q to flip from 0 V to 90% of V_{DD} and as the time at which the difference V_{BL}-V_{BLB} achieves the 10% of V_{DD}. These delays are computed by means of transient simulations performed on the full cells (including all the six transistors). Two capacitors of 20 fF[1] schematically describe the parasitic capacitance of the BLs.

D. RESULTS: WRITE OPERATION (6T CELLS)

Considering the WSNMs for the 6T cell in Fig. 6(a) and (b), the O-ATs appear to perform better than the I-ATs. In fact, the write is performed by forcing the BL pair to differential levels of '1' and '0' before raising the WL to '1'. It follows that only one of the two unidirectional ATs can propagate the data, that is only the logic '1' with the I-AT and only the logic '0' with O-AT. Furthermore, since only transfer of the '0' is really efficient with an n-type transistor, the cell with the O-AT has a better write-ability than the cell with the I-AT, where a successful write can be performed only by sizing the ATs more than ten times larger than the nTFETs of the inverters (Fig. 6(a)). The arguments discussed above are still valid for p-type ATs, just substituting the n-type O-AT with the p-type I-AT, since p-type transistors propagate the '1' better than the '0' [11].

Conversely, the write in the hybrid solution (Fig. 6(c)) is quite similar to the CMOS case (Fig. 6(d)), where both the ATs can propagate the differential data (although with different strength). Interestingly, although with the nMOS ATs it is possible to force the data from both sides, by comparing the WSNMs of Fig. 6(b) and (c), we observe that the O-ATs WSNMs are larger than in the hybrid solution. This is due to the better drivability of the nTFET with respect to the nMOS at $V_{DD} = 0.3$ V. In fact, the hybrid solution is strongly affected by V_{DD} scaling, due to the different shape of the I_D-V_{GS} curves of the nMOS-AT and of the nTFET PD (Fig. 2).

E. RESULTS: READ OPERATION (6T CELLS)

Given that O-ATs feature a better write than I-ATs, we discard the I-AT configuration since, as demonstrated by the Fig. 6(a), it cannot feature both WSNM and RSNM sufficiently larger than zero for a given cell sizing.

At the same time, the read operation with the O-ATs cannot be performed correctly if the BL pair is precharged to V_{DD} because the O-ATs has a negative V_{DS}. Consequently, even if the RSNM is essentially equal to the HSNM (Fig. 6(b)), the cell is isolated, since the O-ATs are off,

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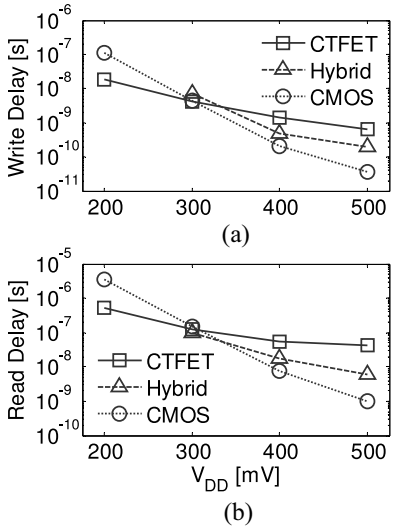

FIGURE 7. Comparison of write (a) and read (b) delays for various supply voltages for all CMOS 6T SRAM cell, all TFET 6T cell (with O-ATs and BLs pre-charge to half V_{DD} for reading) and 6T hybrid cell. In the hybrid configuration, the delays are not reported for V_{DD} = 0.2 V, since the write fails due to the poor drive current of nMOS ATs with respect to TFETs of the inverter.

resulting in a huge read delay of about 10 ms at V_{DD} = 0.3 V (not shown).

In [10] the read-ability with O-ATs is assessed assuming a Φ^{BL} = 0 V, coming to the conclusion that neither I-ATs nor O-ATs provide acceptable write and read SNMs for a given sizing. However, the O-ATs configuration features good SNMs and reasonable delays if the read is performed with $\Phi^{BL} = V_{DD}/2$. As shown in Fig. 6(b), a W_{AT}/W_{PD} ratio close to 2 results in acceptable R- and W-SNMs. Furthermore, even if the $C_{BL(B)}$ connected to the O-AT related to storage node with '0' remains stuck at $V_{DD}/2$ after the rising of WL voltage, the opposite O-AT pulls the corresponding $C_{BL(B)}$ from $V_{DD}/2$ toward V_{DD}, thus enabling a differential sense amplifier to detect the data stored into the cell.

Fig. 7 summarizes the dynamic performances of the 6T TFET SRAM cell with O-ATs, of the hybrid case and of the CMOS cell. The read with $\Phi^{BL} = V_{DD}/2$ is performed only for the O-ATs configuration, while for the other configurations $\Phi^{BL} = V_{DD}$ is used. In fact, in the full CMOS and hybrid configurations the read at half V_{DD} does not lead to an appreciable reduction of the read delay as in the case of O-ATs configuration. According to Fig. 7, the 6T SRAM with O-ATs becomes the best 6T choice when V_{DD} is scaled down below 300 mV, considering that in the hybrid case the nMOS AT should be sized ten times the TFET to guarantee the write operation. For this reason, the associated delays are not shown for V_{DD} = 0.2 V. However, for higher supply voltages the CMOS cell shows better performances.

F. READ AND WRITE IN THE 8T CELL

The 8T SRAM cell is a robust solution for both CMOS and TFET technologies since write and read operations are decoupled. In the TFET version (Fig. 4 (8T)) we employed

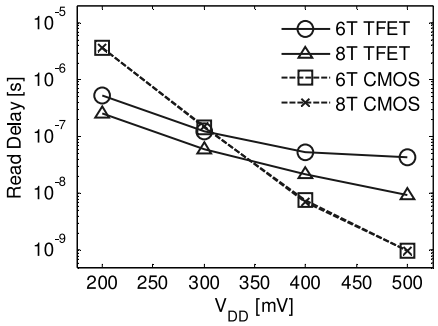

FIGURE 8. Comparison of read delays for various supply voltages of the 6T TFET cell (with O-ATs and BLs pre-charge to half V_{DD} for reading), the 8T TFET cell, and the 6T and 8T CMOS cells.

outward ATs for writing. The write operation is in fact very similar to that in the 6T cell (the impact of the capacitive load represented by the M7 read transistor is negligible), thus the WSNM of 8T TFET and 8T CMOS cells are practically the same as reported in Fig. 6(b) (6T O-AT TFET cell) and 6(d) (6T CMOS cell), respectively. On the other hand, the read is performed through the stack represented by the n-type transistors M7 and M8. The stored data in QB determines whether M7 is in the on- or in the off-state. Thus, when the line capacitor of $BL^{(R)}$ is pre-charged to V_{DD} and the $WL^{(R)}$ is activated, it is possible to interpret the QB value according to whether the C_{BLR} discharges or remains stuck at V_{DD}. Since the state of the cross-coupled inverters is not perturbed during the read, the RSNMs in the 8T cells correspond practically to the HSNMs of the corresponding 6T cells. Furthermore, the RSNMs of the 6T cells corresponds to the immunity margins of the (8T) half-selected cell [15].

Since the static behavior can be derived from the 6T SNMs, and the write is in fact the same as in 6T, the benchmark of our proposal (i.e., O-AT 6T cell with read at $V_{DD}/2$) with the TFET 8T cell (and the corresponding CMOS topologies) reduces to a comparison of the read delays reported in Fig. 8. The 8T performs better than the 6T with pre-charge at $V_{DD}/2$ since the boundary V_{DD} for which TFET cells outperform the corresponding CMOS increases by ~50mV. However, since the 8T solution leads to an area penalty by two further transistors, one can still use the 6T TFET with pre-charge at half V_{DD}. If performance is more important, the 8T TFET is preferable.

In [15], where the proposed topology featured a much slower write delay than the 8T one, *write assist* techniques have been investigated in order to mitigate the gap. However, since in the 6T topology with pre-charge at $V_{DD}/2$ the dynamic performance are comparable with the 8T cell, we believe that write assist techniques are not necessary. Moreover, read to half V_{DD} can be interpreted as a *read assist* technique.

G. INFLUENCE OF THE I_{OFF} TARGET

The boundary V_{DD} voltage of approximately 300 mV at which TFET and CMOS cells performance cross is close

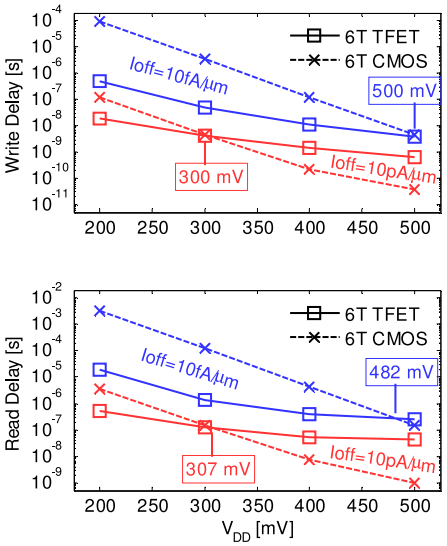

FIGURE 9. Comparison of write and read delays as a function of V_{DD} of the 6T O-AT TFET and 6T CMOS cells implemented with devices whose I_{OFF} was aligned at either 10 pA/um or at 10 fA/um (Fig. 3).

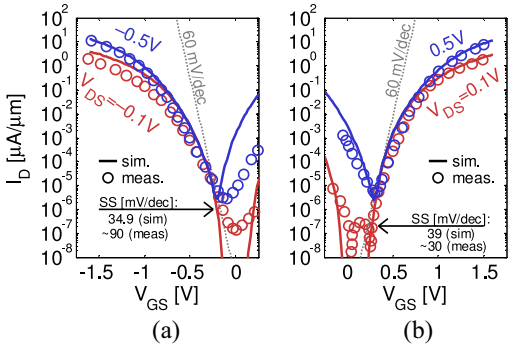

FIGURE 10. Measured [6] and simulated [17] I_D-V_{GS} characteristics of the same device biased as (a) p- and (b) n-mode TFET for $V_{DS} = \pm 0.1$ V and ± 0.5 V.

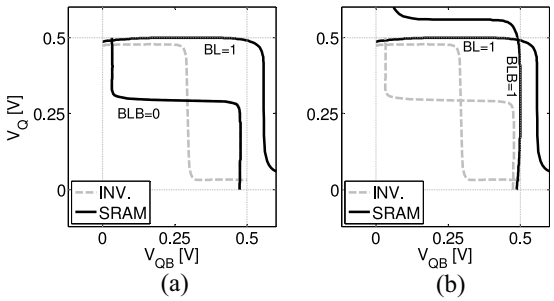

FIGURE 11. Butterfly curves in hold condition (WL = 0) for the I-AT configuration at various BL(B) voltage levels, compared with the pure inverter VTCs ($V_{DD} = 0.5$ V). Devices from [6] and [17] (I_D-V_{GS} in Fig. 10) with $W_{PD} = W_{PU} = W_{AT}$. (a) I-AT: hold (write). (b) I-AT: hold (read).

to the one found from the comparison of the TFET and CMOS I_D-V_{GS} characteristics in Fig. 3 at I_{OFF} = 10 pA/μm. Since from Figs. 7 and 8 one concludes that TFETs are recommended only for such low V_{DD}, we performed further simulations at I_{OFF} = 10 fA/μm (see I_D-V_{GS} in Fig. 3) to estimate the crossover V_{DD} in such case.

Fig. 9 shows that the voltage range where TFETs may be advantageous over CMOS is critically affected by the target I_{OFF}, and the application window for TFET widens with decreasing off-current.

III. 6T SRAM CELLS WITH CALIBRATED TFETS

Now we repeat the analysis of the SNMs and delays considering TFET structures and parameters calibrated on experimental data with the aim of assessing the impact of TFET ambipolarity and low on-current values.

A. THE EFFECTS OF TFET AMBIPOLARITY ON SRAM CELLS

The transistor considered in this sub-section is the trigate TFET employed to make the TFET inverter reported in [6]. Since the N/PTFETs are physically identical [6], the n- or p-operation mode was exclusively determined by the biasing. It is worth noting that the S region in the n-mode (i.e., the p+ doped pocket) becomes the D region in the p-mode convention. At the same time, the n+ pocket is the D/S for the N/PTFET, respectively. Unfortunately, since both junctions are designed to be used as tunneling junction (but in different operation modes), when the gate voltage is near to 0 V the band diagram is sufficiently steep at both interfaces, leading to an ambipolar behavior (see Fig. 10).

Although the ambipolarity is a parasitic effect and some techniques for reducing have been already demonstrated experimentally [21], [22], we investigated the feasibility of symmetric TFET-based 6T SRAM cells using the ambipolar devices whose calibration has been shown in [17] and the 6T TFET topologies (with either I-ATs or O-ATs) discussed so far.

Since the TFET can operate both as n- and p-type (depending on the biasing), the off-state is not strictly controlled by the gate to source voltage when it is employed as AT. In fact for a positive V_{DS} (terminal names related to n-mode convention), it can switch to the on-state both if V_{GS} increases (for $V_{GS} > 0$) and if V_{GD} decreases (for $V_{GD} < 0$). In Fig. 11, the data retention of a minimum-size (W_{AT} = W_{PD} = W_{PU}) SRAM cell implemented with the devices of Fig. 10 [17] is evaluated through the butterfly curves of the I-ATs configuration. The BL and BLB were either set to logic '1' and '0' (a) or both to logic '1' (b), to measure the hold-ability (WL = '0') of the cell under test during read and write operations of a cell in the same column. The figure reports also the butterfly curves obtained from the pure inverter VTCs without considering the ATs (dotted grey lines). When the I-AT is added, even if it is biased with $V_G{}^{AT} = V_{WL} = 0$ V, the VTC related to the side with the bit-line at '1' is considerably deformed and the transition to the low logic level eventually takes places at V_{QB} larger than V_{DD} (i.e., when the drivability of the PD transistor becomes stronger than that of the PU and AT transistors), so that the cell is no more bi-stable. This is due to the fact that, when

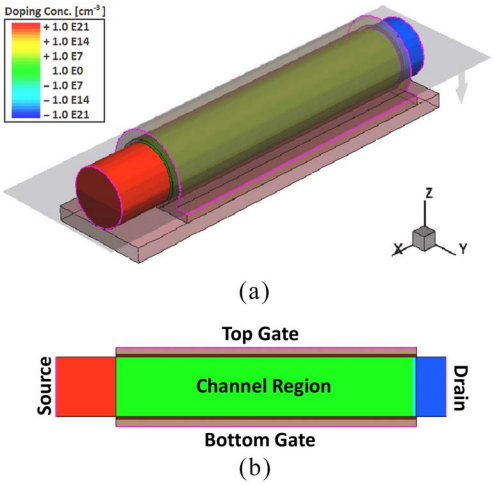

FIGURE 12. **(a) Simulated 3-D structure of a p-type TFET that reproduces the sSi NW reported in [22] and its (b) 2-D approximation (figures not in scale).**

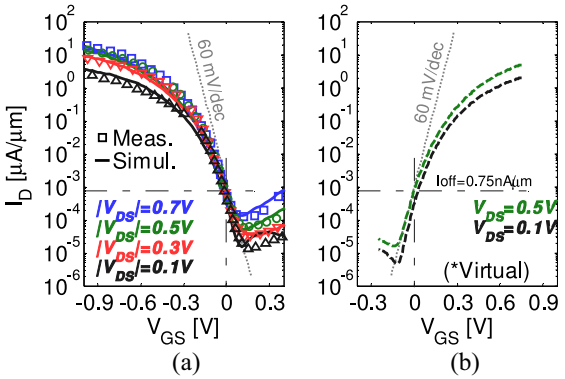

FIGURE 13. **(a) Measured [22] and simulated (2-D mesh) I_D-V_{GS} characteristics of the p-type NW in Fig. 12 for V_{DS} ranging from -0.1 V to -0.7 V (step: -0.2 V). I_D is normalized to the cross section circumference (diameter = 20 nm). (b) Simulated I_D-V_{GS} characteristics of a virtual n-type TFET NW defined by reversing the doping types of the S and D regions of the PTFET. The minimum experimental SS was 69 mV/dec at I_{OFF} = 0.25 μA/μm. For the same current level, the simulated SS is 63.3 mV/dec for both n-type and p-type NW.**

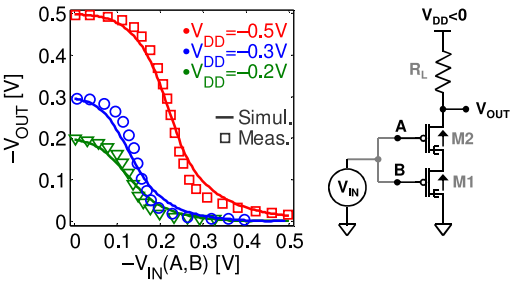

FIGURE 14. **Measured [22] and simulated VTCs of a p-NAND logic gate (the two inputs A and B are tied together). R_L = 500 kΩ (2 MΩ) for the VTC traced with V_{DD} = −0.5 V (−0.3 V and −0.2 V).**

the WL is at the low level and the BL (and/or BLB) is at V_{DD}, the I-AT turns on as a PTFET since the V_{GD} (i.e., V_{GS} if the name of terminals refer to the p-type convention) is $-V_{DD}$. A similar situation occurs for the O-AT configuration when the BL (and/or BLB) is set to logic '0' and for different V_{DD} values.

We can conclude that the ambipolarity of such TFETs degrades the operation of the SRAM cells so severely that it prevents the storage operation. Although we have simulated only 6T cells, similar considerations apply also to other proposed SRAM topologies [9]-[15] that employ TFETs as ATs.

In [17] we presented a further model calibration on pulsed measurements performed on the same device that featured much less ambipolarity, possibly due to suppression of trap-assisted-tunneling using pulse widths shorter than the trap time constants. The simulations reported in [17] on the SRAM performance were performed with such calibration deck. However, in the last part of the present paper we propose a completely new calibration on a less ambipolar p-type NW employed in simple p-type Transistor/Resistor logic gates (i.e., Inverter and NAND) [22].

B. MODELS CALIBRATED ON STATE-OF-THE ART PTFET WITH REDUCED AMBIPOLARITY

In this section, we consider the p-type gate-all-around (GAA) NW TFET published in [22]. Device processing is very similar to the one employed for the aforementioned trigate TFET [6]. However, solutions were adopted to suppress the ambipolar I_D-V_{GS} characteristics, as the dimension scaling toward a 20 nm diameter GAA NW (the channel length is 200 nm) and the asymmetric doping strategy with an n+ pocket at the S side and a low doping at the D side.

As in [17] we reproduced the NW structure with a 3D template (Fig. 12(a)) and a 2D one (Fig. 12(b)) that can be seen as a horizontal cut, except for the oxide thickness, reduced by 20% in the 2D structure to match the electrostatics of the 3D one. The doping levels are $N_D = 4{\cdot}10^{20}$ cm^{-3} and $N_A = 10^{19}$ cm^{-3}, the pocket lengths 10 nm and 5 nm for the n+ pocket and for the p+ pocket, respectively. Regarding the adjustable model parameters, the effective masses m_c and m_v were set to $0.35{\cdot}m_0$ in the S and channel regions, and to $0.55{\cdot}m_0$ in the D region, while the pre-factors g_c and g_v [18] were kept to their default values. In addition, the E_{G0} (i.e., energy gap at 0 K) of sSi was modified to 1 eV. This deck of calibrated parameters leads to the satisfactory agreement between simulated and experimental characteristics illustrated in Fig. 13(a). Even if logic gates have been already fabricated with this device, the lack of an n-type GAA NW with a similar behavior forced the group to design pull-down resistors instead of NTFETs, as in the case of the p-logic NAND gate [22] (see the schematic and the mixed-mode simulations compared with experimental data in Fig. 14). In this respect, we have defined a virtual n-type device (Fig. 13(b)) simply by reversing the S/D doping type to minimize the p/n imbalance, in order to simulate complementary TFET circuits with a reasonable agreement of the existing TFET technology performance.

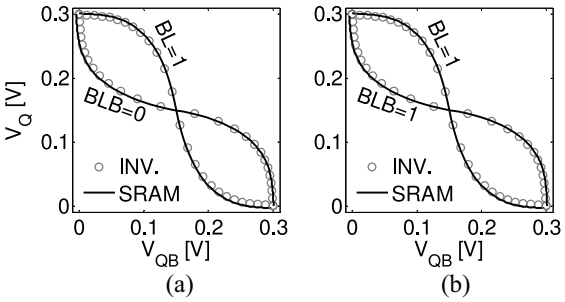

FIGURE 15. Butterfly curves in hold condition (WL = 0) for the O-AT configuration at various BL(B) logic levels, compared with the pure inverter VTCs (V_{DD} = 0.3 V). Devices of Fig. 12 with $W_{PD} = W_{PU} = W_{AT}$. (a) O-AT: hold (write). (b) O-AT: hold (read).

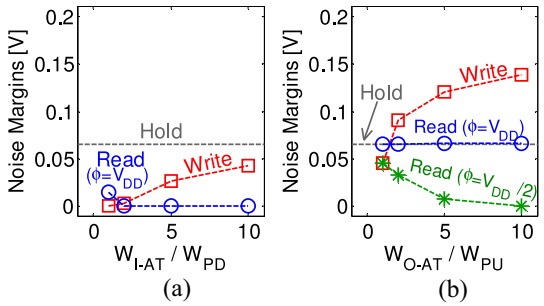

FIGURE 16. Hold, read, and write static noise margins (SNMs) of full-TFET 6T SRAM cell with (a) inward-AT or (b) outward-AT. V_{DD} = 0.3 V. Devices in Fig. 12 with $W_{PD} = W_{PU}$.

C. PERFORMANCE OF 6T SRAM CELLS

In Section II we have demonstrated that the 6T O-AT SRAM cell may outperform the equivalent CMOS cell at a $V_{DD} < V_{Boundary}$ that depends on the targeted off-current.

In this section the O-AT SRAM cell performance, implemented with the p-type GAA NW of Section III-B and the equivalent virtual n-type device whose characteristics are in Fig. 13(b), is compared with the same 6T SRAM cell configuration implemented with the idealized template devices of Section II. However, the devices of Section III-B feature an off-current I_{OFF} of about 0.75 nA/μm (Fig. 13). For this reason, here we translate the I_D-V_{GS} characteristics of the TFET templates of Section II to assure a comparison for the same I_{OFF}.

Due to minimized ambipolarity, the storage operation is ensured by the good switching off capability of the AT, as demonstrated by the overlap between the SRAM butterfly curves simulated in hold operation (WL = '0', Fig. 15) and the inverter VTCs (in contrast to the results in Fig. 11).

The trends of the static simulations (Fig. 16) were basically in line with what we found in Section II (Fig. 6(a) and (b)), but with a general reduction of the SNMs mainly due to the reduced intrinsic voltage gain of the inverter. Furthermore, the read and write delays are 1-2 decades longer than the ones expected from the idealized templates used in Section II (Fig. 17), which emphasizes that the lag between fabricated TFETs and the template TFETs with proven advantages over conventional CMOS is still large and requires many efforts at the device level.

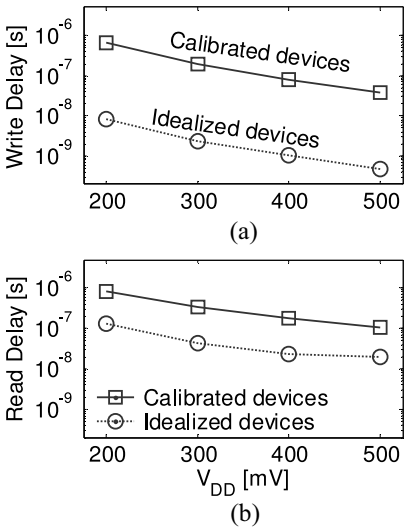

FIGURE 17. Write (a) and read (b) delays for various V_{DD}s of 6T SRAM cells implemented with the TFET templates of Section II and with the calibrated devices of Section III. I_{OFF} = 0.75 nA/μm. Precharge for read is V_{DD}/2.

IV. CONCLUSION

In this paper we presented a study on symmetric 6T SRAM cells implemented with both idealized template TFETs and TFET structures calibrated against state of the art devices [6], [22].

We used TFET templates with much better characteristics compared to actual fabricated samples to address the unidirectional current limit of TFETs when they are employed in 6T SRAM cells. Our results show that only the configuration with outward ATs could achieve both acceptable read and write SNMs, but the read delay was unacceptable (i.e., 10 ms at V_{DD} = 0.3V, not shown). However, a BL pre-charge to V_{DD}/2 allowed a reasonable read delay and a reduced performance degradation at scaled supply voltage.

Calibrations of the effective model parameters were then performed on realistic devices. The first considered samples were severely affected by ambipolarity, therefore it allowed us to investigate the effects of such behavior on 6T SRAM cells. Our results show that ambipolarity affects the gate control of TFET in off-state, thus preventing the SRAM cell data retention. Calibration on a less ambipolar PTFET allowed us to make a reliable estimation of the performance of actually fabricated devices. Our results demonstrated an alarming lag between simulations on idealized template transistors and fabricated devices. However, since further optimizations are required at device levels in order to bridge this gap, we hope that our benchmark will encourage people to look for solutions that can boost the performance of this potentially disruptive technology.

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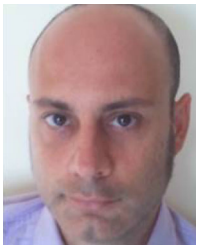
SEBASTIANO STRANGIO received the M.S. degree in electronic engineering from the University of Calabria, Cosenza, Italy, in 2012, where he is currently pursuing the Ph.D. degree. In 2012, he was a Visiting Student at the Interuniversity Microelectronics Center, Leuven, Belgium, for six months. Since 2013, he has been with the University of Udine, Udine, Italy, as a Contract Researcher. His current research interests include electrical characterizations of Resistive Random Access Memory and TCAD simulations of TFET.

PIERPAOLO PALESTRI received the Laurea degree from the University of Bologna, Bologna, Italy, in 1998, and the Ph.D. degree from the University of Udine, Udine, Italy, in 2003, both in electronic engineering. From 2000 to 2001, he was a Post-Doctoral Research Fellow at Bell Laboratories, Lucent Technologies, Murray Hill, NJ, USA. He was a Research Associate and an Associate Professor at the University of Udine, in 2001 and 2005, respectively. His current research interests include the modeling of carrier transport, hot-carriers, and tunneling phenomena in nanoscale devices and nonvolatile memory cells, as well as the design of integrated circuits for high-frequency applications. He has co-authored over 180 papers in international journal and conferences with peer review.

DAVID ESSENI (S'98–M'00–SM'06–F'13) received the Ph.D. degree in electronic engineering from the University of Bologna, Bologna, Italy, in 1999. During 2000, he was a Visiting Scientist at Bell Laboratories, Murray Hill, NJ, USA, and in 2013, he was a Fulbright Research Scholar at the Notre Dame University, Notre Dame, IN, USA. Since 2005, he has been an Associate Professor at the University of Udine, Udine, Italy. His current research interests include the characterization, modeling, and reliability of CMOS and beyond CMOS transistors. He has served or is serving with the Technical Program Committee (TPC) of the International Electron Devices Meeting (IEDM), International Reliability Physics Symposium (IRPS), and European Solid-State Device Research Conference (ESSDERC). He is an Associate Editor of the IEEE Transactions on Electron Devices.

LUCA SELMI received the Ph.D. degree in electronic engineering from the University of Bologna, Bologna, Italy, in 1989. Since 2000, he has been a Professor of Electronics at the University of Udine, Udine, Italy. His current research interests in modeling, simulation, characterization, and reliability of nanoscale MOSFETs and Non Volatile Memory cells. He has been a TPC Committee Member of numerous electron device conferences such as IEDM, ESSDERC, Insulating Films on Semiconductors, International Conference on Microelectronic Test Structures, and Ultimate Integration on Silicon.



FELICE CRUPI received the M.S. degree in electronic engineering from the University of Messina, Messina, Italy, and the Ph.D. degree from the University of Firenze, Firenze, Italy, in 1997 and 2001, respectively. Since 1998, he has been a repeat Visiting Scientist with IMEC, Leuven, Belgium. Since 2002, he has been with the University of Calabria, Cosenza, Italy, as an Associate Professor of Electronics. His main research interests include reliability of CMOS devices, electrical characterization techniques for solid state electronic devices, modeling and simulation of CMOS devices, the design of ultra-low noise electronic instrumentation, and the design of extremely low power CMOS circuits. He has authored and co-authored over 150 papers published in peer-reviewed journals and in international conference proceedings. He is an Associate Editor of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY. He served as a Technical Program Committe Member of the IEEE International Electron Devices Meeting and the IEEE International Reliability Physics Symposium.

SIMON RICHTER received the M.S. and Ph.D. degrees in physics from the RWTH Aachen University, Aachen, Germany, in 2009 and 2014, respectively. He is currently with Peter Grünberg Institute-9, Jülich, Germany. His current research interests include integration of TFETs for digital logic and analog applications.

QING-TAI ZHAO (M'11) received the Ph.D. degree in physics from Peking University, Beijing, China, in 1993. He was at the Institute of Microelectronics, Peking University. In 1997, he joined Peter Grünberg Institute-9, Jülich, Germany, where he is currently a Senior Research Scientist and the Leader of Nano-Device Research Group. His current research interests include Si/SiGe-based devices and technology, nanowire devices, and tunnel-FETs. He has authored or co-authored of over 200 scientific papers and holds over ten patents.

SIEGFRIED MANTL (M'04) received the Ph.D. degree from the University of Innsbruck, Innsbruck, Austria, in 1976. Since 1971, he has been with the Research Center Jülich, Jülich, Germany. He is the Head of the Ion Beam Division, Peter Grünberg Institute-9, Jülich, and a Professor of Physics at Aachen University of Technology, Aachen, Germany. His current research interests include the research of nano-electronic materials and nanodevices, various thin film growth methods, and ion beam techniques. He has authored or co-authored over 340 journal articles, several book chapters, and review articles, and holds over 20 patents. He was the recipient of an Honorary Helmholtz Professorship for his pioneering work in the field of strained silicon structures in 2011.