Self-Heating Phase-Change Memory-Array Demonstrator for True Random Number Generation

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***Abstract*—The stochastic nature of the switching mechanism of phase-change memory (PCM) arrays, which is a drawback for memory applications, can fruitfully be exploited to implement primitives for hardware security. By applying a set voltage pulse, whose amplitude corresponds to a switching probability of 50%, to a memory array initially placed in the full-reset state, half of the memory bits are statistically switched and programmed to state "1", whereas the remainder of the bits persist in state "0". Such a natural randomness can be exploited to create a True Random Number Generator (TRNG), which is the building block of cryptographic applications. The feasibility of a TRNG by means of self-heating PCM cells is assessed and demonstrated through simulations based upon Random Network Model, i.e., a microscopic transport model previously developed and tested by the authors.**

***Index Terms*—Random Number Generator, Semiconductor device modeling, Semiconductor memories**

I. Introduction

A number of chalcogenide materials have been investigated in the last decade in view of their possible exploitation in the non-volatile memory technology. As a matter of fact, chalcogenides like, e.g., $Ge_2Sb_2Te_5$ (a.k.a. GST-225), can easily be made to switch between the amorphous and crystalline states upon the application of an appropriate voltage pulse (Memory Switch, MS). Since the two phases differ in resistivity by orders of magnitude, given the same voltage pulse, a high or a low current is measured depending on the chalcogenide phase. By controlling the external pulse the information is encoded and stored permanently [1], [2]. More recently, other classes of chalcogenide materials have been investigated in order to manufacture selector devices that provide access to the single bits of a memory array [3], [4]. In contrast to those used for storage purposes, these chalcogenides do not undergo a phase change, but feature the so-called Ovonic Threshold Switch (OTS), i.e., a sudden reversible change in the resistivity of the amorphous phase when a voltage pulse larger than a threshold value is applied [5]. The perfect matching between the bit-access device pair is of the utmost importance for enabling stackable 3D geometries that combine high-speed response with a very dense storage capability [6].

In a memory array, the threshold voltage for MS and OTS is not a fixed value, but is statistically dispersed. From the design viewpoint, the goal of manufacturers is finding suitable materials and architectures that minimize variability in order to standardize the device behavior and increase reliability. Despite their efforts, in a real array differences are unavoidable. A recent investigation has compared emerging non-volatile memory concepts, like Phase-Change RAMs, resistive RAMs and Spin-Transfer Torque Magnetic RAMs, revealing that they are also suitable memristors for hardware security [7]. Among them, oxide-based resistive RAMs have been studied in depth [8], as they have a large threshold dispersion. In the present work we apply a simulative approach, called *Random Network Model*, to a small (4-kbit) chip made of self-heating phase-change RAMs, whose theoretical threshold dispersion is comparable to, or even larger than, that of oxide-based resistive RAMs. After assessing its statistical properties, we demonstrate that the chip can be used as a simple True Random Number Generator (TRNG).

Random numbers are essential in cryptography, Monte Carlo and numerical simulations, gambling, lotteries and many other applications [9]. Due to the growing impact of many of these fields on modern society, methods for generating random numbers, using both mathematical algorithms (pseudorandom generators, PRNGs) and nondeterministic physical processes (true generators), have been thoroughly investigated [9]. With respect to PRNGs, TRNGs do not need a seed and make instead use of the entropy coming from a physical phenomenon (e.g., noise, ring oscillator jitter, electric breakdown), so that the obtained random numbers are never reproducible nor predictable, with a notable positive impact on security applications. In principle, any phenomenon affected by inherent variability, i.e., not connected to the measuring system, is suitable for TRNGs: the larger the variability window, the less sensitive the generator to small fluctuations of the biasing signal. The quality of randomness is evaluated by the NIST test suite [10], that represents a *de facto* standard.

II. Sources of variability

The threshold variability is commonly ascribed to two main sources: structural differences from cell to cell due to unavoidable process variations (*intercell* variability) and the inherent stochastic nature of the amorphous phase (*intracell* variability) [11], [12], [13]. Let the experimental threshold voltages $V_{\rm th}$ be measured on Q cells that have undergone P amorphization-crystallization cycles, and let

$$\overline{V}^s_{\rm th} = \frac{1}{P}\sum_{k=1}^{P} V^{sk}_{\rm th} \qquad \overline{V}_{\rm th} = \frac{1}{Q}\sum_{s=1}^{Q} \overline{V}^s_{\rm th}\,,$$

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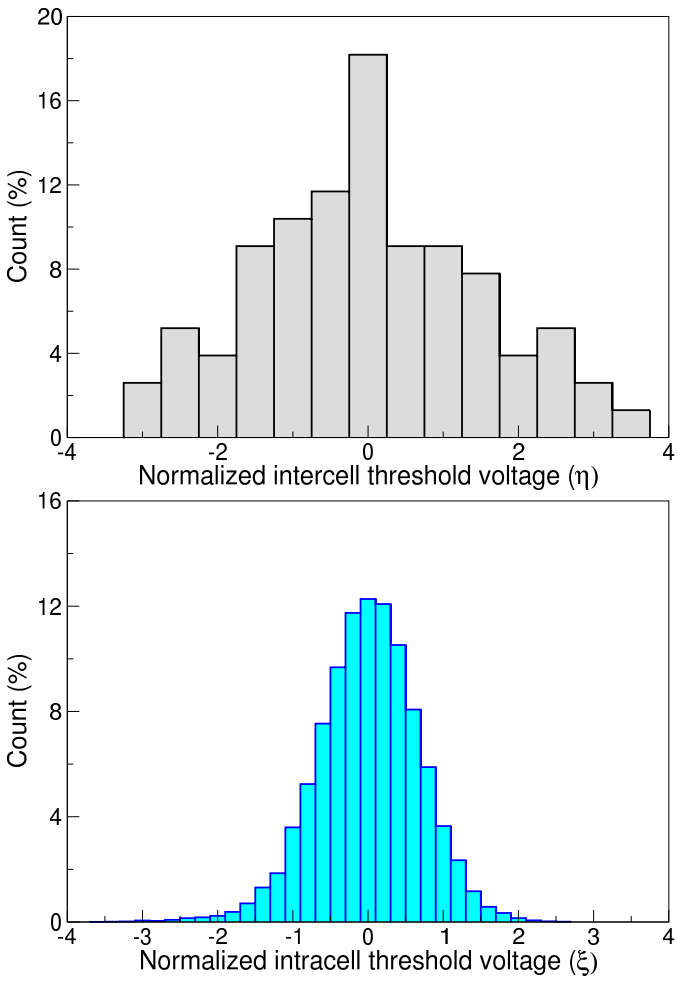

Fig. 1. Intercell (top) and intracell (bottom) threshold-voltage distributions for a phase-change memory array composed of conventional mushroom cells that feature a large cross-section of about 2500 nm^2.

with $V_{\rm th}^{sk}$ being the threshold voltage of the k-th measurement on the s-th cell.

The effects of the process variation and of the stochastic nature of the amorphous phase are separated by calculating and binning the normalized intercell threshold voltage $\eta = \overline{V}^s_{\rm th}/\overline{V}_{\rm th} - 1$ and the normalized intracell threshold voltage $\xi = V_{\rm th}^{sk}/\overline{V}^s_{\rm th} - 1$, respectively. Their relative weights depend primarily on the manufacturing technology. From the design viewpoint, the goal of memory manufacturers is obtaining arrays with very narrow dispersions for both sources of variability in order to standardize the device behavior and increase reliability. For TNRGs, instead, the constraint is still strict only for intercell variability.

Conventional chalcogenide-based memory arrays in the mushroom (or μ-trench) configuration make use of heaters to pump thermal power into the chalcogenide layer. The phase change thus begins always in a dome close to the heater itself [14]; moreover, the efficiency of the thermal transfer is strongly influenced by the shape of the heater/chalcogenide interface [15] and by the material the heater is made of [16]. For these reasons, the mushroom configuration gives origin to a sufficiently narrow dispersion of ξ and, consequently, makes the intercell variability η connected to process variations more evident. An example of experimental distributions of η and ξ is given in Fig. 1.

At the opposite side, in a self-heating cell the phase change is due only to the Joule heating produced by the current flux within the chalcogenide layer [17], [18], [19]. The amorphous-crystalline transition begins in a hot spot within the chalcogenide layer, where the local nanostructure accommodates thermodynamic conditions favorable to nucleation, as a consequence of the energy dissipation provided by electric transport; then, the nuclei grow and form a filament that eventually connects the two contacts. A complete reset operation implies the movement and rearrangement of the atoms giving origin to a different amorphous-phase structure at the nanoscale. This phenomenon may produce a larger dispersion of the scattering centers than that occurring in resistive RAMs, where the conductive filaments are generated only at grain boundaries during forming. The amorphous phase structure of phase-change RAMs features, in fact, a large number of dangling bonds and other structural defects that give origin to tails of the valence and conduction bands, and to *trap states* within the energy gap [20]. The space position [21] and height of the energy barriers of the trap states [22] vary from sample to sample and from an amorphization cycle to another, so that the electric and thermal responses to a given bias strongly depend on them. Consequently, the hot spots for nucleation are always different, and the inherent stochastic nature of the amorphous phase rules over process variability. As shown in Fig. 2, it gives origin to a larger dispersion window due to the combined action of the electric transport and the thermodynamics of crystallization. Moreover, the dispersion of the threshold voltage becomes even larger when the device size shrinks, because the statistical nature of the defective-state distribution within the amorphous lattice gains progressively importance.

III. The Random Network Model

Several theories have been proposed so far to describe carrier transport in amorphous chalcogenides, taking into consideration impact ionization [20], thermal effects [23], filamentary conduction [24], and trap-limited transport [25], [26], [27], [28]. Among them, continuum-medium analytical models for filamentary conduction and, to a larger extent, for thermally-assisted trap-limited transport, have been published, and have obtained a large consensus in the scientific community. The Random Network Model introduced by Cappelli *et al.* [21] is a trap-limited-based approach that disposes of the one-dimensional and the continuum-medium approximations, and allows for statistical analyses at the microscopic scale. Originally developed for Ovonic switching, it was then extended to incorporate the phase change of self-heating cells [29].

The starting point of the Random Network Model is the representation of the amorphous chalcogenide domain. As explained in Sect. II, every amorphization process gives origin to a nanostructurally-different lattice due to the stochastic generation of traps. In order to account for such differences, a number of parallel simulations are run, each of them

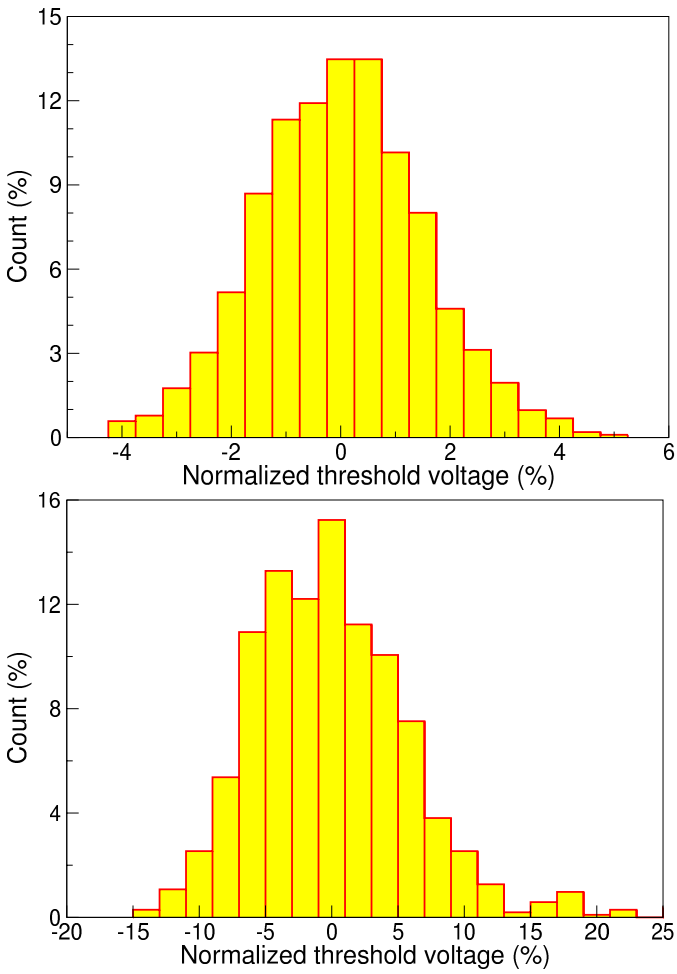

Fig. 2. Simulations of the threshold voltage dispersion of 1024 cells with (top) and without (bottom) heater, with a 100 nm^2 cross section. The simulation of the mushroom cell has been performed by adapting the framework of Ref. [14] and assuming a Gaussian distribution (mean value $\mu = 72$ K/V^2, standard deviation $\sigma = \pm 3\%$) for the R_{th}/R_h ratio to include process variability.

generating N scattering centers at different places in the domain. These centers mimic the clusters of traps that are generated during amorphization; they are connected to each other and to the contacts within a cutoff distance $r_{\rm cut}$, thus creating a network than spans the simulation domain. Each center features its own electrostatic potential φ_i and carrier temperature T_i, and hosts a carrier concentration n_i, whose elements have the common energy e_i. Transitions originating from the scattering center i to any of the possible destination centers j connected to it involve detrapping, propagation and trapping events, all summarized in the scattering rate [21]:

$$S_{ij} = \frac{1}{\tau_\circ} \exp\left(-\frac{E_c - e_i}{k_B\, T_i}\right) \exp\left[\frac{-q\,(\varphi_i - \varphi_j)\,\ell}{r_{ij}\, k_B\, T_i}\right]. \quad (1)$$

In the above, $\tau_\circ$ is a characteristic scattering time, r_{ij} and ℓ are the inter-center distance and the average width of the confining barrier along the $i \to j$ line, respectively, E_c is the energy of the bottom of the conduction band, q is the electron charge and k_B is the Boltzmann constant. In steady state, given an input current I, the charge- and energy-balance equations read:

$$\frac{I}{-q}\,\delta_{0,i} + \sum_{j\neq i} n_j\, S_{ji} = n_i \sum_{j\neq i} S_{ij} + \frac{I}{-q}\,\delta_{N+1,i} \quad (2)$$

and

$$\sum_{j\neq i} n_j\, S_{ji}\left[e_j - q\,(\varphi_j - \varphi_i)\right] + \frac{I}{-q}\, e_i\, \delta_{0,i} = \\ = e_i\left[n_i \sum_{j\neq i} S_{ij} + \frac{I}{-q}\,\delta_{N+1,i}\right] + n_i\,\frac{e_i - e_{i,\rm eq}}{\tau_R}\,, \quad (3)$$

where indices 0 and $N+1$ in Kronecker's delta functions are associated to the two contacts. The last summand of (3) accounts for energy relaxation to the lattice, $e_{i,\rm eq}$ being the equilibrium energy of the carriers at the ith scattering center, and τ_R a relaxation-time constant, respectively.
The Poisson and Fourier-heat equations also add to the model and must be solved over the entire simulation domain:

$$\nabla\cdot(\varepsilon\,\nabla\varphi) + Q_i = 0\,, \quad (4)$$

$$\nabla\cdot(\kappa\,\nabla T) + W_{ij} = 0\,. \quad (5)$$

The right hand sides $Q_i = -q\,(n_i - n_{i,\rm eq})$ and $W_{ij} = q\,(n_i\, S_{ij} - n_j\, S_{ji})\,\left[e_i - e_j - q\,(\varphi_i - \varphi_j)\right]$ apply at the scattering centers and along the straight lines connecting them, respectively, whereas they vanish elsewhere; in the expression of Q_i in (4), $n_{i,\rm eq}$ is the carrier concentration that, in the equilibrium condition, provides charge neutrality. The numerical solution of (2)-(5) yields the electrostatic potential φ_k, the temperature T_k over the entire domain, the carrier concentration n_i and the energy e_i at the scattering centers. In order to incorporate the phase-change mechanism, the average temperatures of the transition lines $i \to j$ and that of the simulation domain are evaluated at each iteration; if one of them exceeds the glass transition temperature T_g of the chalcogenide layer, a crystallization event takes place and the parameters of that sub-domain are adjusted accordingly. For further details, we refer the reader to the original papers about the Random Network Model [21], [29], [30].

IV. Results

A. Calibration

A feasibility study of self-heating, phase-change memories as sources of primitives for security applications requires preliminary actions. First, it is necessary to calibrate the model with respect to some experimental data, and find the average biasing condition that induces the phase change. Prototypes of self-aligned memory cells contacted with carbon nanotubes (CNT) [19], [31] have been considered as reference devices, since the phase change is induced by the current flowing through the memory and not by a heater. On the modeling side, such concepts have been simplified as shown in Fig. 3, where a test cell made of a SiO_2 substrate with a GST-225 chalcogenide layer lying on top of it is represented. Two parallel plates at the opposite sides represent the two contacts, which are rendered in the simulation with specific thermal and electric boundary conditions. The prismatic region within

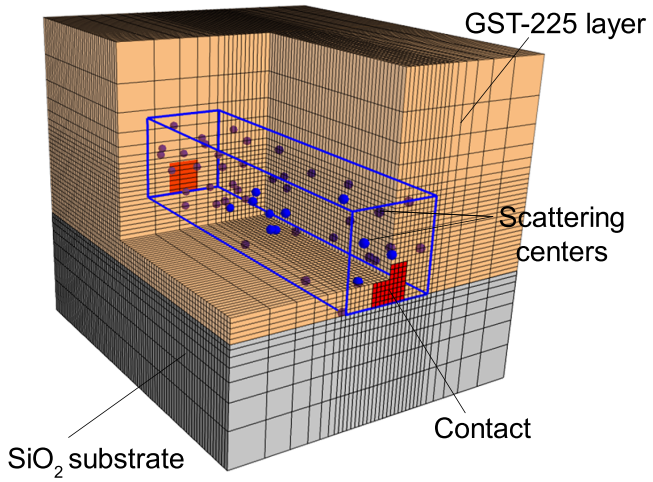

Fig. 3. Geometry, elements and layers composing the simulated cell. The boxed volume represents the transport-active subdomain of the device; part of it has been removed from the representation to make the interior visible. The active subdomain is surrounded by a buffer chalcogenide volume that prevents undesired cross-talk effects with the adjacent cells.

TABLE I
LIST OF PARAMETERS USED IN THE SIMULATIONS

Parameter	Value	Parameter	Value
N	48	$\varepsilon_{\mathrm{GST}}$	$15\,\varepsilon_{\mathrm{o}}$
r_{cut}	6 nm	$\varepsilon_{\mathrm{subs}}$	$3.9\,\varepsilon_{\mathrm{o}}$
ℓ	2.9 nm	$E_c - e_{\mathrm{eq}}$	0.3 eV
$r_{ij,\mathrm{min}}$	2.8 nm	n_{eq}	$1.2 \cdot 10^{19}$ cm^{-3}
τ_{o}	49 fs	κ	0.2 W/(m K)
τ_R	5 fs	T_g	420 K

the chalcogenide layer delimited by the two plates defines the active subdomain, whereas the surrounding volume is the guard ring preventing electric or thermal cross-talk with the adjacent memory cells. Model calibration has been performed against experimental data of a 40-nm long, self-heating GST-CNT device [19] with a 100 nm^2 cross-section. The set of optimized parameters have been adjusted from those of case L40 in [21] in order to introduce the phase change. The complete set is listed in table I.

In the next stage, the electric responses of 512 cells have been simulated and compared. The cells differ from each other only in the position of the scattering centers. In the framework of the Random Network Model, running replicas of the simulation is equivalent to testing the same cell after repeated set-reset (or crystallization-amorphization) cycles, or to investigating the entire array at the same time, where each cell is a single bit, under the assumption that cross-talk effects are negligible. For the case in hand, the latter condition applies: all cells in the array undergo a preliminary amorphization process and are reset to the high-resistance state (state 0); then, a bias voltage is applied to each cell, and is increased until the switching condition is recorded (Fig. 4). The switching region spans approximately from 3.2 to 4.7 V

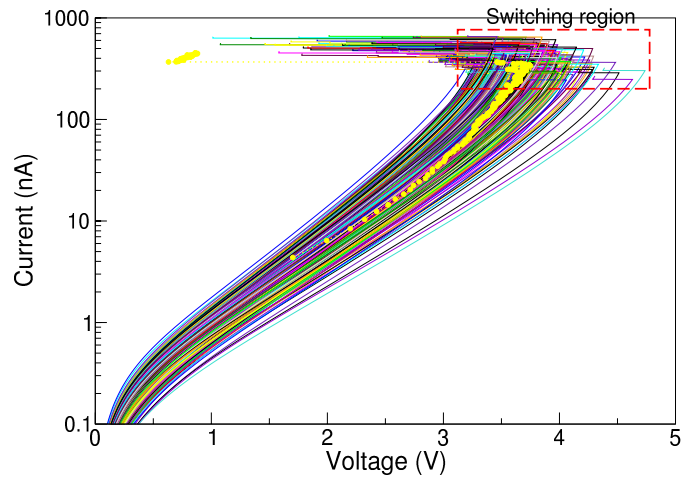

Fig. 4. Current vs. voltage characteristics of 512 bits used as reference for the preliminary investigation of the switching behavior of PCM devices. Simulation parameters have been calibrated against experimental data of a 40-nm long, self-heating GST-CNT device[19], shown as solid dots in the figure. The boxed area identifies the switching region.

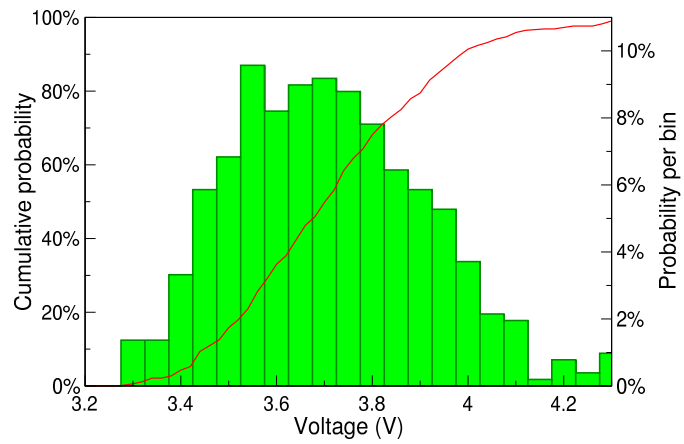

Fig. 5. Simulated distribution (histogram) and cumulated switching probability (curve) of the 512-bit self-heating phase-change memory of Fig. 4, as functions of the applied voltage.

and from 200 to 800 nA; thus, the reading window can safely be set between 1 and 2.5 V.

The simulated switching voltage distribution is also reported in Fig. 5, showing a mean value $\mu(V_{\mathrm{th}}) = 3.72$ V and a standard deviation $\sigma(V_{\mathrm{th}}) = 0.22$ V. The cumulative switch probability sets the 50th percentile (median) to $V = 3.70$ V, with a linear increase from 3.45 to 3.95 V. In other words, if one applied a 3.70 V voltage to each cell in the array, 50% of the cells would switch to the low-resistance state (state 1).

B. True Random Number Generation

1) Ideal conditions: A biasing voltage $V_{\mathrm{set}} = 3.7$ V is applied to a simulated 4-kbit demonstrator made of self-heating phase-change memory cells, initially placed in a full-reset state (bit state: 0), under ideal conditions (vanishing parasitic devices and cross-talk effects). Each cell state is then read at $V_{\mathrm{read}} = 2.0$ V. According to the preliminary analysis of Sect. IV-A, part of the cells switches to the low-resistance

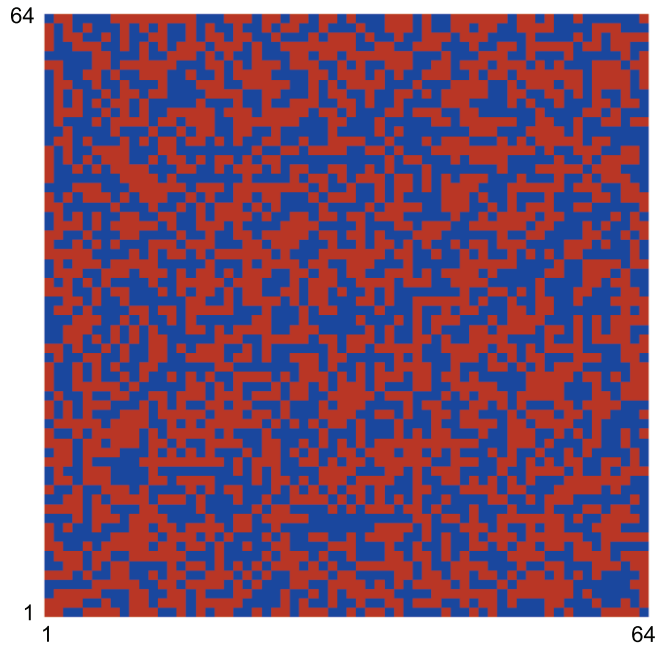

Fig. 6. Simulated map of a 4-kbit array after the application of a voltage pulse $V = 3.70$ V to each cell. Dark and bright squares indicate the 0 and 1 bits, respectively.

state, encoding the bit state 1. A pictorial representation of the array is shown in Fig. 6.

The true randomness of the switching variability can be verified with standard benchmarks, like those proposed in the NIST statistical test suite. To this purpose, data have been grouped in 32 sequences of 128 bits each. Since some tests require a number of bits larger than 10^6 to provide significant results, only the 9 tests (out of 15) applicable to the sequences generated in our study have been performed; a test is passed when the success rate is larger than $29/32$. Due to the relatively low number of bits to be processed, the following block lengths have been set according to NIST guidelines: *Block Frequency test* $M = 16$, *Non-Overlapping Template test* $m = 8$, *Approximate Entropy test* $m = 2$, and *Serial test* $m = 5$. Results are reported in Table II. The 9 applicable tests have been passed with a success rate close to 100%, which allows one to infer that the test chip is a good candidate for representing a TRNG.

2) Effect of parasitics: In a real array, parasitic voltage losses occur due to the line resistance and the presence of selector devices that allow for single-bit addressing. In principle, both types of loss alter the voltage drop across the bit, so that the probability of switching may be influenced by the position of the bit in the array: the closer the bit to the voltage source, the higher the probability of switching. The demonstrator should prove to be free of significant biasing effects; otherwise, a steadily decreasing percentage of 1-states as long as the distance from the voltage source increases would result, this jeopardizing the applicability to random number generation.

Until now, the architecture of selector devices has been based on transistors; in this application, transistors normally operate

TABLE II
RESULTS OF 9 TESTS FROM THE NIST STATISTICAL SUITE.

Test name	Success rate	Result
Frequency	$32/32$	PASS
Block Frequency	$32/32$	PASS
Cumulative Sums (forward)	$32/32$	PASS
Cumulative Sums (reverse)	$32/32$	PASS
Runs	$32/32$	PASS
Longest Run of 1's	$32/32$	PASS
FFT	$31/32$	PASS
Non Overlapping Template	$\geq 29/32$	PASS
Approximate Entropy	$32/32$	PASS
Serial (P-value$_1$)	$32/32$	PASS
Serial (P-value$_2$)	$32/32$	PASS

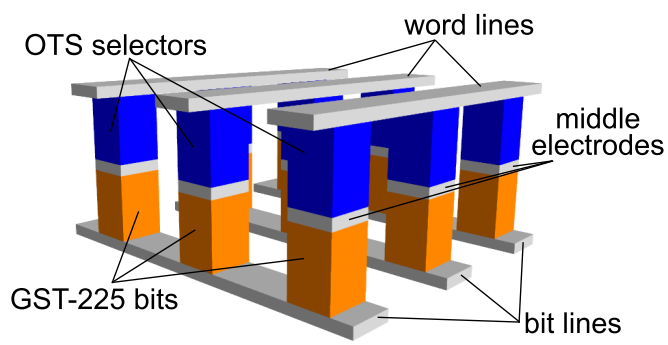

Fig. 7. Schematics of a crossbar array, where a two-terminal device like an Ovonic Threshold Switch is used as a selector.

in the OFF state, so that parasitic currents cannot alter the controlled bit. The transistors used in selectors are temporarily switched to a low-resistance (ON) state only when the bit is read, written, or erased. In the novel architecture based on crossbar arrays, transistors are typically replaced by two-terminal Ovonic devices, (Fig. 7) since the resistivities of the open (ON) and closed (OFF) states differ by more than 3 orders of magnitude [3], [6]. The voltage losses due to parasitic effects depend on the number of active cells along the bit line and word line at the same time. In order to evaluate such losses, we assume *a)* sequential access, i.e., only one cell at a time is written; *b)* an intra-chip line resistance $R_\square \approx 0.03\ \Omega$ [32] that leads, for the chip under test, to a maximum line resistance $R_L \lesssim 250\ \Omega$, identical for word and bit lines; finally, *c)* a selector resistance $R_{\rm sel} \sim 70$ MΩ for the OFF state and $R_{\rm sel} \sim 4$ kΩ for the ON state, supposing an OTS material for the selector similar to that of Ref. [3] (Fig. 8). A first-order approximation of the working point of any (b, w) cell is given by the implicit circuit equation

$$I = \frac{V_{\rm set} - V(I)}{(\alpha\,\beta + \omega)\,R_L + R_{\rm sel}}\,, \tag{6}$$

where $\alpha = W/B$ is the ratio between the number W of word and the number B of bit lines of the array (we assume here $\alpha = 1$), $\beta = b/B$ and $\omega = w/W$ are the fractional positions

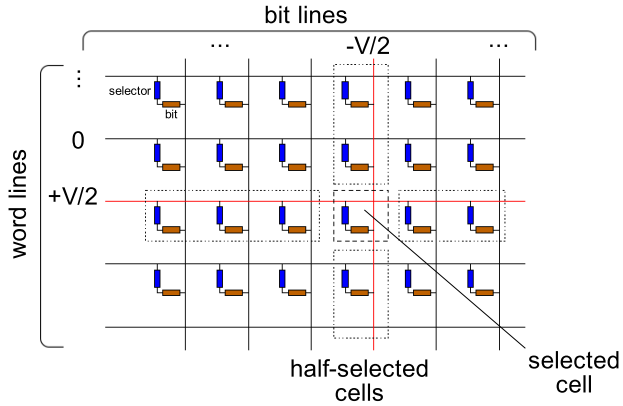

Fig. 8. Schematic circuit representation of a crossbar array. To select the active cell, $+V/2$ and $-V/2$ voltages are applied along the word and bit lines at two edges of the array, whereas unselected lines are grounded. Voltage drops occur along the wirings (line resistance $\lesssim 250\Omega$), the selector ($R_{\rm sel} \sim 70$ MΩ for the OFF state and $R_{\rm sel} \sim 4$ kΩ for the ON state), and the active bit.

along the word and bit lines, respectively, and $V(I)$ is the voltage vs. current characteristic of the actual chalcogenide bit. Since $R_L \ll R_{\rm sel}$, the first term in the denominator can be neglected in small chips, unless the uncommon case $\alpha \sim R_{\rm sel}/R_L$ occurs. Estimating $V(I)$ with the help of Fig. 4, we calculate a parasitic current in the range $I_{\rm OFF} \approx 1.3 - 4.9$ nA (average value: 2.7 nA) per half-selected cell, irrespectively of the position in the array.

Let (b^*, w^*) be the indices of the selected cell. By adding up contributions from all the closed cells in the bit and word lines (half-selected cells), we estimate the voltage drop due to parasitic currents as

$$\Delta V_{\rm hs} = \frac{R_L}{2} I_{\rm OFF} \left[\alpha \frac{b^* (b^* - 1)}{B} + \frac{w^* (w^* - 1)}{W} \right] . \quad (7)$$

This contribution is usually lower than the accuracy of the estimate of the threshold voltage provided by the Random Network Model ($\sim 10^{-3}$ V), even for Gbit-arrays (for the test chip under consideration $\Delta V_{\rm hs} \lesssim 80$ μV), and can safely be neglected.

Concerning the selected cell, in the ideal case the switching condition is given by $V_{\rm th} < V_{\rm set}$. In the real case, the presence of the selector in the ON state and of parasitic effects of the line tend to decrease the slope of the load line, so that the cells whose threshold voltages are slightly smaller than the set voltage may not switch in reality. Given the threshold current $I_{\rm th}$, the additional voltage drop due the selected cell is approximated by

$$\Delta V_{\rm s} = V_{\rm set} - V(I) = \left[\left(\alpha \frac{b^*}{B} + \frac{w^*}{W} \right) R_L + R_{\rm sel} \right] I_{\rm th} . \quad (8)$$

For currents within the switching region of Fig. 4 the maximum voltage drop for selected cells of the test array of Fig. 6 is less than 5 mV, which corresponds to a reduction of the switching probability by less than 0.5% (see Fig. 5). The lower value of the selector resistance in the ON state does not allow to assume this result independent of the position if a high number of word and bit lines makes R_L comparable to $R_{\rm sel}$. According to the line resistance above, differences do

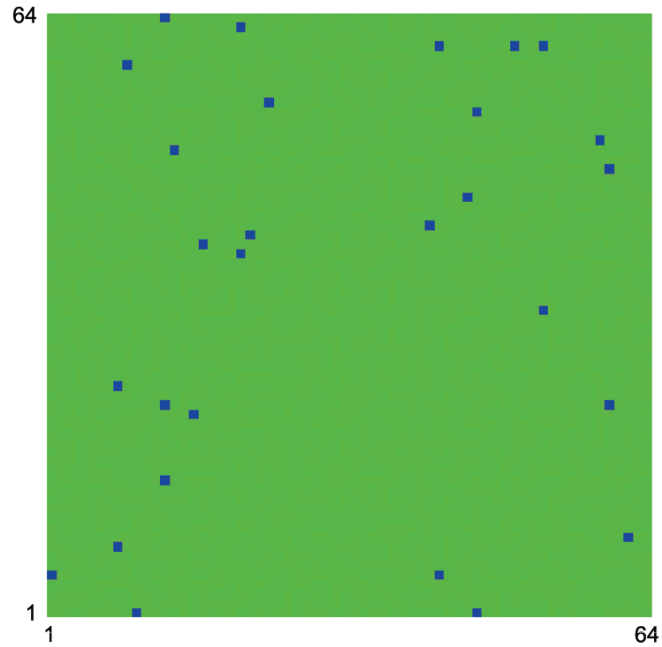

Fig. 9. Simulated map of the changes in the bit state of a 4-kbit array after the application of a voltage pulse $V = 3.70$ in presence of parasitic voltage drops. The bit positions are the same as in Fig. 6. The 28 dark squares out of 4096 (0.68%) indicate bits that failed to switch.

not exceed 1 mV every 400 lines in the worst case, so that for the demonstrator under consideration the position of the selected cell does not influence substantially the final outcome, and the non-switching bits are almost equally dispersed over the array area, as shown in Fig. 9.

Despite the fact that the number of non-switching bits of the test chip is very limited, the 9 applicable tests from the NIST benchmark have been repeated. Results and figures of merit listed in Table II are confirmed: the true randomness of the switching variability of self-heating phase-change memory cells can be exploited to create a TRNG.

V. Discussion

In the calculations above we have supposed an Ovonic selector that perfectly matches to the underlying bit, providing the same electric response to each cell. However, in a real array these responses are dispersed for the same reasons listed in Sect. II, and, in particular, it is possible to estimate the variability of the resistances in the ON and OFF states. Apart from numerical challenges connected to highly non-linear sets of equations, the Random Network Model allows for simulating also the selector. The same calibration procedure presented in Sect. IV-A applies in order to find a suitable set of parameters for the material in hand. In the absence of any further information (as a matter of fact semiconductor companies do not disclose any detail on the chalcogenides used for storage or selection), we designed the demonstrator making reference to literature data [3], [19], where GST-225 and $GeTe_6$ are identified as educated templates for the bit and the selector, respectively. The parasitic current $I_{\rm OFF}$ and the voltage drop of the selected cell $\Delta V_{\rm s}$ have been evaluated in

the worst case according to the data of [3] (minimum $R_{\rm sel}$ for the OFF state and maximum $R_{\rm sel}$ for the ON state) to stress the demonstrator. A deeper material screening, supported by experimental evidences, would certainly provide more efficient and better matching alloys for the selector and the bit, and lead to other figures, but not to a different qualitative outcome. As it stems from the calculations of Sect. IV-B2, parasitic currents due to OFF cells hardly affect the results for $R_{\rm sel} \sim 1$ MΩ and above. As far as the ON state is considered, the smaller the selector resistance, the lesser the parasitic effects, but the higher the influence of the position in the array, so that a tradeoff between the efficiency of the selector and the size of the array must be sought.

Both process variability and, under appropriate conditions, parasitic effects can slightly alter the generation of the random bits by superimposing a biasing pattern. A similar phenomenon often occurs, e.g, in optical sensors, where pixel-to-pixel variability sets in and is taken into consideration by software post-processing [33]. Algorithms like the von Neumann procedure [34] can be applied for correcting a biased random number generation at a post-processing stage; though, the architectural complexity of the generator notably increases due to the additional storage registers that are required to compare bits in successive generations.

Finally, a further element that deserves attention is multiple-time generation, which is a key challenge in order to define suitable applications for TRNGs based on non-volatile memory concepts. According to the literature, electromigration due to heavy pulsed cycling between set and reset states limits the endurance of Phase-Change RAMs around 10^9 programming cycles [2], a value that outperforms by at least two orders of magnitude the cyclability of Resistive RAMs [35]. Self-heating cells can slightly widen this gap, since they exhibit a superior endurance than mushroom cells as a consequence of the less aggressive conditions required to trigger the phase change [36]. The filamentary conduction mechanism for transport somehow similar to that of resistive RAMs, but able to eventually trigger crystallization events, on the one side, and the typical endurance of Phase-Change RAMs on the other side join together in self-heating phase-change memories, making these devices attractive also for TRNGs.

VI. Conclusion

In this paper we propose a method for exploiting the switching mechanism of self-heating, amorphous phase-change memory arrays to implement a True Random Number Generator. When a calibrated voltage pulse is applied to a full-reset PCM array (all bits in state 0), the stochastic nature of the switching mechanism is such that about one half of the memory bits are statistically switched and programmed to state 1, whereas the remainder of the bits persist in state 0. This creates a random sequence of 0s and 1s, which is unique to the array considered. In this way the randomness of the threshold distribution of the individual cells, which is a drawback of PCM arrays in the field of data storage, is given a turn for the better as it is exploited for creating a True Random Number Generator.

The simulation of a 4-kbit array demonstrator has been carried out by means of the Random Network Model for the case of prototypes of self-heating memory cells. The true stochasticity of the switching events has successfully been checked by means of the benchmarks proposed in the NIST statistical test suite.

Albeit the analysis has been based on a relatively small sample, the method proposed here for exploiting amorphous phase-change memory arrays to implement a True Random Number Generator seems promising; it points out useful applications of this class of devices to fields different from data storage like, e.g., cryptographic applications.

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