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Investigation of trapping/detrapping mechanisms in Al_2O_3 electron/hole traps and their influence on TANOS memory operations

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Alumina is a key material for developing innovative Charge-Trapping Non-Volatile Memory (CT-NVM) devices. Al_2O_3 is used to implement the top dielectric in TANOS devices [1], and it has been proposed as trapping layer [2] and to engineer the tunnel dielectric [3]. Despite the large use of this material, the quantitative investigation of defect features still lacks. *In this scenario, the purpose of this work is to investigate the physics of electron/hole trapping/detrapping mechanisms in Al_2O_3. Combining I-V and C-V measurements with a physical model we derive the energy levels of electron/hole traps and the location of electron/hole charge. The influence of electron/hole alumina traps on TANOS operations and reliability is investigated.*

We developed a combined I-V and C-V measurement scheme: 1) C-V on fresh device; 2) I-V measure performed applying a gate voltage V_G ramp (0.1V/s) from 0 to $V_{G,MAX}$; 3) C-V; 4) I-V varying Vg from $V_{G,MAX}$ to $V_{G,MIN}$; 5) C-V; 6) I-V varying V_G from $V_{G,MIN}$ to 0. $V_{G,MAX}$ and $V_{G,MIN}$ are selected to limit the maximum current density to ~100 mA/cm^2 in order to prevent the dielectric breakdown. Devices used are large area (~9.18E-3 cm^2) n-MOS capacitors with $TiN/Al_2O_3/SiO_2/Si$ stack, manufactured using standard process. Alumina thicknesses are t_{Al}=5, 10 and 15nm, with a thin (~1 nm) interfacial SiO_x layer at the Si interface. Thicknesses and relative dielectric constants of interfacial SiO_x (k_{SiOx}=5 [5]) and Al_2O_3 (k_{Al2O3}=9.15) layers are extracted from C-V measurements. Fig. 1 shows C-V curves measured on samples with t_{Al}=15nm. Simulations performed using the model in [6] reproduce accurately the measurements. For virgin devices, we assumed a fixed electron charge density ~10^{12} e/cm^2 at the SiO_x/Al_2O_3 interface, attributed to the process. Fig. 2 shows I-V curves measured on the t_{Al}=15nm capacitor. I-V characteristics show a significant hysteresis especially at positive V_G, indicating that electron trapping occurs during the V_G=0-16V ramp. This is confirmed also by the C-V curve measured after the V_G=0-16V ramp, showing a positive shift of the flat-band voltage ΔV_{FB}=1.6V. Negligible hysteresis is observed at negative V_G, whereas C-V curves measured after the negative V_G ramp shows a significant ΔV_{FB}=-1.6V, indicating a large hole trapping in the SiO_x/Al_2O_3 stack. Despite the same $|\Delta V_{FB}|$ after positive and negative V_G ramps, the larger I-V curve hysteresis observed with V_G>0 indicates that electron traps are much slower than hole ones. This result is not affected by the relative sequence of positive and negative I-V. We repeated the same experiment on devices with t_{Al}=10 nm. Again, we found that I-V hysteresis is significant especially for positive V_G. C-V curves measured after negative V_G ramp shows a negative ΔV_{FB}=-076V, confirming that hole trapping is significant. We investigated also samples with t_{Al}=5nm, observing neither I-V hysteresis nor flat band voltage shift after both positive and negative V_G ramp. This indicates that electron and hole trapping is negligible for t_{Al} thinner than 5 nm. V_{FB} shifts after positive and negative V_G ramps are plotted versus t_{Al} in the inset of Fig. 1. The ΔV_{FB} reduction with decreasing t_{Al} is due to the lower electron/hole charge trapped within the Al_2O_3 stack. Since ΔV_{FB} is negligible for the t_{Al}=5nm capacitors, we conclude that the charge trapping at the SiO_x/Al_2O_3 interface is not dominant. The charge is thus expected to be distributed across the Al_2O_3 volume.

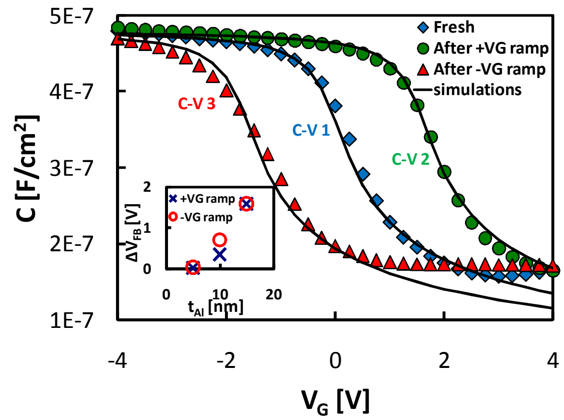

FIGURE 1. C-V CURVES SIMULATED (SOLID LINES) AND MEASURED ON FRESH DEVICE (CIRCLES), AFTER VG RAMP FROM 0V TO VG,MAX (TRIANGLES), AFTER VG RAMP FROM VG,MAX TO VG,MIN (SQUARE). THE INSET SHOWS THE ΔV_{FB} MEASURED AFTER POSITIVE AND NEGATIVE VG RAMPS FOR DIFFERENT ALUMINA THICKNESSESES.

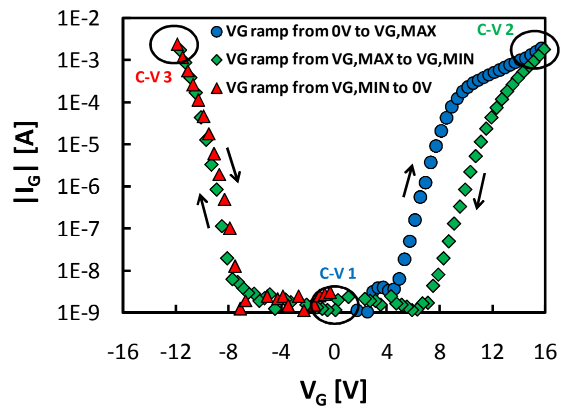

FIGURE 2. I-V CURVES MEASURED ON T_{AL}=15NM CAPACITORS.

To derive the energy distribution of electron/hole traps we performed retention experiments after positive and negative V_G ramps. ΔV_{FB} curves measured during retention experiments at different temperatures are shown in Fig. 3. The temperature does not affect ΔV_{FB} in retention, see empty symbols, suggesting that charge detrapping is mainly due to tunneling emission rather than thermally activated mechanisms. We use the model in [7] to reproduce the experimental data and to calculate the energy levels for defects. The time evolution of the trapped electron/hole charge is determined by solving self-consistently current continuity and Poisson equations including drift and diffusion mechanisms. Tunneling currents through bottom oxide and alumina blocking layers include direct/FN/modified tunneling contributions, Trap-to-Band Tunneling (TBT) and Trap-Assisted-Tunneling (TAT). Trapping is described according the SRH theory, while detrapping accounts for thermal emission (TE) and TBT contributions. ΔV_{FB} simulations in Fig. 3 performed considering unbiased samples agree very accurately with measurements. Noticeably, a unique set of trap parameters is

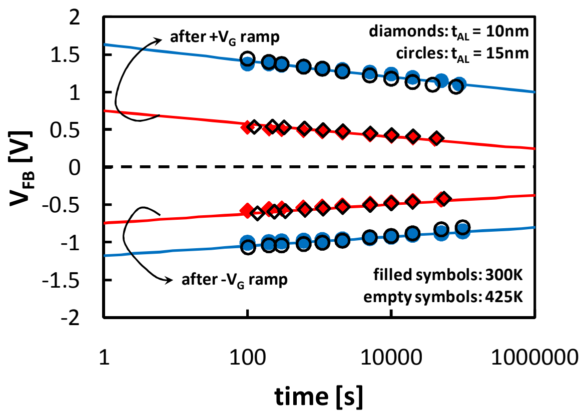

FIGURE 3. IV CURVES MEASURED (SYMBOLS) AND SIMULATED (SOLID LINES) USING THE MODEL IN [2] ON DEVICES WITH T_{AL}=15NM AND T_{AL}=10NM AFTER POSITIVE (ΔV_{FB}>0) AND NEGATIVE (ΔV_{FB}<0) V_G RAMPS.

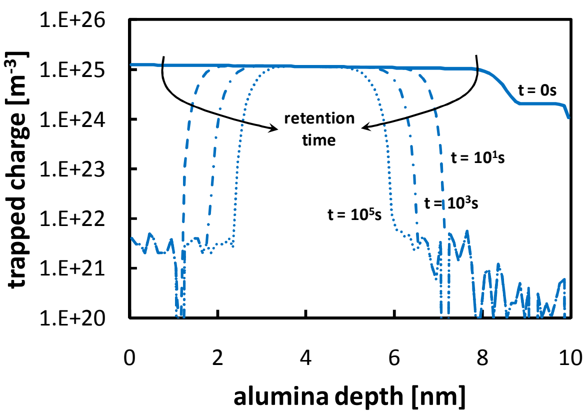

FIGURE 4. ELECTRON CHARGE EVOLUTION DERIVED FROM RETENTION SIMULATIONS ON DEVICES WITH 10 NM THICK ALUMINA.

considered independently of t_{AL}. The energy levels for electrons are deeper (E_T=2.0-2.6 eV) than hole ones (E_T=1.6-2.2eV), demonstrating that electron detrapping is slower due to the higher tunneling barrier of trapped electrons. Simulations allow deriving also the location of electron and hole charge inside the Al_2O_3 and its evolution over time in retention, see Fig. 4. As expected, electrons trapped close to the Al_2O_3 interfaces escape immediately, explaining the lower charge found in thinner Al_2O_3 capacitors, i.e. trends of retention and I-V hysteresis measurements.

Charge trapping in Al_2O_3 layer affects TANOS memory operation and reliability, contributing significantly to the V_{FB} shifts in both retention and P conditions. Using the model in [7], we reproduce accurately ΔV_{FB} evolution during program in TANOS devices, see Fig. 5. The charge distribution calculated after program shows a significant electron trapping in the alumina, see Fig. 6. This is also confirmed by the V_{FB} shift observed in retention conditions, performed applying a large gate voltage V_G=6V to accelerate the charge loss, see Fig. 7. The ΔV_{FB} curve shows a double slope over time well reproduced by simulations, related to the presence of electrons trapped in the alumina layer. Thanks to the much higher tunneling probability, electrons in alumina traps escape much faster compared to electrons in the nitride, determining the double-slope V_T curve. This behavior cannot be reproduced by simulations without considering electron trapping in Al_2O_3, see dashed line, and is more and more evident with increasing V_G. Simulations show that electron trapping in the alumina can contribute up to the 15% of the total V_{FB} shift.

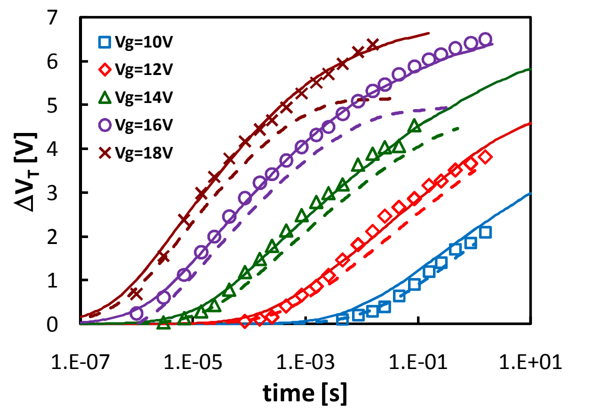

FIGURE 5. I-V CURVES MEASURED (SYMBOLS) ON TANOS CAPACITORS WITH 15NM/4NM/4.5NM ALUMINA/NITRIDE/OXIDE THICKNESSES. SIMULATIONS ARE PERFORMED TAKING INTO ACCOUNT (SOLID LINES) AND NEGLECTING (DASHED LINES) CHARGE TRAPPING INTO THE ALLUMINA LAYER.

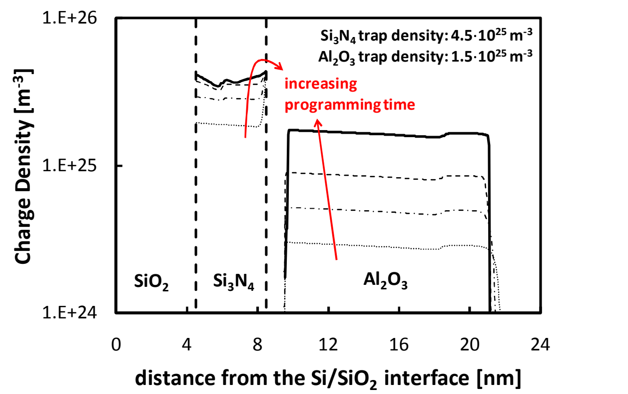

FIGURE 6. ELECTRON CHARGE DISTRIBUTION DERIVED FROM PROGRAM SIMULATIONS PERFROMED WITH THE MODEL IN [2] CONSIDERING A TANOS STACK WITH 4.5/4/15 NM OXIDE/NITRIDE/ALUMINA.

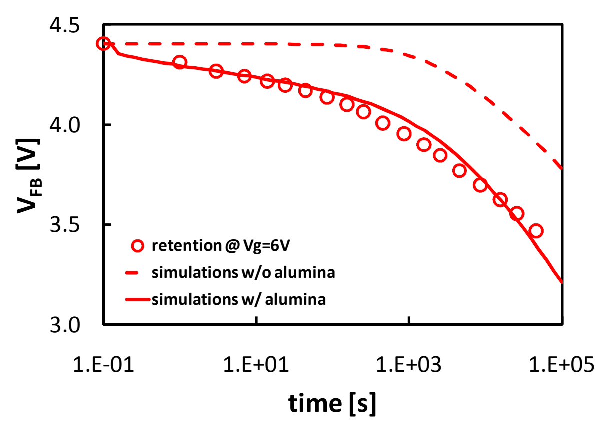

FIGURE 7. ΔV_{FB} MEASURED (SYMBOLS) AND SIMULATED TAKING INTO ACOUNT (SOLID LINES) AND NEGLECTING (DASHED LINES) ELECTRON TRAPPING IN THE ALLUMINA LAYER IN RETENTION CONDITIONS APPLYING V_G=6V TO ACCELLERATE THE CHARGE LOSS.

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