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Article

Reliability Investigation of GaN HEMTs for MMICs Applications

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Abstract: Results obtained during the evaluation of radio frequency (RF) reliability carried out on several devices fabricated with different epi-structure and field-plate geometries will be presented and discussed. Devices without a field-plate structure experienced a more severe degradation when compared to their counterparts while no significant correlation has been observed with respect of the different epi-structure tested. RF stress induced two main changes in the device electrical characteristics, *i.e.*, an increase in drain current dispersion and a reduction in gate-leakage currents. Both of these phenomena can be explained by assuming a density increase of an acceptor trap located beneath the gate contact and in the device barrier layer. Numerical simulations carried out with the aim of supporting the proposed mechanism will also be presented.

Keywords: GaN HEMT (High Electron Mobility Transistors); reliability; RF stress; degradation mechanism

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1. Introduction

GaN-based High Electron Mobility Transistors (HEMTs) are experiencing a rapid development and are proving to be excellent candidates for power applications [1,2]. Reliability issues are, however, still

limiting the use of their full capabilities [3], which are significantly greater of the currently available competing solid-state devices such as Silicon LDMOS and GaAs HEMTs [1].

In this paper, the authors would like to present an experimental evaluation of RF degradation carried out on several devices with either epi-structure variation and/or different field-plate structures introduced in order to both improve device performances and relax the electric field which builds up within the device active region [4,5].

The devices tested did not show a clear correlation between their stability during the RF stress test and their epi-structure. On the other hand, the introduction of the field-plate structure greatly improved both their performances and reliability suggesting that the high-electric fields within the device are the main cause of the observed degradation. Said degradation also induced a significant variation only in device dynamic performances, *i.e.*, an increase in device drain current dispersion, and in gate leakage currents, which decreased after the applied RF stress. Other DC parameters such as saturated drain current, device threshold voltage and peak transconductance remained fairly unchanged.

The paper will thus be organized as follows: after a brief description reported in Section 2 of the device used in this work, details on the experimental procedure used for carrying out the presented RF stress test will then be presented in Section 3. RF stress test results will then be reported on in Section 4, where also the main changes in device electrical characteristics before and after the applied RF stress will be highlighted. In Section 5, experimental data obtained in this work will be compared to previously published work carried out on GaN HEMT. Numerical simulations will also be carried out in order to support the proposed main degradation mechanisms, which we speculate are related to the increase in trap density of an acceptor trap located beneath the gate contact within the device barrier layer. Conclusions will then follow in Section 6.

2. Device Description

The devices tested in this work are all SiN passivated GaN HEMTs on SiC substrate fabricated by SELEX E.S. (Roma, Italy) with $L_G = 0.5$ μm, $L_{GS} = 1.25$ μm and $L_{GD} = 2.25$ μm. Field-plate terminals are present on some of the tested devices while the total gate periphery was 4 μm × 75 μm for all of them. Concerning the field-plate structure three different options were available, not on all wafers, namely a no-field plate structure (FP0), and two different field-plate structures FP1 and FP2 with gate connected field-plate extensions $L_{FP2} > L_{FP1}$. Significant epi-structure parameters for all the wafers tested are summarized in Table 1.

3. RF Stress Procedure Description

Devices fabricated on the different wafers previously described in Section 2 have been subjected to a 24 h RF stress test following a two steps procedure that will now be summarized. A first step concerns a load-pull characterization on a fresh device in order to figure out optimal matching condition, while the second step involves a 24 h RF stress test carried out on other fresh devices from the same process using a load matching point chosen as a compromise between maximum output power and power added efficiency (PAE).

Table 1. Main epi-structure parameters of the wafers tested.

WAFER	Barrier thickness (nm)	Aluminum concentration (%)	Buffer Doping	Buffer thickness (µm)
A	20	25	Fe-doped	1.9
B	22	25	Fe-doepd	1.9
C	24	22.4	Undoped	1.8
D	25	24	Undoped	1.8
E	20	25	Fe-doped	1.8
F	21	24	Fe-doped	1.9
G	24	25	C-doped	1.8

3.1. Load-Pull Characterization

A fresh device for each of the available processes has been characterized by means of (direct current) DC *I-V* measurements in order to extract the I_{DSS} current level (defined as the drain current at V_{GS} = 0 V and V_{DS} = 5 V) and then biased at V_{DS} = 30 V and at a 30% of I_{DSS} drain current level. At this point, a load-pull measurements sequence is applied to the device in order to obtain the load-pull contour plot of output power, small-signal gain, and input reflection coefficient and peak power added efficiency. For each load-pull point, a power sweep is carried out starting from the linear operating region up to the compression region until the device experiences a 6 dB gain compression. Load-pull characterization was carried out by maintaining the source matching at $\Gamma_S = 0 < 0°$. Γ_L points that yielded input reflection coefficient Γ_{IN} higher than 0.94 were avoided in order to reduce the risk of oscillation issues both during load-pull and the subsequent RF stress tests. A typical result of load-pull characterization carried out on a device from wafer B with an FP2 field-plate structure is depicted in Figure 1.

3.2. 24 h RF Stress Test

After load-pull characterization, a 24 h RF stress test was performed on fresh devices for each of the wafers described in the previous section. Particularly, the following measurement steps have been performed for each device:

1. 200 ns Double-pulse IV pre-stress characterization at the V_{Gbl} = 0 V, V_{Dbl} = 0 V and V_{Gbl} = −6 V, V_{Dbl} = 25 V baselines in order to evaluate drain current dispersion phenomena before the applied RF stress.
2. DC IV pre-stress characterization carried out in order to extract device saturation current at V_{DS} = 5 V, peak trasconductance (g_m) at V_{DS} = 5 V, gate leakage current at V_{GS} = −6 V, V_{DS} = 5 V and device threshold voltage V_{TH} defined at 1 mA·mm^{-1} with V_{DS} = 5 V.
3. RF power sweep carried out with a 2.5 GHz continous wave (CW) signal, base-plate temperature of 40 °C, V_{DS} = 30 V and I_D = 30% of I_{DSS} by using matching condition determined during load-pull measurements.
4. Selection of RF input drive level needed to drive the device into its 6 dB gain compression point.

5. 24 h RF stress test carried out with a 2.5 GHz CW signal, base-plate temperature of 40 °C, V_{DS} = 30 V and I_D = 30% of I_{DSS} by using matching condition determined during load-pull measurements driving the device into its 6 dB gain compression point.
6. 200 ns Double-pulse *I-V* post-stress characterization at the V_{Gbl} = 0 V, V_{Dbl} = 0 V and V_{Gbl} = −6 V, V_{Dbl} = 25 V baselines in order to evaluate drain current dispersion phenomena after the applied RF stress.
7. DC *I-V* post-stress characterization carried out in order to extract device saturation current at V_{DS} = 5 V, peak g_m at V_{DS} = 5 V, gate leakage current at V_{GS} = −6 V, V_{DS} = 5 V and device threshold voltage V_{TH} defined at 1 mA·mm^{-1} with V_{DS} = 5 V.

A typical results showing the degradation of the RF output power level during the applied RF stress is depicted in Figure 2. Particularly it can be seen how devices from the same wafer B are experiencing a lower degradation when field-plate length is increased from FP0 (no field-plate) to FP2 (longest available field-plate geometry).

Figure 1. Typical Load-pull contour plots obtained on a device from wafer B with an FP2 field-plate structure. Device is biased at V_{DS} = 30 V and at a 30% of I_{DSS} drain current level and driven with a 2.5 GHz CW signal.

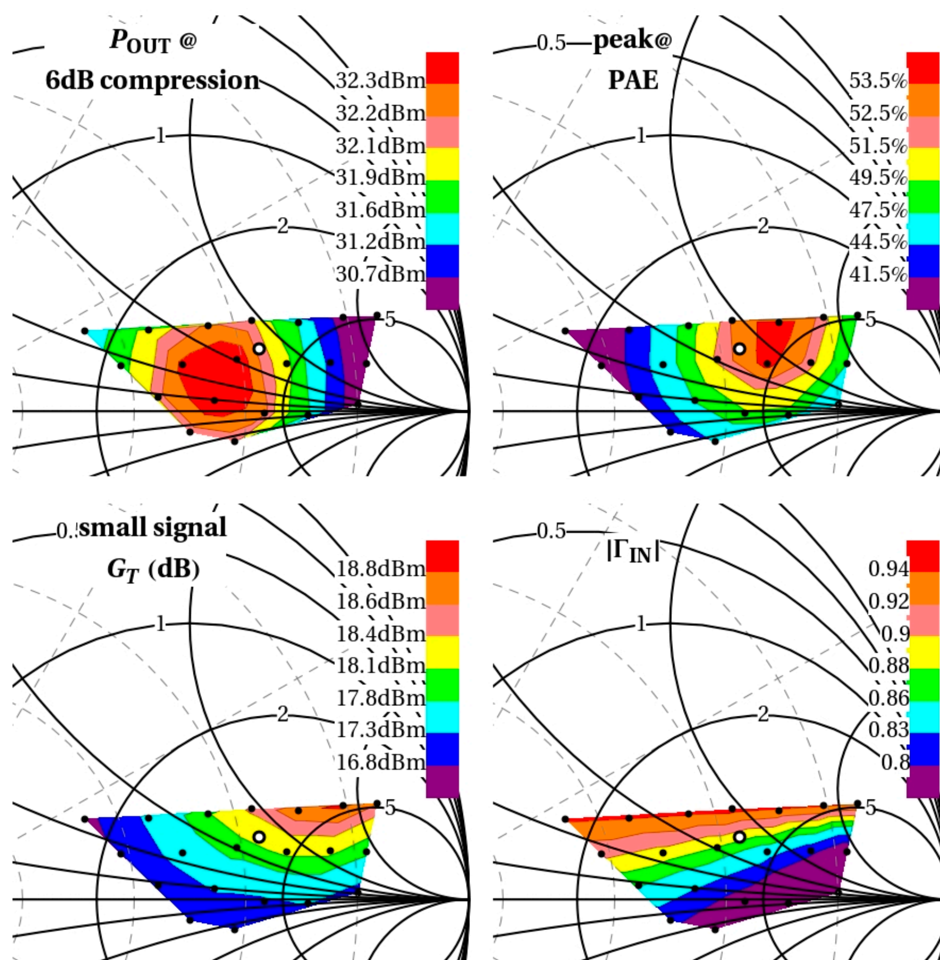
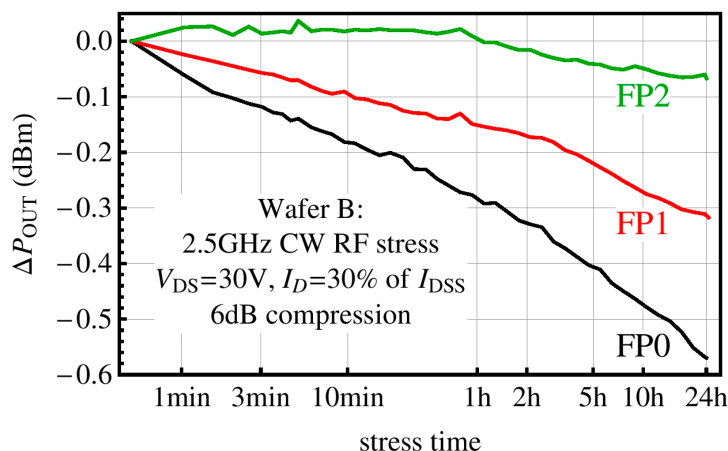


Figure 2. Output power variation during the 24 h RF stress test carried out on devices from wafer B with different field-plate geometries. Devices are biased at V_{DS} = 30 V and 30% of I_{DSS}. They are all driven at their 6 dB compression point by means of a 2.5 GHz CW signal. Base-plate temperature is maintained constant at 40 °C.



4. RF Stress Test Results

Results obtained during the RF stress campaign will now be summarized and the pre-stress post-stress variations of the DC and dispersion parameters observed in the different device tested will also be shown. Figure 3 shows the output power variation experienced during the 24 h stress test *vs*. the operating output power level. At first, it can be clearly seen when comparing devices from wafer A, B and D that the introduction of the field-plate both improves device reliability, lower output power variation, and device output power operating levels [6,7]. As an example, devices A0, *i.e.*, from wafer A and FP0 structure, experienced a −0.55 dBm variation when operated at a 2.8 W·mm^{-1} while power variations and operating level were −0.3 dBm and 3.5 W·mm^{-1} for devices A1 and −0.05 dBm and 5.5 W·mm^{-1} for devices A2. Another interesting result can also be speculated by the fact that higher operating power levels (*i.e.*, larger junction temperatures) does not seems to implicate larger device degradation. We can thus speculate that, at least for the devices tested in this work and for the operating conditions used, thermal effects does not seem to be the primary cause of the observed degradation. On the other hand, the clear variation observed by increasing the field-plate length suggests that the degradation occurring during RF operation is likely to be related to the high electric fields within the device structure.

Device parameters variation before and after the applied RF stress test will now be presented: Figure 4A shows the variation in the DC saturated drain current level at V_{DS} = 5 V, V_{GS} = 0 V *vs.* the output power variation. Although most devices exhibited a small decrease (below 10%) in the I_{DSS} value, said decrease does not seem to be somehow correlated with the amount of output power degradation. A similar observation can also be made when comparing the variation in the DC peak transconductance level measured at V_{DS} = 5 V. As can be seen in Figure 4B peak-transconductance variation is within 5% and again said decrease does not seems to be somehow correlated with the amount of output power degradation. Threshold voltage variation, not shown, again was not very significant (within ±0.2 V variation) and again did not showed a particular trend when analyzed *versus* the output power variation.

Figure 3. Output power variation at the end of the 24 h RF stress test *vs.* output power level reached by the device at the beginning of the stress. Devices are biased at V_{DS} = 30 V and 30% of I_{DSS}. They are all driven at their 6 dB compression point by means of a 2.5 GHz CW signal. Base-plate temperature is maintained constant at 40 °C. Introducing a field-plate structure and increasing its length greatly improves both device performance and reliability.

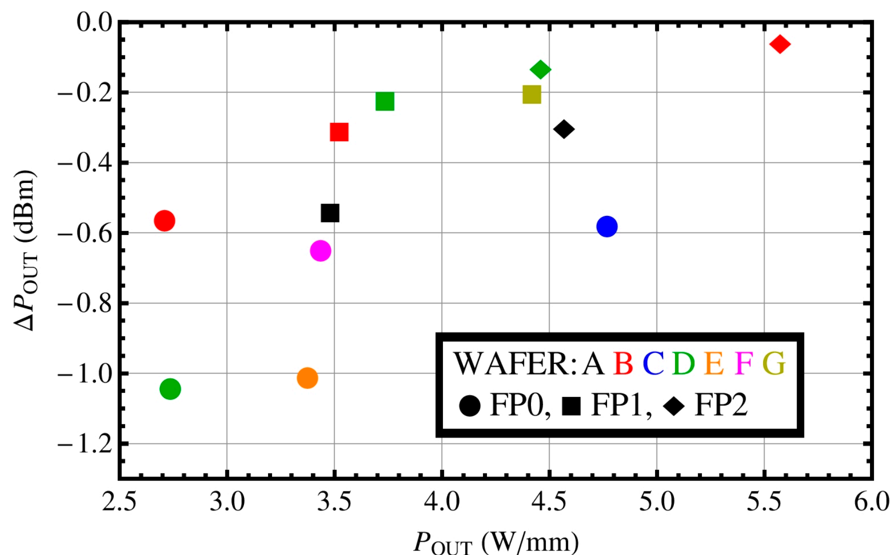
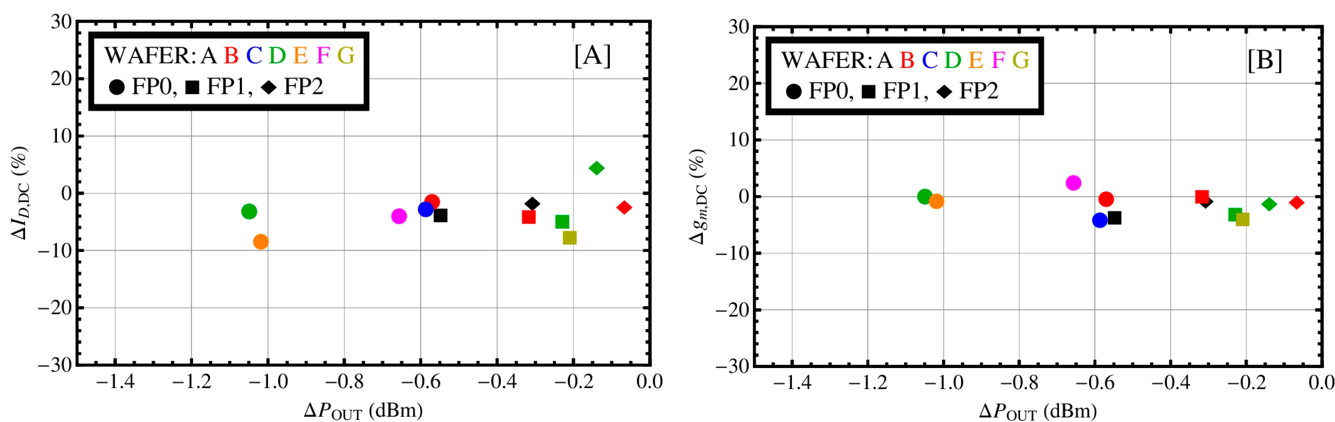
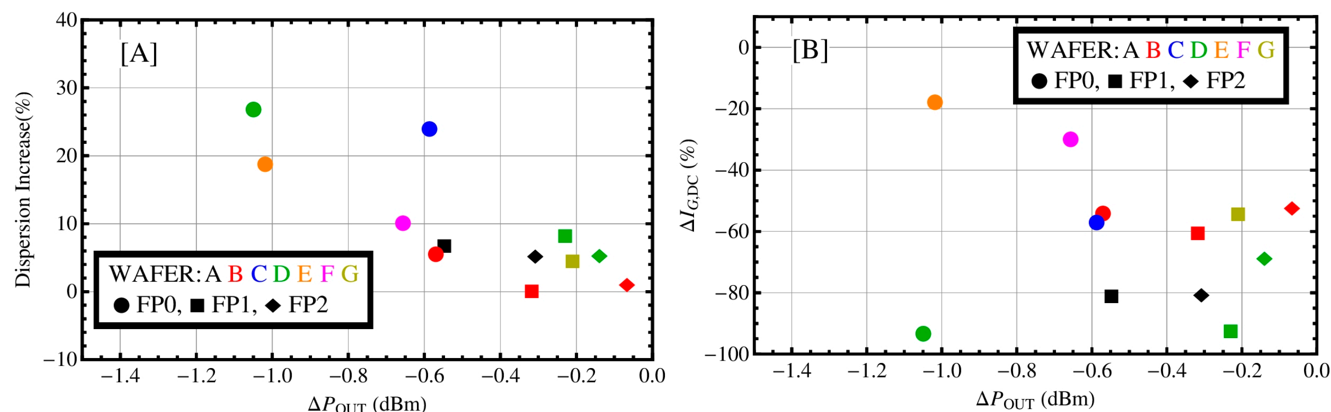


Figure 4. I_{DSS} (**A**) and peak g_m (**B**) variations *vs.* output power variation at the end of the 24 h RF stress test.



A clear correlation was instead observed between the variation in drain current dispersion and the output power variation. Particularly drain current dispersion was evaluated as $(I_D - I_{Dpul})/I_D$ where I_D represents the drain current level at V_{GS} = 1 V and V_{DS} = 3 V measured when pulsing from the V_{Gbl} = 0 V and V_{Dbl} = 0 V baseline, while I_{Dpul} represents the drain current level at V_{GS} = 1 V and V_{DS} = 3 V measured when pulsing from the V_{Gbl} = −6 V and V_{Dbl} = 25 V baseline. As can be seen in Figure 5A a clear trend is observed between the increase in drain current dispersion, *i.e.*, the difference in the dispersion coefficient after and before the RF stress, and the device experienced output power decrease during the RF stress. At the increasing of the output power variation an increase in device current dispersion is observed.

Figure 5. Drain current dispersion (**A**) and reverse gate current (**B**) variations *vs.* output power variation at the end of the 24 h RF stress test.



Finally, a strong variation in the gate reverse current measured at $V_{GS} = -6$ V and $V_{DS} = 5$ V was also observed on the entire tested device. As can be seen in Figure 5B gate-leakage reduction in tested devices was higher than 20% with some devices experiencing reductions up to 94%, *i.e.*, more than an order of magnitude decrease. Although this decrease was not clearly related with the output power variation experienced by the device during the RF stress, we can however confirm that the device degradation occurring during the RF stress strongly affects the gate-leakage current levels on all tested devices, and that more than one-order of magnitude decrease has been observed in some devices.

We can now summarize the main results presented in this section:

1. Introducing a field-plate structure and increasing its length allow for improvement in both device performance and reliability.
2. Operating power level does not seem to directly affect the device stability during the RF stress, at least for the power levels reached in this work.
3. Drain current dispersion increase experienced by the device after the stress well correlates with the decrease in output power variation.
4. Concerning DC parameters, only the gate-leakage current levels are showing a significant variation after the applied RF stress test.

5. RF Stress Results Discussion and 2D Numerical Simulations

As summarized in the previous section, the main variation observed in device parameters after the RF stress tests have been an increase in device current dispersion and a lowering in the gate-leakage currents. Similar results have also been obtained by other authors carrying out either DC or RF stress tests on GaN HEMTs.

Hayashi *et al.* [8] reported a significant decrease in gate leakage current after applying a 30 min on-state stress on AlGaN/GaN HEMT. On the other hand, the changes in the other electrical characteristics were small. The saturated drain current (I_{DSS}) changed only from 452 to 442 mA·mm^{-1}, and the threshold voltage (V_{TH}) changes from −2.59 to −2.65 V.

Dammann and coworkers [9] also observed a reduction in gate-current levels when applying an on-state DC Stress test at V_{DS} = 30 V, T_{ch} = 260 °C, I_{DS} = 150 mA·mm^{-1} on 0.25 μm gate-length GaN HEMT devices on SiC substrate.

Medjdoub *et al.* [10] reported again a reduction of gate current during on-state stress carried out on GaN HEMT on Silicon substrate biased at V_{DS} = 50 V and at a power dissipation level of 2.5 W·mm^{-1}. No significant degradation of DC drain current or transconductance parameters was observed, while a slight increase in device drain current dispersion under pulsed condition was reported.

Chini *et al.* [6] reported a gate current decrease during RF stress test carried out on GaN HEMT on Silicon substrate, and associated the device experienced degradation to the increase in trap density of a pre-existing electron trap located below the gate contact within the AlGaN device barrier. In [6] it was also reported that RF degradation was also related to an increase in device drain current dispersion.

All these results are very similar to those presented in this paper. Particularly the correlation found between RF degradation and increase in trap density below the gate contact [6] suggest that, at least for the device presented in this work and for those reported in [6] an increase in electron trap density in the AlGaN barrier might be the main degradation mechanisms causing the RF output power drop observed.

Numerical simulations have then been carried out in order to gain insights in the physical mechanisms associated with the increase of an acceptor trap located beneath the gate contact in the AlGaN barrier. A 20 nm barrier with 25% Al-concentration GaN HEMT was simulated by introducing an acceptor trap level at 0.75 eV from the conduction band [6] within the first 5 nm of the AlGaN barrier beneath the gate contact with a constant trap density n_t. Traps concentration n_t was then varied from 1×10^{19} to 8×10^{19} cm^{-3} concentration and DC, pulsed *I-V* and drain current transient measurements were simulated. The simulated device has a 0.5 μm gate-length, 1.5 μm and 2.5 μm gate-source and gate-drain spacing respectively. Field-plate structure was not introduced.

First, we are going to show the simulation results obtained, and then a detailed discussion will follow. As can be seen in Figure 6, where the I_D and g_m *vs.* V_{GS} characteristics at V_{DS} = 5 V are depicted, varying the n_t concentration does not induce any sensible variation in the DC parameters evaluated. On the other hand, as reported in Figure 7 where the I_G *vs.* V_{GS} characteristics at V_{DS} = 5 V are depicted, increasing the acceptor trap concentration n_t induces a sensible reduction in the gate current levels of more than one order of magnitude.

Drain current transient obtained by pulsing the gate and drain terminal from V_{GS} = −8 V, V_{DS} = 50 V (*i.e.*, off-state high drain voltage condition) to V_{GS} = 1 V, V_{DS} = 5 V (*i.e.*, on-state low drain voltage condition) are reported in Figure 8. Simulations showed how the increase in n_t yielded an increase in the drain current dispersion which was in the order of 1% for 1×10^{19} cm^{-3} trap concentration and increased up to 16% when n_t was settled equal to 8×10^{19} cm^{-3}. We can thus speculate that increasing the barrier trap density n_t allows us to reproduce the two main parameters variations, decrease in gate leakage current and increase in drain current dispersion, observed at the end of the carried out RF stresses. Moreover, other parameters such as saturated drain current level and peak transconductance are insensitive at the increasing of n_t, which again is in good agreement to what observed experimentally. Pulsed *I-V* characteristics obtained from the V_{GS} = −8 V and V_{DS} = 50 V baseline while varying n_t were also simulated. Results depicted in Figure 9, clearly shows the increase in drain current dispersion at the increasing of the acceptor trap concentration n_t.

Figure 6. Simulated I_D *vs.* V_{GS} and g_m *vs.* V_{GS} characteristics at V_{DS} = 5 V for different acceptor trap densities n_t. No significant change is observed in the simulated characteristics when varying the acceptor trap concentration within the 1 × 10^{19} to 8 × 10^{19} cm^{-3} range.

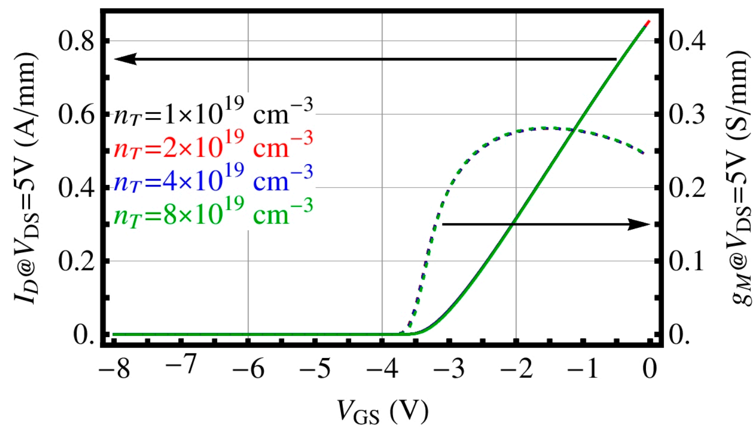


Figure 7. Simulated I_G *vs.* V_{GS} characteristics at V_{DS} = 5 V for different acceptor trap densities n_t. The increase in trap density n_t induces a decrease in device gate leakage currents.

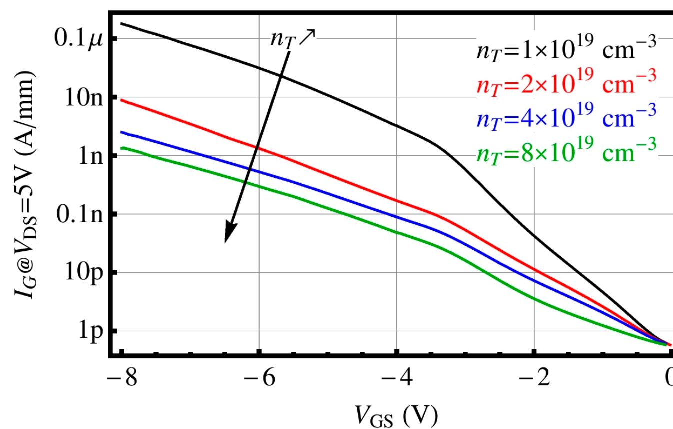


Figure 8. Simulated drain current transients for different acceptor trap densities n_t. Device terminal are pulsed from V_{GS} = −8 V, V_{DS} = 50 V (*i.e.*, off-state high drain voltage condition) to V_{GS} = 1 V, V_{DS} = 5 V (*i.e.*, on-state low drain voltage condition). The increase in trap density n_t induces a larger drain current dispersion.

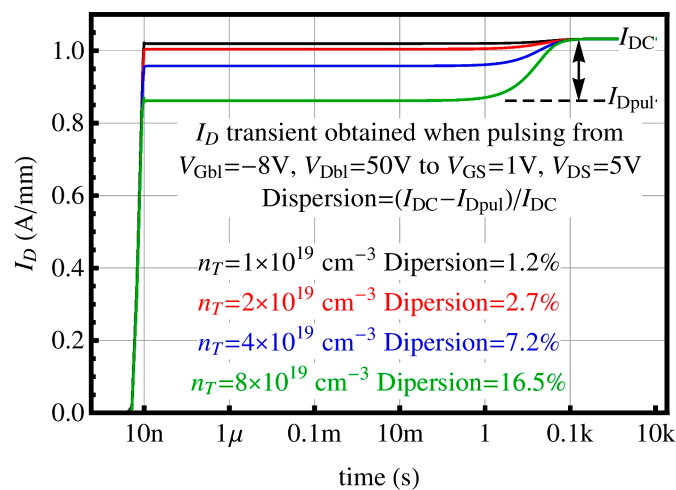
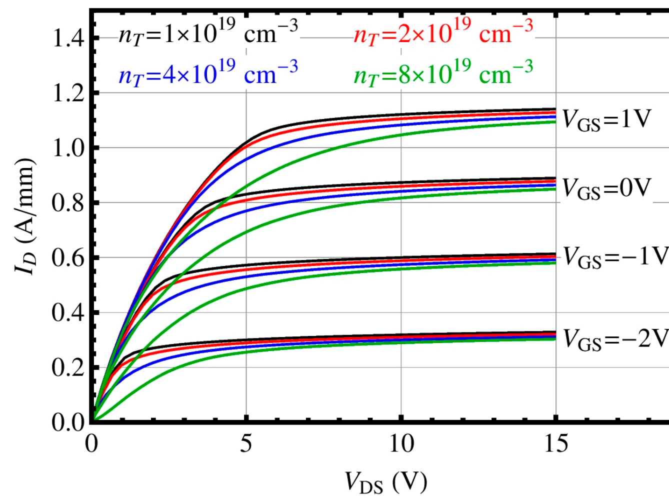


Figure 9. 200 ns simulated *I-V* characteristics for different acceptor trap densities n_t obtained from the V_{GS}= −8 V and V_{DS} = 50 V baseline. The increase in trap density n_t induces a larger drain current dispersion.



The effect of a barrier trap on the dynamic characteristics of a GaN HEMT is reported in details in [6]. Basically, electrons tunneling from the reverse-biased gate contact and traveling through the AlGaN barrier get trapped in the acceptor traps. Increasing the trap density and/or increasing the gate-reverse current by applying larger reverse biases on the gate junction yields an increase in the trapped electron concentration, which then limits the capability of the device to drive high current levels when it is pulsed to on-state low drain voltage conditions. This phenomena induces the observed drain current dispersion in the simulated drain current transient where the device recovers its steady-state operating level (I_{DC} see Figure 8) once all the excess trapped electrons are emitted. This effect can also be noticed when analyzing the simulated trapped electrons concentration within the AlGaN barrier at V_{GS} = −8 V and V_{DS} = 5 V extracted at the gate-edge towards the drain contact for n_t = 1 × 10^{19} cm^{-3} and 8 × 10^{19} cm^{-3}, see Figure 10. The presence of trapped electron is also modifying the electric field profile within the device barrier and beneath the gate contact. Particularly, as can be seen in Figure 11, increasing n_t causes an increase in the negative trapped charge which, by counteracting the positive piezo-electric charge located at the AlGaN/GaN barrier, reduces the electric-field at the gate junction when n_t is increased. Said reduction in the electric-field at the gate junction is thus responsible for the decrease in gate-leakage currents observed in Figure 8. As electrons are tunneling from the gate to the AlGaN barrier, they accumulate below the gate electrode within the acceptor traps. The negative charge that forms within the trap region is thus providing an electrostatic feedback [11] to the gate that works to suppress the gate current leakage.

We can thus conclude that the increase of an acceptor trap density spatially confined below the gate Schottky contact in the AlGaN barrier can qualitatively explain the degradation mechanism observed in the device presented. At the increase of the trap density n_t, device leakage currents are decreasing, and current dispersion is increasing while other DC parameters remains mainly unchanged.

Figure 10. Simulated trapped electrons profile at the gate-edge towards the drain contact for two different barrier trap densities n_t of 1 × 10^{19} and 8 × 10^{19} cm^{-3} when the device is biased at V_{GS} = −8 V and V_{DS} = 5 V.

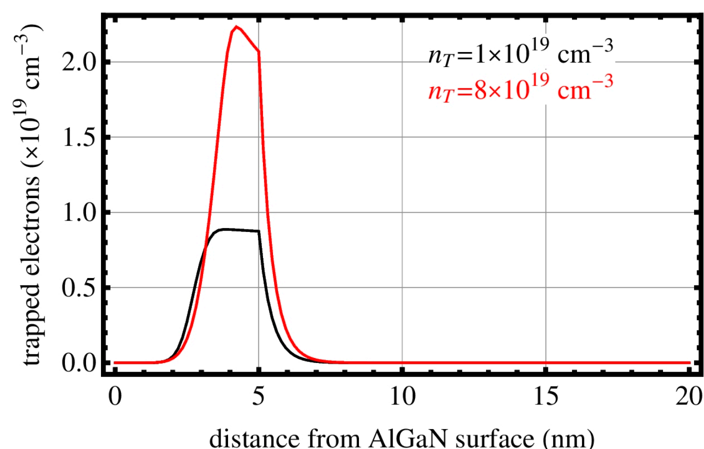
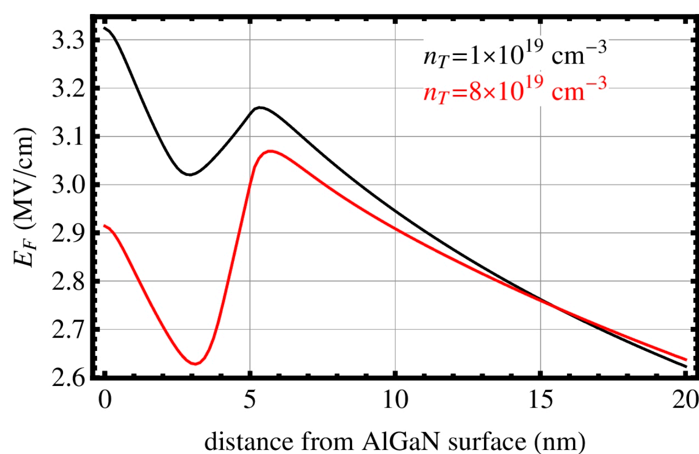


Figure 11. Simulated electric field profile at the gate-edge towards the drain contact for two different barrier trap densities n_t of 1 × 10^{19} and 8 × 10^{19} cm^{-3} when the device is biased at V_{GS} = −8 V and V_{DS} = 5 V. At the increasing of n_t an increase in trapped electrons (*i.e.*, negative charge) allows a reduction of the electric field beneath the gate Schottky contact thus reducing the gate leakage currents.



6. Conclusions

Results obtained by RF stress tests carried out on several devices from different wafer and with different field-plate geometries have been presented. No direct correlation between device epi-structure and RF degradation was observed. On the other hand, the introduction of the field-plate structure greatly improved both the devices performance as well as their reliability. The observed RF degradation has then been related to an increase in trap density below the gate contact in the AlGaN barrier. The proposed mechanism is able to predict the two main variations observed in stressed devices: an increase in the drain current dispersion with a consequent reduction in the device dynamic performances, and a reduction in the gate leakage currents. The proposed mechanism leaves also unaffected other typical DC parameters such as device saturated drain current levels, device threshold

voltage and peak transconductance which is also in agreement with the experimental results obtained by comparing the device characteristics before and after the applied RF stress test.

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Author Contributions

Alessandro Chini has defined the characterization procedure, carried out the measurements, numerical simulations, and participated to the results discussions. Gaudenzio Meneghesso has contributed to the definition of the characterization procedure and participated to the results discussions. Alessio Pantellini provided the samples and participated to the results discussions. Claudio Lanzieri provided the samples and participated to the results discussions. Enrico Zanoni has contributed to the definition of the characterization procedure and participated to the results discussions.

Conflicts of Interest

The authors declare no conflict of interests.

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