

Article

# Single-Phase Current Source Inverter with Reduced Ground Leakage Current for Photovoltaic Applications

Giovanni Migliazza <sup>1</sup>, Emilio Lorenzani <sup>1</sup>, Fabio Immovilli <sup>1</sup> and Giampaolo Buticchi <sup>2,\*</sup> 

<sup>1</sup> Department of Sciences and Method for Engineering, University of Modena and Reggio Emilia, 42122 Reggio Emilia, Italy; giovanni.migliazza@unimore.it (G.M.); emilio.lorenzani@unimore.it (E.L.); fabio.immovilli@unimore.it (F.I.)

<sup>2</sup> Zhejiang Key Laboratory on the More Electric Aircraft Technologies, University of Nottingham Ningbo China, Ningbo 315100, China

\* Correspondence: buticchi@ieee.org

Received: 31 August 2020; Accepted: 25 September 2020; Published: 2 October 2020



**Abstract:** Integrated power electronics for photovoltaic applications has attracted increasing interest, due to the possibility of having grid-connected photovoltaic modules with independent maximum power point tracking and high reliability. In this paper, a single-phase Current Source Inverter (CSI) is discussed for a photovoltaic application. The basic CSI topology will be explained for the sake of completeness, highlighting its main features and analyzing the ground leakage current problem, an important benchmark for photovoltaic application. A novel topology, called CSI5, is proposed in this work. The main feature is the presence of additional switches for ground leakage current reduction. The performance of the proposed topology is assessed by numerical simulation, and the experimental results confirm that this solution is able to strongly reduce the ground leakage current and conduction power losses.

**Keywords:** power electronics; current source inverter; photovoltaic power system

## 1. Introduction

Photovoltaic (PV) energy production has witnessed a steady increase in the past 15 years. The growth has been fueled by technological advancements and the support of incentive programs from the world's governments. Nowadays, the scenario for power electronics is well-established [1,2], and several possibilities are present for different power levels, ranging from (Megawatt) MW-scale centralized inverters (for very large solar arrays), to the medium-power solution (single and three-phase) to the micro-inverter type, also called a string inverter or module-integrated converter (MIC). They are usually single-phase converters which are directly connected to the grid. This latter type has been in the spotlight due to its unique advantages, including:

1. Individual Maximum Power Point Tracking (MPPT) is possible, where this allows for better extraction efficiency, preventing the partial shading phenomena.
2. High availability of the system, since the failure of a power electronics module would minimally impact the performance of a bigger system.
3. Since the module would have an AC output, the installation and protection system would be cheaper, due to the absence of a high-voltage DC distribution, as in some centralized inverter solutions.

An initial classification of the MICs has been proposed in [3]. One of the peculiar problems of the photovoltaic systems is the possibility of ground leakage current insurgence [1], due to the parasitic

capacitance between the photovoltaic cells and the ground and the electric distribution. The typical solutions imply a transformer (either high-frequency or low-frequency), but transformerless solutions normally feature better efficiency and lower weight. For years, the main topologies have been based on the Voltage Source Inverter paradigm, and modifications to the unidirectional full-bridge or to the three-phase bridge with additional switches were proposed to reduce the common mode voltage generation, which causes the ground leakage current [4–6]. Recently, the Z-source or quasi-Z-source [7] have been employed for MICs, due to the advantage of low ground leakage current and intrinsic boost capability.

This article critically analyses a modified Current Source Inverter topology, named CSI5, that is able to improve the performance of the basic single-phase CSI in terms of efficiency and is also capable of reducing the ground leakage current to almost zero. Recently, PV CSI architectures have been proposed for full-sized PV arrays, both in single-phase [8,9] and three-phase [10] architectures, but also for MIC solutions for three-phase distribution grids [11]. The CSI5 topology was proposed for the first time in [12], where the present work further expands the theoretical and simulation analysis, offering a comprehensive coverage of the benefits and drawbacks of single-phase CSI for PV applications, and in particular of the proposed solution. These improvements are analyzed in the following sections in order to verify the effectiveness of this power converter employed as a PV MIC. The contribution of this paper is a thorough analysis of the CSI5 topology with active decoupling devices, which clamp the output of the H-bridge stage during the zero states of the pulse width modulation, allowing for extremely low levels of ground leakage current.

## 2. Basic Single-Phase CSI Topology

Figure 1 shows the basic single-phase Current Source Inverter (CSI) for a photovoltaic grid connected system: it is worth noticing that the schematic features the equivalent parasitic capacitance,  $C_{PV}$ , of the PV string connected between the earth and the frame of the PV panels [13]; resistance  $R_G$  represents the ground resistance between the neutral connection and the earth. For simplicity's sake, only a lumped capacitor connected to the negative DC rail of the panels is considered, and it holds the overall capacitance of the panels. The capacitance connected to the positive rail of the panel (the panel not shown in Figure 1) is not drawn, because the capacitance of both DC rails are connected in parallel in the equivalent common-mode circuit. Since for the PV converter, the main source of capacitance to the ground is the panel parasitic one, the capacitance of the devices to the heatsink and then to the ground are not considered for this work.

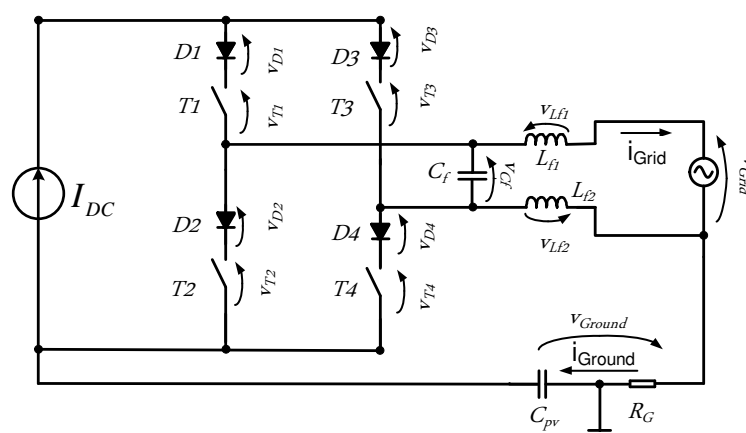


Figure 1. Basic single-phase CSI topology.

This topology, like all single-phase PV topologies, faces the drawback of matching a pulsating power to a constant power source. For the CSI, this is even more critical, since the energy would need to be stored in the DC inductor, which would imply unacceptable values in terms of weight and size.

This issue will be discussed later in the manuscript, and in this section the assumption of a constant DC current source will be made for the operating principle explanation.

### 2.1. CSI Operating Principle

The basic principle of the CSI is that a constant current source (for example, by employing an inductor) is modulated to synthesize an arbitrary current waveform at the output. To reduce distortion in the output current waveform, a filter comprising a capacitor, or a capacitor and an inductor, is placed to realize the coupling to the grid. In the case of a simple capacitive filter, the inductance of the grid would act as an inductive element to limit the high-frequency current harmonics injected into the grid. However, to prevent excessive voltage distortion at the point of common coupling (PCC), a physical inductor is preferred. The immediate advantages of this topology is the ease of current control (the current is directly controlled via the modulation index), the intrinsic voltage boost capabilities, the high reliability due to the low failure rate of the inductor if compared to an electrolytic capacitor, as well as the intrinsic short-circuit protection inherent of the topology.

On the other hand, the presence of two devices connected in series (the diode and the transistor) to realize a bi-directional voltage blocking device has a strong impact on the efficiency due to increased conduction losses, an aspect which has limited the widespread adoption of CSI topologies.

The command sequence of the four transistors in the unidirectional full-bridge (T1, T2, T3, and T4) is obtained with the strategy shown in Figure 2. Considering grid-tied operation, the sinusoidal waveform shown in Figure 2 represents the reference shape of the current, which can be extracted with a Phase-Locked Loop (PLL) or can be obtained from the grid voltage measurement.

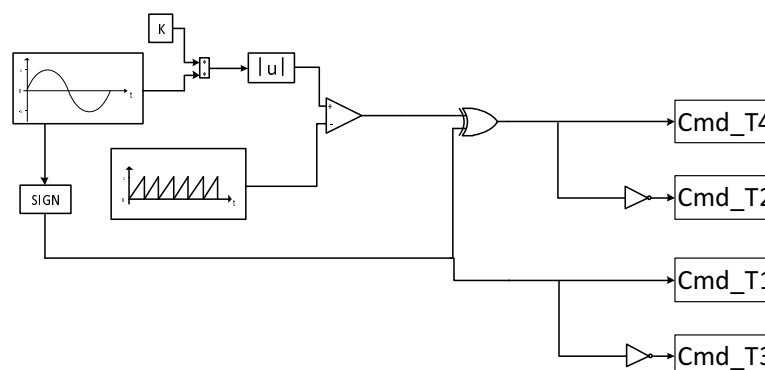


Figure 2. Basic single-phase CSI control. ©2016 IEEE [12].

The basic operation implies that for each grid-voltage half-wave, a diagonal of the H-bridge is switched on for a time, depending on the reference (active state), providing the DC-link current to the grid. During the remaining switching period, a shoot-through state (zero state) is applied to the H-bridge. In this latter case, zero current is provided to the grid [12].

Similarly to the dead-time that is applied between the switches of a VSI, an overlap time is introduced in the commutation of the CSI to prevent the DC-link open-circuit, as shown in Figure 3.

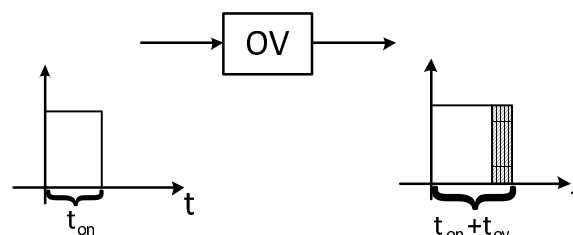
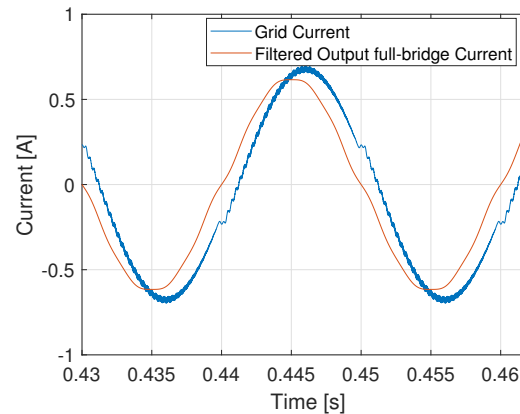


Figure 3. Overlap time insertion. ©2016 IEEE [12].

The result of the commutation process is shown in the exemplified condition of Figure 4, where the grid current and a zero-phase filtered version [14] of the bridge output current are shown. It can be seen that a small phase shift and amplitude difference exists, due to the current absorbed by the output filter. This effect can be compensated for by properly adjusting the reference to compensate for the current absorbed by the output C-L filter.



**Figure 4.** Comparison between the output full-bridge current, zero-phase filtered to remove the Pulse Width Modulation (PWM) components (orange) and an actual injected grid current (blue) in order to highlight the phase shift introduced by the output Capacitive-Inductive CL filter.

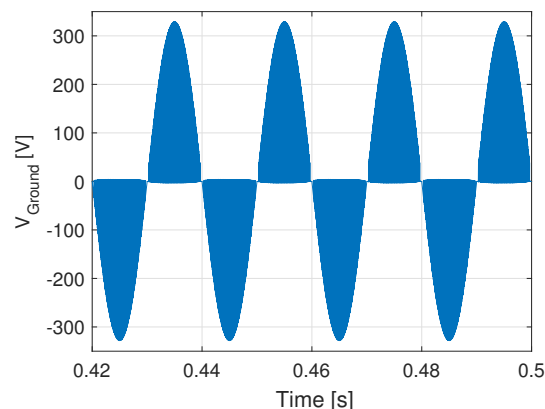
## 2.2. Common Mode Voltage Analysis for the CSI Topology

The theoretical tool used for the analysis of the ground leakage current in grid-connected Pulse Width Modulation (PWM) is usually the common mode voltage evaluation, as shown in the relevant literature for the VSI [15,16].

For the CSI application, due to the different operating principles, the analysis of the ground leakage current is performed with the evaluation of the ground voltage  $C_{ground}$ , that is, the voltage between the neutral conductor of the grid generator and the negative terminal of the DC power source.

Since the impedance of  $C_{pv}$  against high-frequency voltage components is very low, the high-frequency component of ground voltage has to be minimized. For simplicity's sake, the assumption of a unity power factor will be made.

Referring to Figure 1,  $V_{ground}$  is analytically computed in the case of positive and negative semi-periods of the grid voltage, respectively, during both Active and Zero states. Figure 5 shows a possible waveform of  $v_{ground}$  when the parasitic capacitor is neglected, since the ground voltage depends on the  $C_{pV}$  value, contrary to the VSI case [17].



**Figure 5.** Basic CSI topology  $v_{ground}$  waveform with zero  $C_{pV}$ .

It can be seen that the ground voltage envelope follows the same shape of the grid voltage with the additional high-frequency harmonic component due to the switching of the power electronics. This level of ground voltage is not acceptable for transformerless PV applications, and the following sections will explain the mitigation strategies, both for ground leakage current reduction and for efficiency improvement.

### 3. Proposed CSI5 Topology

In order to address the main drawback of the CSI topology, two main modifications were performed, which will be detailed in the following.

The first improvement was obtained by adding a switch to the basic CSI topology and obtaining the CSI5 converter, as shown in Figure 6. The additional power device ( $T_5$  and  $D_5$ ) was used to provide the zero state to the output [12], strongly reducing the conduction loss of the topology (where only two devices carry the current, instead of four). As a matter of fact, during overlap time, the input current always flows through  $T_5$  and  $D_5$  instead of one leg of the full-bridge. This way, all commutations of the full-bridge switches are zero-current commutations (ZCS). This results in all the commutations of  $T_5$  being hard-switching, but the switching power losses are also concentrated only on this device. In order to maximize the converter efficiency,  $T_5$  should be chosen with different criteria than the other transistors—for example, a SiC device would be preferred, but this would come at the price of additional cost. The control for the additional switch  $T_5$  is shown in Figure 7. The efficiency improvement consequent to the addition of the zero-state switch has been addressed in previous works by the authors [18].

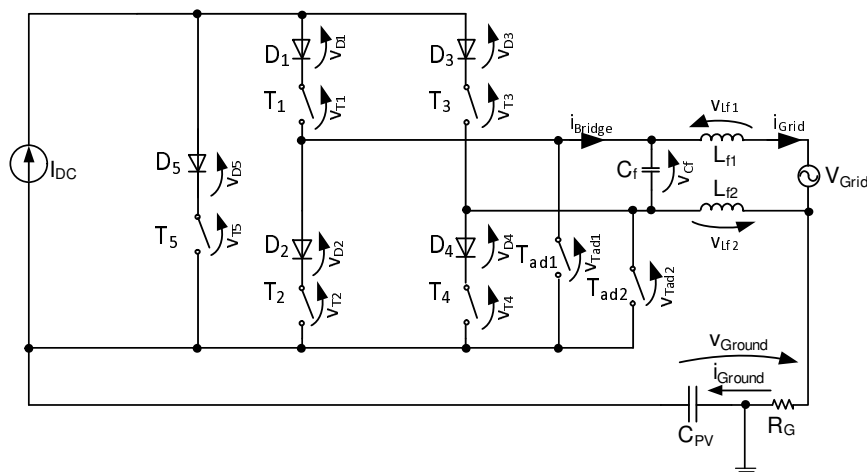


Figure 6. CSI5 topology with active clamp.

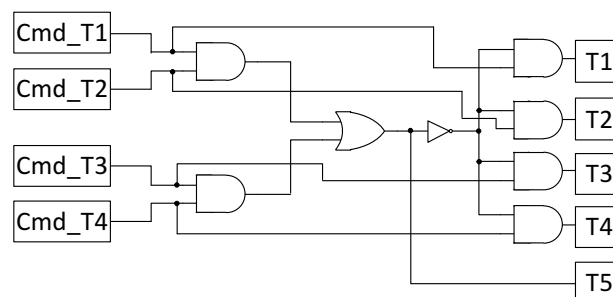


Figure 7. PWM command generation for  $T_5$ .

A further modification to the basic CSI topology is also shown in Figure 6. The two low-power switches,  $T_{ad1}$  and  $T_{ad2}$ , were adopted to obtain a strong reduction of the ground leakage current.

The operating principle relies on the joint action of T5 and the low-power devices. During the zero state, T5 is on and the H-bridge devices are switched off. This operating point effectively decouples the electrical grid from the DC source, and reduces the ground leakage current. However, the full-bridge output terminals remain floating with respect to the grid generator. For this reason, the two additional switches  $T_{ad1}$  and  $T_{ad2}$  connect the output terminals to the negative side of the DC panel, with the objective of limiting the high-frequency oscillation across the parasitic capacitance represented by  $C_{pv}$ . Only one of the two additional switches is active for each half-wave:  $T_{ad2}$  is used during the positive half-wave, and  $T_{ad1}$  during the negative half-wave, respectively. Since some reactive power handling capability is often required for the MICs, a bidirectional device is preferred for the decoupling devices  $T_{ad1}$  and  $T_{ad2}$ . Figure 8 shows the schematic block diagram for the generation of the PWM commands for  $T_{ad1}$  and  $T_{ad2}$ . For the sake of clarity, the PWM signals for a grid voltage period are depicted in Figure 9 where all full bridge signals of the CSI5 (T1-T5) and the additional switches ( $T_{ad1}$  and  $T_{ad2}$ ) are shown.

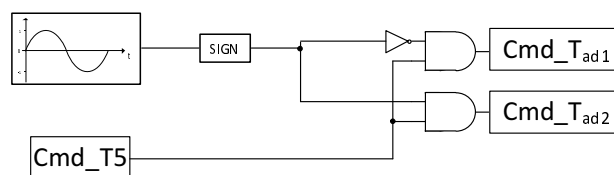


Figure 8. Block diagram of the signal generation for  $T_{ad1}$  e  $T_{ad2}$ .

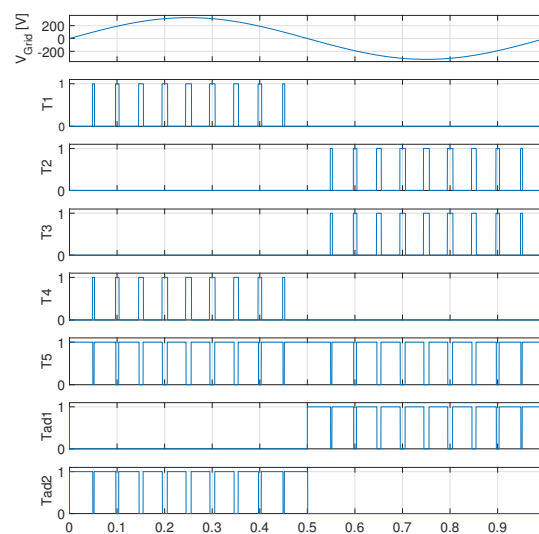


Figure 9. PWM modulation of the proposed CSI5 topology.

Considering the additional features of the proposed solution, the ground voltage can be computed for all the converter states, and it is detailed in Table 1.

Table 1. Summary of ground voltage depending on the modulation states and output half-wave.

	Positive Half-Wave	Negative Half-Wave
<b>Active State</b>	$v_{ground} = +v_{Lf2_{AS}} + v_{D4} + v_{T4}$	$v_{ground} = -v_{Lf1_{AS}} - v_{grid} + v_{D2} + v_{T2}$
<b>Zero State</b>	$v_{ground} = +v_{Lf2_{ZS}} + v_{T_{ad2}}$	$v_{ground} = -v_{C_f} - v_{Lf2_{ZS}} + v_{T_{ad1}}$

As an example, Figure 10 shows the expected ground voltage waveform. During the positive half-wave its value is very low, and it is mainly determined by the voltage across the semiconductor

devices in on-state and the inductive part of the output filter. During the negative half-wave, the grid voltage shape can be recognized, but without the high-frequency switching components.

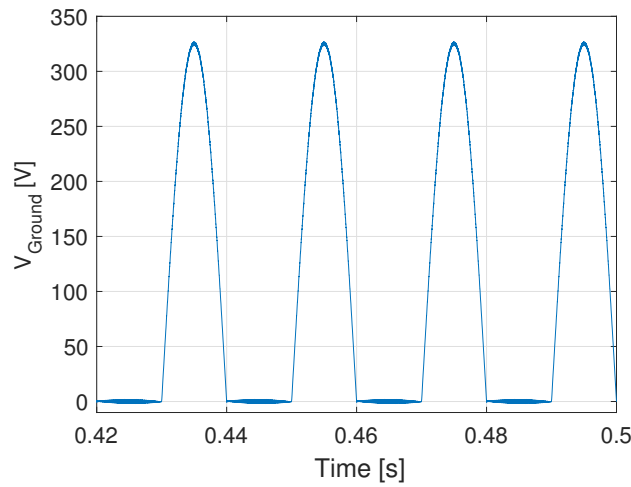


Figure 10. CSI5 topology  $v_{ground}$  waveform with zero  $C_{PV}$ .

The overall control of the proposed solution, considering the pre-stage and the gate signal generation for all devices, is shown in Figure 11. The ideal current source is substituted by a PV panel and a DC–DC synchronous buck converter.

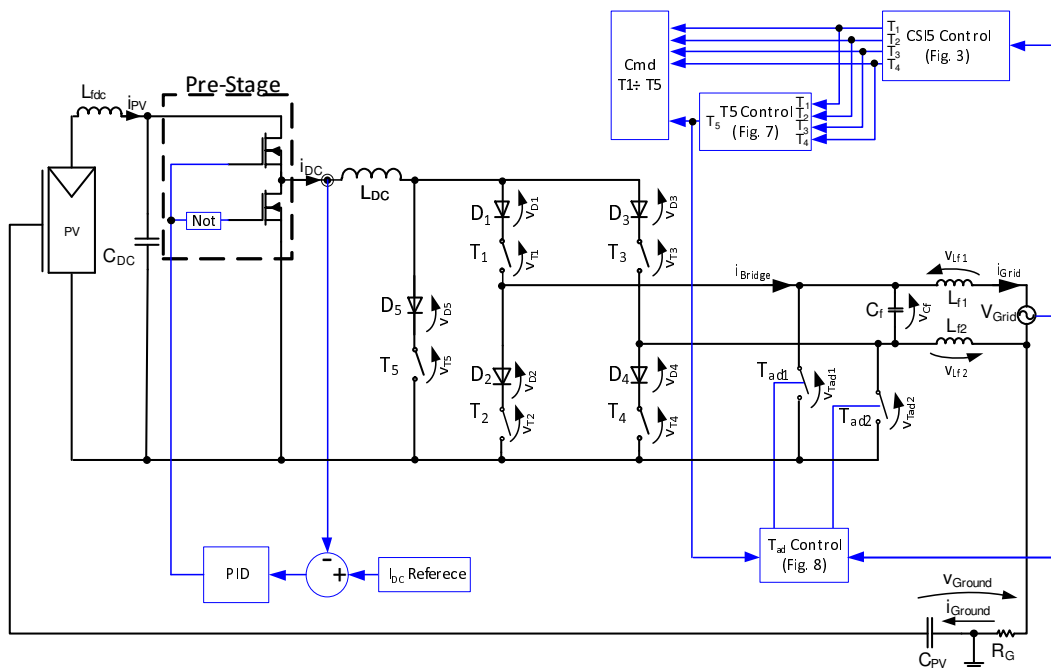


Figure 11. Schematic of the proposed CSI5 topology and control.

The task of the pre-stage is to control the CSI inductor current, effectively reducing the inductance requirement for  $L_{DC}$  and to decouple the PV source from CSI5. Differently from the three-phase PV CSI, in single-phase operation, the pre-stage is needed in order to manage the fluctuation of the instantaneous electric power output with the mandatory low variations of PV source voltage and current.

Different kinds of converters can be chosen for the pre-stage, and a synchronous buck was chosen for its simplicity. It is to be noted that, for this manuscript, the task of the pre-stage was not to control

the input current, since the focus is on the CSI5 topology, and the input current control issues are common to all single-phase PV applications. A DC capacitor was adopted at the input of the pre-stage to reduce the oscillation of the panel operating point. This represents the main drawback for the use in actual PV microinverters of single-phase CSI topologies—to keep the small dimensions and weight, there is the need to manage the output pulsating power through a capacitor. However, different solutions, based on active capacitors [19], can be employed.

It is worth repeating that a single-phase converter would always need some kind of active decoupling connected either in parallel or in series, to match the different power flow of the panels and grid. It is also worth noting that having a continuous fixed current in the inductor is not necessary, since the current value can be changed even without a front-end [20], and inductor current oscillation can be compensated for with proper Pulse Area Modulation [21]. For simplicity's sake and to better focus on the ground leakage current problem, these aspects have not been introduced in this paper, and a simple DC–DC buck converter is used, although it would not represent a practical application.

#### 4. Simulation Results

The performance and operation of both the basic CSI and the CSI5 topology were assessed and compared via numerical simulations in the PLECS environment. The converter topologies are the same as that showed in Figures 1 and 11, and Table 2 summarizes the simulation parameters.

**Table 2.** Parameters used in the simulations.

Name	Description	Value	Unit
$I_{dc}^*$	DC current reference	6	A
$v_{grid}$	Grid Voltage (50 Hz)	230	V <sub>RMS</sub>
$L_{f1}, L_{f2}$	Inductor output Filter	0.5	mH
$L_{fdc}$	Inductor input Filter	0.1	mH
$L_{DC}$	DC Inductor	1	mH
$C_f$	Capacitor output Filter	2.2	μF
$C_{pv}$	Equivalent PV parasitic capacitance	330	nF
$R_G$	Ground resistance	3	Ω
$t_{ov}$	Overlap time	0.5	μs
$f_{sw}$	CSI Switching frequency	30	kHz
$f_{sw,pre}$	Pre-stage Switching frequency	100	kHz
$C_{DC}$	Pre-stage Input Capacitance	2200	μF

The control strategy implemented in the simulation environment for the two solutions are those showed in Figures 2 and 8 and no additional dedicated power factor correction was employed.

The simulations were carried with four BP365PV panels in series and the parameters are summarized in Table 3.

**Table 3.** BP365 PV panel parameters.

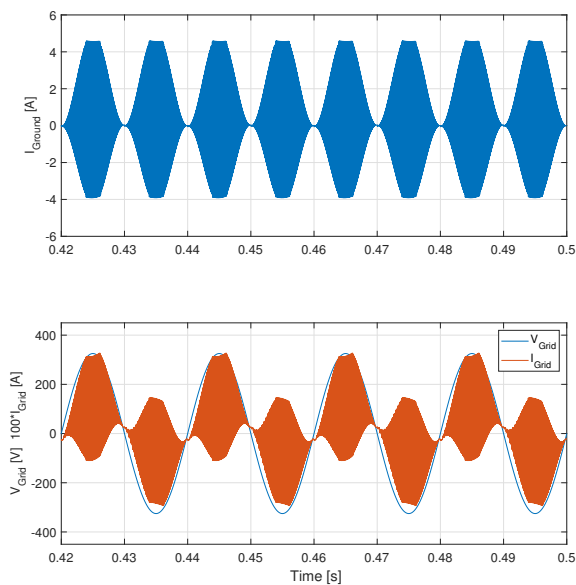
Name	Description	Value	Unit
$P_{max}$	Maximum Power	65	W
$V_{P_{max}}$	Voltage at $P_{max}$	17.6	V
$I_{P_{max}}$	Current at $P_{max}$	3.69	A
$V_{OP}$	Open-circuit voltage	22.1	V
$I_{SC}$	Short-circuit current	3.99	A

The overlap time (see Figure 3) was inserted before the transition command of every transistor. In the simulations, the modulation index K (see Figure 2) was kept equal to 0.23. No common-mode filters were introduced in the electric circuit. Without any degradation of the power quality caused by equivalent parasitic capacitance, the injected power into the grid is equal to 221 W. Figure 12 shows

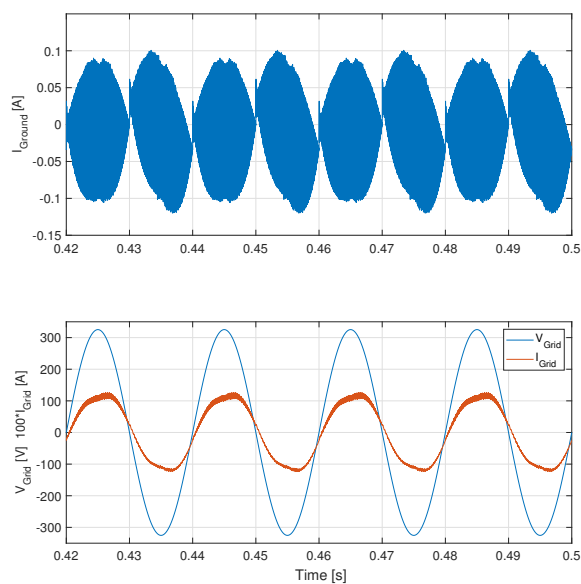


that the grid voltage and injected grid current were characterized by a strong distortion due to the presence of an unacceptably high ground leakage current in the case of basic topology.

Figure 13 shows the same signals of Figure 12 in the case of a proposed CSI5 topology. The strong reduction of the ground leakage current is clearly visible, together with noticeably lower distortion in the injected current. The phase displacement of the injected current with respect to the grid voltage is due to the output filter reactive power, as previously discussed. The asymmetry in the peaks of the ground leakage current is caused by the asymmetry of the ground voltage, as described in Table 1.

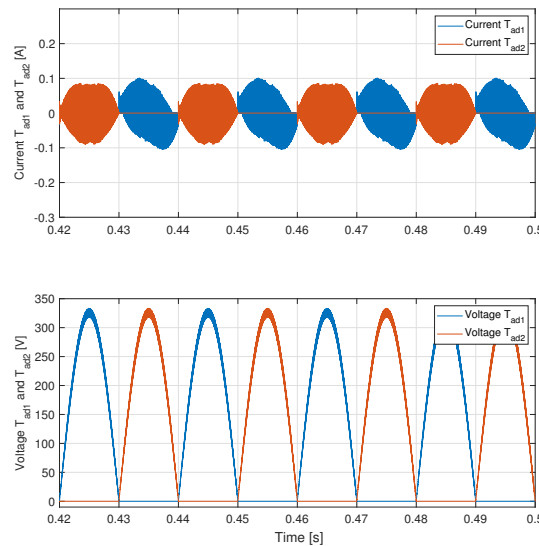


**Figure 12.** Ground leakage current waveform (top), injected grid current waveform ( $\times 100$ ), and grid voltage waveform (bottom) in the case of CSI basic topology. The Root Mean Square RMS of the ground leakage current is equal to  $1.83 V_{RMS}$ .



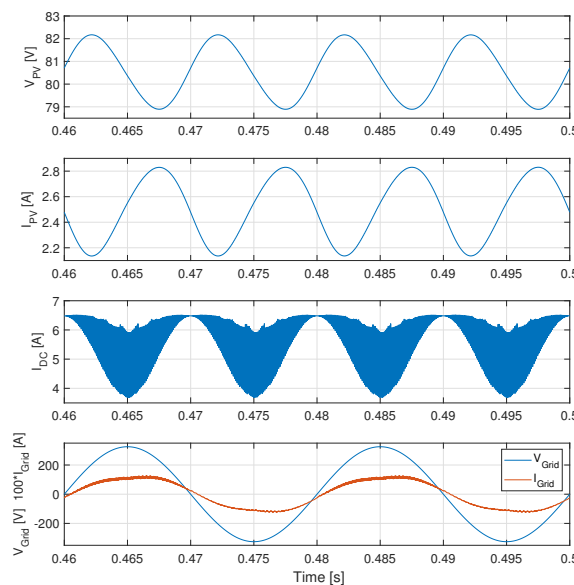
**Figure 13.** Ground leakage current waveform (top), injected grid current waveform ( $\times 100$ ), and grid voltage waveform (bottom) in the case of CSI5 topology. The RMS of the ground leakage current results equal to  $54 mA_{RMS}$ .

The currents of the clamping switches  $T_{ad1}$  and  $T_{ad2}$  are very low, as Figure 14 shows, together with their blocking voltage. The RMS current flowing on  $T_{ad1}$  and  $T_{ad2}$  are equal to 32 mA<sub>RMS</sub> and 27 mA<sub>RMS</sub>, respectively. The two current levels are different because of different resulting current paths, shown in Figure 11.



**Figure 14.** Current waveform (top) and voltage waveform (bottom) of the additional switches  $T_{ad1}$  (blue trace) and  $T_{ad2}$  (red trace).

Another set of simulations was conducted in order to verify the robustness of the CSI5 solution when taking into account the inductance asymmetry between  $L_{f1}$  and  $L_{f2}$ , such as due to manufacturing tolerances; in particular, considering the worst case scenario with a difference of 20% ( $L_{f1} = 450 \mu\text{H}$  and  $L_{f2} = 550 \mu\text{H}$ ), the RMS value of the  $i_{ground}$  results are equal to the previous value (50 mA<sub>RMS</sub>), while the RMS current that flowed in  $T_{ad1}$  and  $T_{ad2}$  were respectively equal to 30 mA<sub>RMS</sub> and 26 mA<sub>RMS</sub>—the difference is negligible.



**Figure 15.** Simulation results with PV panel and DC input current regulation. From top to bottom: PV panel voltage; PV panel current; current on  $L_{DC}$ ; grid voltage (blue) and output current (red) waveforms.

Figure 15 shows an acceptable variation of the PV input current that could be exploited for MPP tracking of the PV panel. As it can be seen, the variation of the current that flows in the DC inductance  $L_{DC}$  did not result in excessive distortion in the current waveform injected into the grid. In the case of a larger variation, such as in order to exploit the  $L_{DC}$  inductor for power decoupling, the injected current THD can be kept under control by employing PAM modulation [22].

## 5. Low Voltage Experimental Validation

A laboratory scale prototype and test set-up was developed in order to perform experimental measurements of the CSI5 topology with aims of assessing the feasibility of the proposed solution and to validate the ground leakage current capability of CSI5 compared to the basic CSI solution.

Figure 16 shows the experimental test set-up, where the CSI5 solution is realized from an existing three-phase CSI7 converter [17]. A basic CSI topology is obtained by disabling in the control firmware the additional bidirectional and clamp switches. Table 4 summarizes the experimental operating parameters.

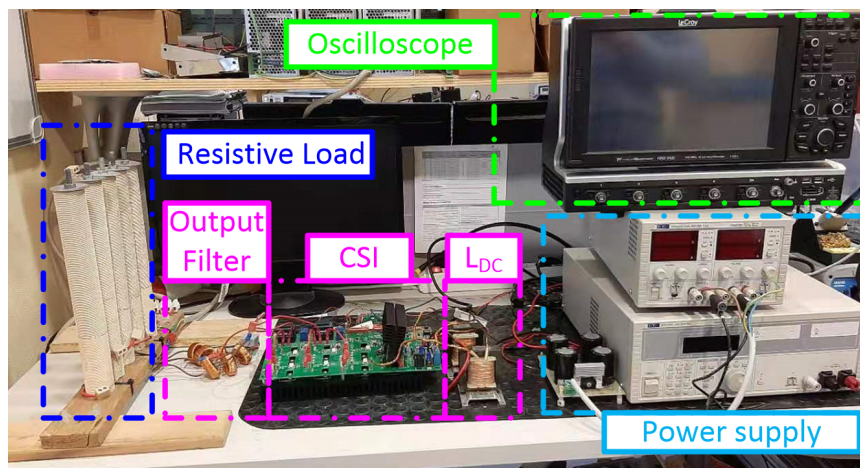


Figure 16. Experimental setup.

Table 4. Experimental test-bed parameters.

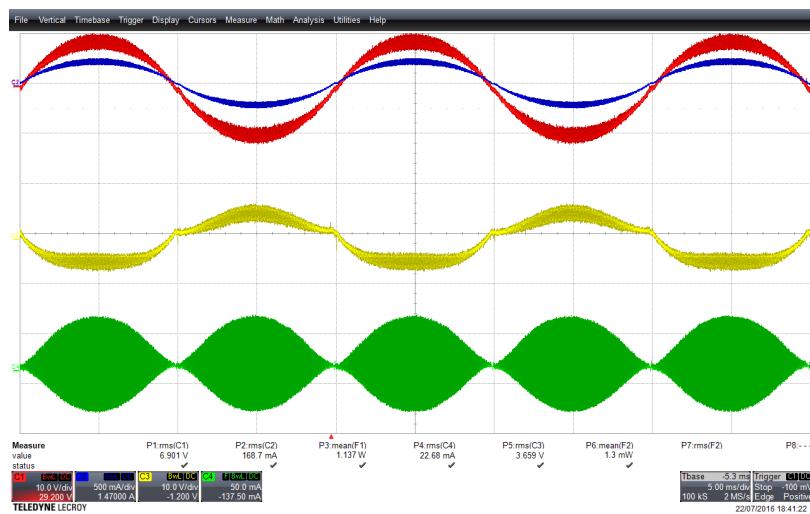
Name	Description	Value	Unit
DC Voltage	$V_{DC}$	30	V
DC source resistance	$R_{DC}$	30	$\Omega$
CSI DC Inductance	$L_{DC}$	1	mH
Output Filter Inductance	$L_{f1} = L_{f2}$	1	mH
Output Filter Capacitance	$C_f$	1.5	$\mu F$
Switching Frequency	$f_{sw}$	30	kHz
Ground Resistance	$R_G$	5	$\Omega$
Equivalent PV parasitic capacitance	$C_{pv}$	250	nF
Load Resistance	$R_{load}$	42	$\Omega$

In the preliminary experimental evaluation, the tests were carried out in stand-alone mode, and the grid was substituted by a load resistor  $R_{load}$ . The converter was supplied by a DC power supply with a resistor  $R_{DC}$  connected in series in order to emulate the PV source I/V characteristic when operating in current control mode. A capacitor with the value described in Table 4 connected between the neutral and the negative terminal of the DC supply was used to simulate the effect of the parasitic capacitance. The ground leakage current was measured with a current probe on the wire connecting this capacitor.

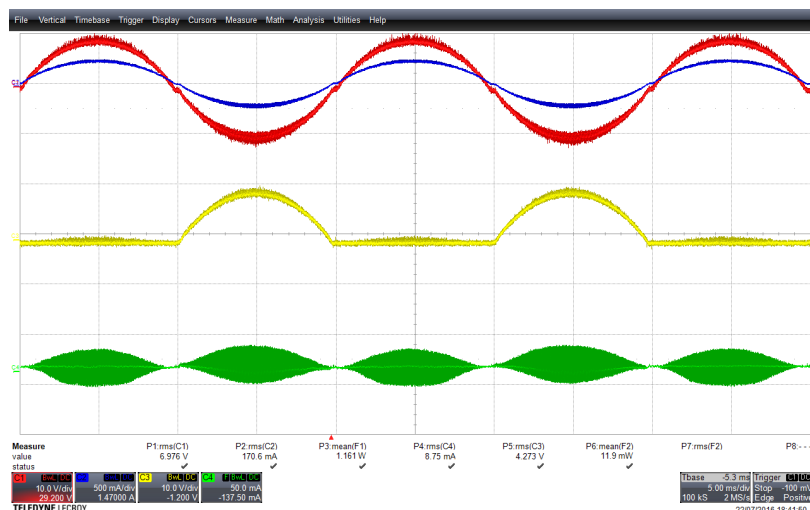
Figure 17 shows the ground leakage current performance of the basic CSI topology. Output voltage and current waveforms, as well as ground voltage and current waveforms are shown. As can be seen, the ground voltage presents large high-frequency components, and the value of ground leakage current is high.

Figure 18 shows the same waveforms of the previous Figure, but with the CSI5 solution without clamping, that is, the presence of the two additional switches  $T_{ad1}$  and  $T_{ad2}$ . As can be seen, the ground voltage waveform is different than in Figure 17, and there is a consequent reduction of ground leakage current.

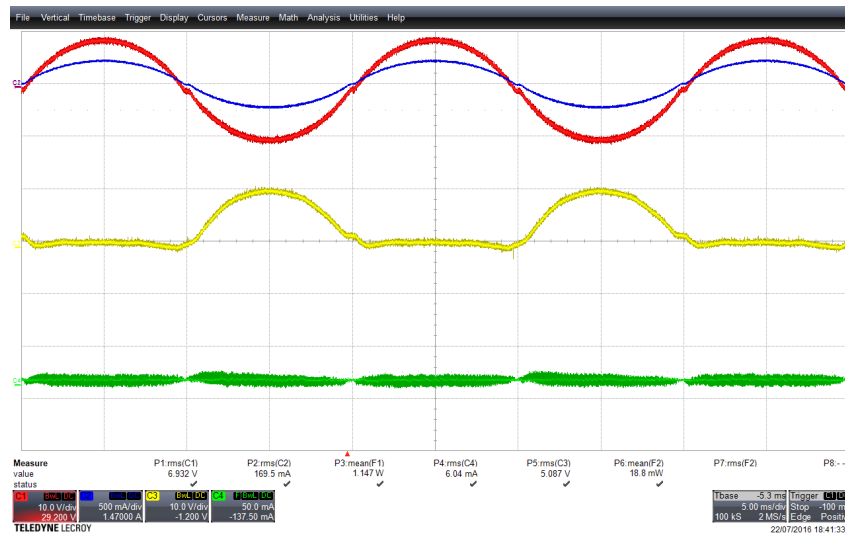
Finally, Figure 19 shows the relevant results for the proposed solution, that is, CSI5 and the additional clamping switches,  $T_{ad1}$  and  $T_{ad2}$ . The high-frequency ground voltage oscillation is further reduced, and the ground leakage current is minimized. Overall, the ground current was reduced from 22.7 mARMS to 6 mARMS by adopting the proposed solution.



**Figure 17.** Experimental results of the basic CSI solution. From top to bottom trace: output voltage (red trace, 10 V/div), output current (blue trace, 500 mA/div), ground voltage (yellow trace, 10 V/div), and ground leakage current (green trace, 50 mA/div). ©2016 IEEE [12].



**Figure 18.** Experimental results of CSI5 solution without clamp. From top to bottom trace: output voltage (red trace, 10 V/div), output current (blue trace, 500 mA/div), ground voltage (yellow trace, 10 V/div), and ground leakage current (green trace, 50 mA/div).



**Figure 19.** Experimental results of proposed CSI5 solution. Trace list from top to bottom: output voltage (red trace, 10 V/div), output current (blue trace, 500 mA/div), ground voltage (yellow trace, 10 V/div), and ground leakage current (green trace, 50 mA/div). ©2016 IEEE [12].

## 6. Conclusions

This paper has thoroughly analyzed the main benefits and disadvantages of a novel Current Source Inverter topology, named CSI5, applied to transformerless photovoltaic single-phase systems. The main advantage is the extremely low ground leakage current, demonstrated theoretically, both by simulations and experimental verification and the ease of control. Furthermore, the CSI5 topology presents the intrinsic boost capability of the CSI and the additional switch T5, dedicated to obtain the output zero state and which allows to strongly reduce the conduction losses with respect to the basic CSI topology.

The main drawback, common to all the single-phase integrated converter solutions, is the power matching between the single-phase grid (characterized by a fluctuating power) and the photovoltaic source (characterized by constant power). In order to decouple the DC PV source requiring almost constant current and voltage at MPP and the instantaneous pulsating output power, an additional pre-stage must be inserted for single-phase CSI.

Another aspect that is worth pointing out for future works is that a certain percentage of power decoupling could be obtained by suitably varying the current of the DC input inductor  $L_{DC}$  without compromising the THD of the injected current, thanks to the use of the Pulse Area Modulation. To conclude, the CSI5 topology can be employed for module integrated application, although a thorough evaluation of the final application requirement should be carried out to weigh the drawbacks described in this manuscript.

**Author Contributions:** Conceptualization, E.L., G.M., F.I., methodology, E.L., G.M., F.I., G.B., validation, G.M., writing—original draft preparation, E.L., G.B., G.M., F.I. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research received no external funding.

**Conflicts of Interest:** The Authors declare no conflict of Interest.

## Abbreviations

The following abbreviations are used in this manuscript:

PV	Photo-voltaic
CSI	Current Source Inverter
VSI	Voltage Source Inverter
MIC	Module Integrated Converter
MPP	Maximum Power Point
MPPT	Maximum power Point Tracker
PLL	Phase Locked Loop
PAM	Pulse Area Modulation
PWM	Pulse Width Modulation
PCC	Point of Common Coupling

## References

1. Barater, D.; Lorenzani, E.; Concari, C.; Franceschini, G.; Buticchi, G. Recent advances in single-phase transformerless photovoltaic inverters. *IET Renew. Power Gener.* **2016**, *10*, 260–273. [[CrossRef](#)]
2. Khan, M.N.H.; Forouzesh, M.; Siwakoti, Y.P.; Li, L.; Kerekes, T.; Blaabjerg, F. Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 805–835. [[CrossRef](#)]
3. Li, Q.; Wolfs, P. A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations. *IEEE Trans. Power Electron.* **2008**, *23*, 1320–1333.
4. Li, W.; Gu, Y.; Luo, H.; Cui, W.; He, X.; Xia, C. Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4537–4551. [[CrossRef](#)]
5. Barater, D.; Buticchi, G.; Crinto, A.; Franceschini, G.; Lorenzani, E. Unipolar PWM Strategy for Transformerless PV Grid-Connected Converters. *IEEE Trans. Energy Convers.* **2012**, *27*, 835–843. [[CrossRef](#)]
6. Concari, L.; Barater, D.; Toscani, A.; Franceschini, G.; Buticchi, G.; Liserre, M.; Zhang, H. Assessment of Efficiency and Reliability of Wide Band-gap based H8 Inverter in Electric Vehicle Applications. *Energies* **2019**, *12*, 1922. [[CrossRef](#)]
7. Ellabban, O.; Abu-Rub, H. Z-Source Inverter: Topology Improvements Review. *IEEE Ind. Electron. Mag.* **2016**, *10*, 6–24. [[CrossRef](#)]
8. Cossutta, P.; Aguirre, M.P.; Cao, A.; Raffo, S.; Valla, M.I. A novel modulation technique for single phase current source inverters with Active Buffering. In Proceedings of the 2015 IEEE International Conference on Industrial Technology (ICIT), Seville, Spain, 17–19 March 2015; pp. 2036–2041.
9. Ohnuma, Y.; Orikawa, K.; Itoh, J.i. A single-phase current-source PV inverter with power decoupling capability using an active buffer. *IEEE Trans. Ind. Appl.* **2014**, *51*, 531–538. [[CrossRef](#)]
10. Lorenzani, E.; Immovilli, F.; Bianchini, C.; Bellini, A. Performance analysis of a modified Current Source Inverter for photovoltaic microinverter applications. In Proceedings of the IECON 2013—39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, Austria, 10–13 November 2013; pp. 1809–1814.
11. Sahan, B.; Araujo, S.V.; Nöding, C.; Zacharias, P. Comparative evaluation of three-phase current source inverters for grid interfacing of distributed and renewable energy systems. *IEEE Trans. Power Electron.* **2010**, *26*, 2304–2318. [[CrossRef](#)]
12. Migliazza, G.; Lorenzani, E.; Immovilli, F.; Bianchini, C. Ground leakage current reduction in single-phase current source inverter topologies. In Proceedings of the IECON 2016—42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, Italy, 23–26 October 2016; pp. 2325–2330.
13. Gubia, E.; Sanchis, P.; Ursua, A.; Lopez, J.; Marroyo, L. Ground currents in single-phase transformerless photovoltaic systems. *Prog. Photovolt. Res. Appl.* **2007**, *15*, 629–650. [[CrossRef](#)]
14. Oppenheim, A.V.; Schafer, R.W.; Buck, J.R. *Discrete-Time Signal Processing*, 2nd ed.; Prentice-Hall, Inc.: Upper Saddle River, NJ, USA, 1999.
15. Kerekes, T.; Teodorescu, R.; Rodríguez, P.; Vázquez, G.; Aldabas, E. A New High-Efficiency Single-Phase Transformerless PV Inverter Topology. *IEEE Trans. Ind. Electron.* **2011**, *58*, 184–191. [[CrossRef](#)]

16. Xiao, H.; Xie, S. Leakage Current Analytical Model and Application in Single-Phase Transformerless Photovoltaic Grid-Connected Inverter. *IEEE Trans. Electromagn. Compat.* **2010**, *52*, 902–913. [[CrossRef](#)]
17. Lorenzani, E.; Migliazza, G.; Immovilli, F.; Gerada, C.; Zhang, H.; Buticchi, G. Internal Current Return Path for Ground Leakage Current Mitigation in Current Source Inverters. *IEEE Access* **2019**, *7*, 96540–96548. [[CrossRef](#)]
18. Lorenzani, E.; Migliazza, G.; Immovilli, F.; Buticchi, G. CSI and CSI7 current source inverters for modular transformerless PV inverters. *Chin. J. Electr. Eng.* **2019**, *5*, 32–42. [[CrossRef](#)]
19. Wang, H.; Wang, H.; Zhu, G.; Blaabjerg, F. An Overview of Capacitive DC-Links-Topology Derivation and Scalability Analysis. *IEEE Trans. Power Electron.* **2020**, *35*, 1805–1829. [[CrossRef](#)]
20. Migliazza, G.; Buticchi, G.; Carfagna, E.; Lorenzani, E.; Madonna, V.; Giangrande, P.; Galea, M. DC Current Control for a Single-Stage Current Source Inverter in Motor Drive Application. *IEEE Trans. Power Electron.* **2020**. [[CrossRef](#)]
21. Hirachi, K.; Ishitobi, M.; Matsumoto, K.; Hattori, H.; Ishibashi, M.; Nakaoka, M.; Takahashi, N.; Kato, Y. Pulse area modulation control implementation for single-phase current source-fed inverter for solar photovoltaic power conditioner. In Proceedings of the 1998 International Conference on Power Electronic Drives and Energy Systems for Industrial Growth, Perth, WA, Australia, 1–3 December 1998; Volume 2, pp. 677–682.
22. Hirachi, K.; Tomokuni, Y. Improved control strategy to eliminate the harmonic current components for single-phase PWM current source inverter. In Proceedings of the Power and Energy Systems in Converging Markets, Melbourne, VIC, Australia, 23 October 1997; pp. 189–194.



© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).