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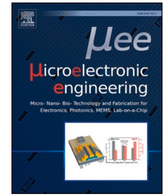

A simple figure of merit to identify the first layer to degrade and fail in dual layer SiO_x/HfO_2 gate dielectric stacks

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ABSTRACT

Understanding the degradation dynamics and the breakdown sequence of a bilayer high-k (HK) gate dielectric stack is crucial for the improvement of device reliability. We present a new Figure of Merit (FoM), the IL/HK Degradation Index, that depends on fundamental materials properties (the dielectric breakdown strength and the dielectric constant) and can be used to easily and quickly identify the first layer to degrade and fail in a bilayer SiO_2/HK dielectric stack. Its dependence on IL and HK material parameters is investigated and its validity is demonstrated by means of accurate physics-based simulations of the degradation process. The proposed FoM can be easily used to understand the degradation dynamics of the gate dielectric stack, providing critical insights for device reliability improvement.

1. Introduction

The adoption of the high-k/metal gate (HK/MG) technology beyond the 45 nm technology node [1] led to the replacement of the thin SiO_2/SiON gate oxide of the MOSFET transistor with a bilayer dielectric stack, consisting of a relatively thin SiO_2 Interfacial Layer (IL) and a thicker overlying HfO_2 high-k (HK) layer. Besides ensuring further device scaling along the path indicated by the Moore's law [2], such change also revealed new behaviors and phenomena concerning overall transistor reliability (and especially gate oxide degradation dynamics), which have been ascribed mainly to the intrinsically higher defectivity of the HK and to its interaction with the underlying IL. One of the key aspects still most debated today concerns dielectric stack degradation and more specifically the identification of the first layer to degrade and fail: is it the SiO_2-based IL or the overlying HfO_2 high-k? The studies published on this topic are about evenly split between the two possibilities: some indicate the HK layer as the primary source of dielectric stack degradation [3–7], while others identify the IL as the first layer to fail [8–15]. The presence of such controversial results supporting the two opposing theses can be ascribed to two main factors: i) the adoption of non-homogeneous stress conditions, which may determine different degradation scenarios [16], and ii) the assumption that the SiO_2-based IL possesses much better properties than the high-k layer (for example in terms of trap density and breakdown strength), which is not the case for the relatively thin SiO_2 layer inserted into the IL-HK bilayer stack. One thing remains obvious: a correct understanding of the degradation dynamics of the IL/HK dielectric stack (as well as of the underlying physics) is of critical importance for a proper interpretation of experiments and for the assessment and prediction of device lifetime.

The purpose of this work is twofold. First, we critically discuss and refute two key misunderstandings (or false myths) that are commonly reported in the literature to support and promote the idea that the high-k is the first material of the gate dielectric stack to degrade under electrical stress. Second, we propose a new figure of merit (FoM), that provides a quick and simple way to identify which layer is expected to degrade (and fail) first in a given IL/HK dielectric stack. The proposed figure of merit is analyzed as a function of specific material properties that are relevant for trap generation (that are, bond energy, dielectric constant and bond polarizability) and demonstrated by means of device simulations.

2. On the properties of the SiO_2-based interfacial layer of a high-k dielectric stack

Two common misunderstanding are usually made (by both academia and industry) when studying and analyzing the degradation and breakdown of high-k gate dielectric stacks comprised of a thin SiO_2 and a thicker overlying high-k (typically HfO_2).

First, there is the strong tendency of assuming the high-k material to

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be (by far) more defective than the SiO_2-based IL, which is instead considered to be very similar to the high quality thermally grown silicon dioxide that was used as the gate dielectric of transistors until the advent of the HK/MG technology. Although this reasoning is substantially correct when considering single layers of the two materials, it does not apply when they are stacked together, due to the structural modifications caused to the IL by its interactions with the overlaying HfO_2 film. Several studies demonstrated that the SiO_2 layer of the high-k stack is typically sub stoichiometric [17] and as such characterized by a higher dielectric constant [18,19] and by a significant density of oxygen vacancy traps. The latter has been estimated to be in the range of 10^{18}–$5{\cdot}10^{19}$ cm^{-3} [9,20,21] and thus comparable with the typical density of HfO_2 traps, 10^{18}–10^{20} cm^{-3} [22,23]. In presence of a relatively thin HK layer ($\leq$ 3 nm) these IL oxygen vacancies dominate the charge transport through the dielectric stack [24]. This is shown in Fig. 1, reporting the gate leakage current measured and simulated as a function of the temperature on MOSFET capacitors having either a 2 nm-thick SiO_2 layer or a 1.1 nm/3 nm SiO_x/HfO_2 gate dielectric stack (with TiN metal gate). Simulations are performed with the Ginestra® simulation platform (see Section 4) [25]. In the case of the 2 nm-thick SiO_2, see Fig. 1(a), the experimental current and its temperature dependence are nicely reproduced by the direct tunneling (DT) current, while the trap-assisted tunneling (TAT) contribution is negligible owing to the low defect density (10^{15} cm^{-3}) of the high-quality SiO_2 [24]. On the contrary, in the SiO_x/HfO_2 gate dielectric stack the gate leakage current is dominated by the TAT component, while DT contribution is orders of magnitude smaller, see Fig. 1(b). Furthermore, simulations show that the charge transport is primarily assisted by the traps located in the IL [9,24]. Table 1 reports material and trap parameters used in the simulations.

The second common misunderstanding in the analysis of degradation and breakdown of the IL/HK gate dielectric stacks is related to the breakdown (or dielectric) strength (F_{BD}), an intrinsic property corresponding to the electric field at which an insulating material experiences breakdown. It has been experimentally demonstrated and is widely accepted that F_{BD} is inversely proportional to the material dielectric constant [28,29]. Consistently, SiO_2 is characterized by a much higher F_{BD} (in the 10–20 MV/cm range) with respect to Hafnium oxide (in the 4–7 MV/cm range) [30,31]. This leads to the general belief that HfO_2 is the first layer to degrade in the high-k gate dielectric stack, since its breakdown strength is by several times smaller than the one of the Silicon dioxide-based interfacial layer. Again, this reasoning applies only when the two materials are considered separately, but not when they are stacked together as in the case of the high-k dielectric stack. In the latter case, there is another important factor that must be taken into consideration: the applied electric field redistributes according to Gauss's law and will be higher in the material with the lowest dielectric constant (κ). Therefore, any consideration on the degradation of the materials composing the stack cannot be made only by considering the breakdown

Table 1
SiO_2 IL and HfO_2 HK material and trap parameters used in the leakage current simulations in Fig. 1.

Parameter	SiO_2 IL	HfO_2 HK	Reference
Relative dielectric constant, κ	6.6	21	[24,25]
Elecron affinity, χ_e (eV)	0.95	2.4	[24,25]
Energy band-gap, E_G (eV)	8.9	5.8	[24,25]
Electron tunneling effective mass, m_e*	0.5	0.25	[24,25]
TiN work function, WF (eV)	4.57		[26]
Traps' density, N_T (cm^{-3})	$4.7{\cdot}10^{19}$	$4.5{\cdot}10^{19}$	this work
Traps' thermal ionization energy, E_T (eV)	2.3–3.4	1.7–2.7	[24,25,27]
Traps' relaxation Energy, E_{REL} (eV)	0.36	1.19	[24,25]

strength, but must also take into account the difference between their dielectric constants, which determines the internal field redistribution. It will be the balance between the ratios of F_{BD} and κ of the different materials that will ultimately determine what layer of the stack will degrade and break first.

The two common misunderstandings just discussed may wrongly promote and strengthen the idea that the HK is the first layer to degrade and fail in a bilayer IL/HK stack. In the next section we will derive and define a new Figure of Merit that unambiguously provides a clear indication about the first layer that is expected to break in a bilayer stack.

3. A new figure of merit: the IL/HK degradation index

As discussed in the previous Section, any analysis or consideration about the breakdown of the materials composing a multi-layer dielectric stack must take into account both the breakdown strength and the dielectric constant of the different layers. The first defines the value of the electric field at which the specific material is subject to breakdown. The latter determines the field redistribution within the different layers of the stack and thus the electric field to which each layer is subjected. Here we define a FoM incorporating these two key properties (F_{BD} and κ) into a simple formula allowing determining which layer of an IL/HK bilayer dielectric stack is expected to experience breakdown (and degradation) first.

First of all, the breakdown process of a given dielectric layer subjected to electrical stress is determined by the electric field it experiences. Adopting the effective energy formalism [30,32,33], the rate G (or trap generation rate) in the dielectric can be expressed as a function of temperature (T) and field (F) as:

$$G = G_0 exp\left[-\frac{E_A - bF}{k_B T}\right] = G_0 exp\left[-\frac{b}{k_B T}(F_{BD} - F)\right] \tag{1}$$

G_0 is the bond vibration frequency, E_A the zero-field bond-breakage activation energy, $b = p_0(2+\kappa)/3$ the bond polarization factor (p_0 is the active dipole moment and κ the relative dielectric constant), and k_B the

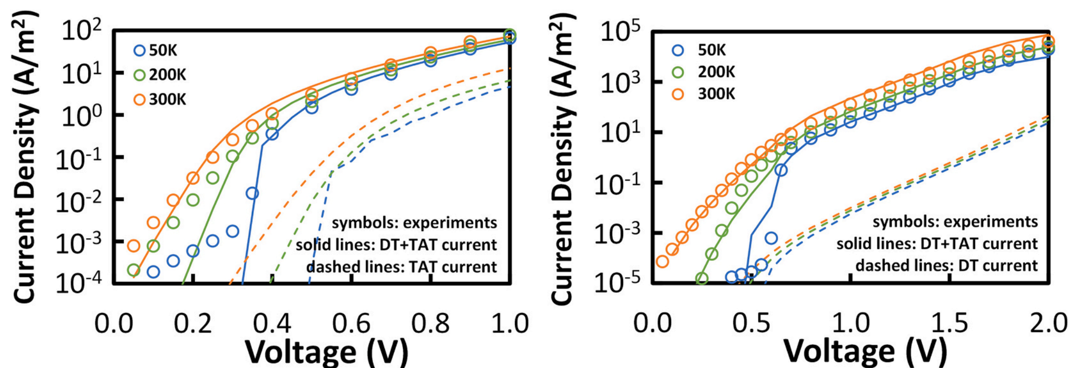

Fig. 1. Gate leakage current densities (symbols) measured and (lines) simulated as a function of the temperature on MOSFET capacitors with (a) a 2 nm-thick SiO_2 layer and (b) a 1.1 nm/3 nm SiO_x/HfO_2 gate dielectric stack. Material and trap parameters used in simulations are reported in Table 1.

Boltzmann's constant. $F_{BD} = E_A/b$ is the so-called breakdown strength [29,30], that in (1) identifies the field corresponding to the maximum bond breaking rate ($G = G_0$).

From (1), it is clear that the magnitude of the external field F with respect to the breakdown field F_{BD} provides information on the dielectric degradation rate (note that this is valid independently on the considered breakdown model). Therefore, we can define a degradation metric for a given material as the ratio between the electric field F at which is subjected and its breakdown strength F_{BD}. For the IL and HK layers of a high-k dielectric stack we have:

$$D_{IL} = \frac{F_{IL}}{F_{BD,IL}} \tag{2}$$

$$D_{HK} = \frac{F_{HK}}{F_{BD,HK}} \tag{3}$$

where F_{IL}, F_{HK} and $F_{BD,IL}$, $F_{BD,HK}$ are respectively the electric field and the breakdown strength of IL and HK layers. As the electric field across the layer approaches F_{BD}, the degradation rate in the dielectric increases until it reaches breakdown conditions when $F = F_{BD}$ [for which G is maximum, see (1)] that is, when D = 1.

From (2) and (3) follows:

$$\frac{D_{HK}}{D_{IL}} = \frac{F_{BD,IL}}{F_{IL}}\frac{F_{HK}}{F_{BD,HK}} \tag{4}$$

By applying the Gauss' law to the two layers one can relate F_{IL} and F_{HK} in (4) to each other and to their dielectric constants [10]:

$$F_{HK}\kappa_{HK} = F_{IL}\kappa_{IL} \tag{5}$$

where κ_{IL} and κ_{HK} are the relative dielectric constants of IL and HK layers, respectively. Eq. (5) can be used to determine the ratio between the electric fields in the HK and IL, which is equal to the inverse ratio of the relative dielectric constant: $F_{HK}/F_{IL} = \kappa_{IL}/\kappa_{HK}$. When this is substituted into (4) we obtain

$$DI_{IL/HK} = \frac{F_{BD,IL}}{F_{BD,HK}}\frac{\kappa_{IL}}{\kappa_{HK}} \tag{6}$$

That we define as the **IL/HK Degradation Index $DI_{IL/HK}$**, a simple, field-independent figure of merit indicating which among HK and IL is expected to degrade and break first. It must be noted that the ratio between the breakdown strengths, $F_{BD,IL}/F_{BD,HK}$, is always higher than one (as discussed in Section 2), whereas the ratio between the dielectric constants (that represents the ratio between the electric fields), κ_{IL}/κ_{HK}, is always smaller than one. It is therefore the balance between these two quantities, expressed by the IL/HK Degradation Index, that determines which layer breaks first. When $DI_{IL/HK} < 1$, this balance favors the degradation of the IL, that thus breaks faster than the HK. When $DI_{IL/HK} > 1$, the opposite applies. BD conditions are reached earlier in the HK, that will thus degrade and break faster than the IL.

Using (6) to calculate the IL/HK Degradation Index considering typical material parameter for SiO_2 IL and HfO_2 HK layers (Table 2) indicates that degradation is more likely to occur first in the interfacial layer, since $DI_{IL/HK}$ is always smaller than one (from 0.35 to 0.84). It must be noted that the dielectric constant of the IL can be significantly higher than the one of the pure SiO_2, due to its sub-stoichiometric nature [18,19] which is not accounted for in most of the cases reported in Table 2. The exact κ_{IL} value depends on the process conditions and on the thicknesses of the IL and HK layers. Relative IL dielectric constants of 5–6 [14,24], 7.5 [19] and 9 [19] have been reported for IL thicknesses around 10 Å, 5 Å and 3 Å, respectively (with HfO_2 thicknesses in the 20-40 Å range). Similarly, theoretical calculations show that the κ_{IL} is expected to increase to values of ~6 and ~ 10 for thicknesses of 5 Å and 3 Å, respectively [18]. However, even taking into account a higher $\kappa_{IL} = 6$ for all the cases in Table 2 (a quite reasonable value for an IL in the 8-10 Å thickness range), the IL/HK Degradation Index remains smaller than one, indicating that the degradation of the high-k stack is still expected to be controlled by the Interfacial Layer (not shown).

Table 2
Typical breakdown strengths and relative dielectric constants reported for IL and HK materials. Values indicated with * are not provided in the indicated reference and are thus selected according to other values reported in the literature.

HK material	κ_{IL}	κ_{HK}	$F_{BD,IL}$ (MV/cm)	$F_{BD,HK}$ (MV/cm)	$DI_{IL/HK}$	Reference
HfO_2	3.9	25	15	3.9	0.6	[30]
HfO_2	3.9	25	15	6.7	0.35	[30]
HfSiON	6	14	13.6	7.2	0.81	[14]
HfO_2	6	21	20	7.5	0.84	[15]
HfO_2	3.9*	21*	18	6	0.56	[31]
HfO_2	3.9*	21*	13	4	0.6	[31]

Based on these results and considerations, an early degradation and breakdown of the HK layer seems unlikely and possible only in presence of a highly sub-stoichiometric IL (characterized by a κ_{IL} higher than the 3.9 of stoichiometric SiO_2) and/or a value of the HK relative dielectric constant lower than 20 (that is typically too small for its use in a high-k gate dielectric stack). The impact of IL and HK material parameters on the IL/HK Degradation Index will be addressed in the next Section.

4. Simulation results and discussion

Simulations are performed with Applied Materials' commercial semiconductor device simulation software Ginestra® [25], which provides a comprehensive and self-consistent description of charge trapping and transport [34], degradation phenomena [26,35,36], and material modifications in the considered material stacks. The conduction through dielectric materials is described accounting simultaneously for a variety of charge transport mechanisms, such as direct/Fowler-Nordheim tunneling, drift-diffusion in conduction/valence and defect bands, thermionic emissions, and trap assisted tunneling (TAT), the latter implemented in the framework of the multi-phonon theory [24,37–39]. An example of the related material and trap parameters is reported in Table 1 for the charge transport simulations in Fig. 1. Charge transport equations are self-consistently solved together with the Poisson's equation (accounting for defects charge state and occupation), the Fourier's equation (for the calculation of power dissipation and temperature increase within the material stack [35]) and the equations describing atomic-level material modifications originating from electrical/thermal stresses [26,35,36,40]. The atomistic processes responsible for the creation of new defects are implemented using the effective energy formalism [30,32,33], see eq. (1) in Section 3. The stochastic nature of the trap generation process is accounted for by exploiting the Monte Carlo technique described in [41]. In this work (1) is used in its simpler form, in which E_A and b are macroscopic quantities providing an equivalent description of more complex microscopic processes (typically involving bond weakening induced by carriers' injection and trapping into pre-existing defects [26,35,36]). Such a macroscopic description of the bond-breakage process is more suitable for the scope of this work.

Finally, it is important to underline again that the breakdown field of a given material can be calculated as the ratio between E_A and b in (1) [30]. This provides a direct connection between (1) and (6) that will be exploited in the following to analyze the dependence of the FoM introduced in Section 3 on specific IL and HK material properties and thus understand under which conditions the degradation of the IL/HK dielectric stack is expected to be dominated by one layer or the other.

Figure 2 shows four contour plots of the IL/HK degradation index calculated as a function of IL and HK relative dielectric constants. They are obtained considering different values of IL and HK breakdown strengths, matching the experimental limits derived in [31] [Fig. 2(a), (b)], and to the theoretical values reported in [30] [Fig. 2(c), (d)]. The yellow stars on the plots identify five specific points matching to the κ_{IL} and κ_{HK} values of typical IL/HK dielectric stacks (1: $\kappa_{IL}/\kappa_{HK} = 3.9/25$; 2: $\kappa_{IL}/\kappa_{HK} = 3.9/21$; 3: $\kappa_{IL}/\kappa_{HK} = 6/25$; 4: $\kappa_{IL}/\kappa_{HK} = 6/21$; 5: $\kappa_{IL}/\kappa_{HK} = 9/$

Fig. 2. Contour plots showing the IL/HK degradation index as a function of IL and HK relative dielectric constant, corresponding to four different cases of IL and HK breakdown strengths: a) $F_{BD,IL} = 13MV/cm$; $F_{BD,HK} = 4MV/cm$ b) $F_{BD,IL} = 18MV/cm$; $F_{BD,HK} = 6MV/cm$, corresponding to the experimental limits derived in [31], and c) $F_{BD,IL} = 15MV/cm$; $F_{BD,HK} = 4MV/cm$ d) $F_{BD,IL} = 15MV/cm$; $F_{BD,HK} = 6.7MV/cm$, corresponding to the theoretical values reported in [30]. Yellow stars indicate some typical values of IL and HK relative dielectric constants (see Section 3). Black solid lines indicate the level curve corresponding to $DI_{IL/HK} = 1$. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

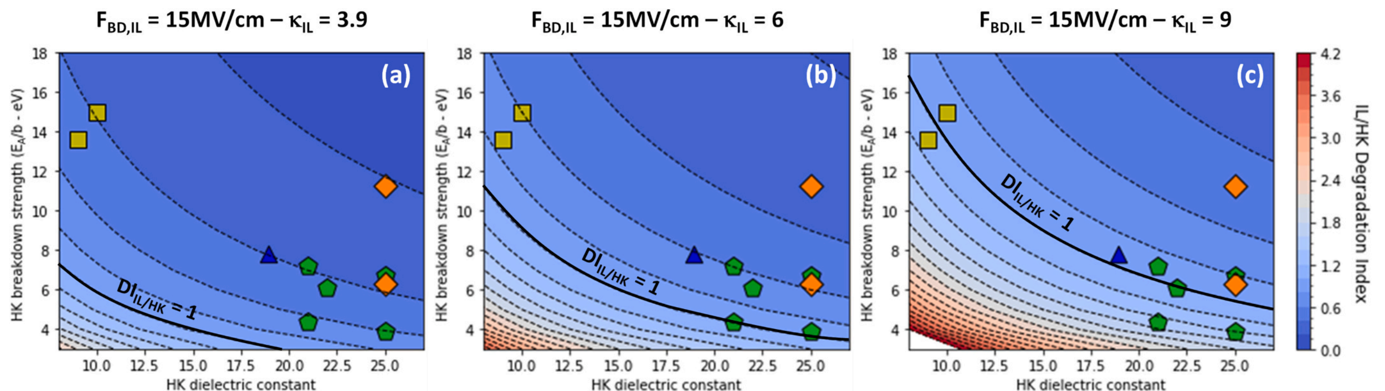

Fig. 3. Contour plots showing the IL/HK degradation index as a function of HK relative dielectric constant and breakdown strength, for $F_{BD,IL} = 15MV/cm$ and three different cases of the IL relative dielectric constant: a) $\kappa_{IL} = 3.9$, b) $\kappa_{IL} = 6$, and c) $\kappa_{IL} = 9$. Symbols indicate the $DI_{IL/HK}$ values calculated considering HfO_2/HfO_x (green pentagons), ZrO_2 (orange diamonds), Al_2O_3 (yellow squares), and HfAlO (blue triangle) materials (see Table 3) as the HK layer of the stack. Black solid lines indicate the level curve corresponding to $DI_{IL/HK} = 1$. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

25). They are representative of stacks with thick (≥ 12 Å, points 1 and 2), thin (8-10 Å, points 3 and 4) and very thin (3 Å, point 5) IL and a HfO_2 thicknesses in the 20A-40 Å range (see also discussion in Section 3). As can be seen, these points are almost always located in the region characterized by $DI_{IL/HK} < 1$ (that is, the blue region below the solid black line), suggesting that the earlier degradation of the interfacial layer can be expected in most of the cases. Only when the ratio between IL and HK breakdown strength is high (roughly speaking, larger than 3.5), as in Fig. 2(c), or the IL dielectric constant is high, as for point 5 in Figs. 2(a)-(c), $DI_{IL/HK} > 1$ and the degradation is expected to start in the high-k layer. It is worth noting that also a smaller high-k dielectric constant (below 20) significantly increases the probability to have $DI_{IL/HK} > 1$ and thus the HK as the first layer to break (it would correspond to a left shift of the considered κ_{IL}/κ_{HK} point in Fig. 2).

The IL/HK degradation index is reported in Fig. 3 as a function of high-k material properties, the relative dielectric constant and the breakdown strength, while considering $F_{BD,IL}$ = 15MV/cm and three different values of the IL relative dielectric constant (typical of different IL thicknesses, as already discussed). The symbols on the plots identify the $DI_{IL/HK}$ values calculated when considering the specific materials listed in Table 3 as the HK layer of the IL/HK stack: HfO_2/HfO_x (green pentagons), ZrO_2 (orange diamonds), Al_2O_3 (yellow squares), and HfAlO (blue triangle). Note that in these cases the HK breakdown strength has been calculated as the ratio between the zero-field bond-breakage activation energy E_A and the bond polarization factor b, whose values are either provided in the indicated references or extracted from the reported time-dependent dielectric breakdown experimental data using the methodology in [23]. As discussed above, these numbers are macroscopic quantities providing an equivalent description of the more complex microscopic degradation processes involving bond weakening induced by carriers' injection and trapping into pre-existing defects [26,35,36]. Fig. 3 shows that all the calculated data points are located in the region characterized by $DI_{IL/HK} < 1$ (the blue region above the solid black line) when the relative dielectric constant of the underlying IL is either 3.9 or 6, see Figs. 3(a), (b). Therefore, degradation is expected to occur first in the IL when considering any of the materials in Table 3 as the HK layer of the stack. Only in the case of a higher κ_{IL} (> 6), which corresponds to a thin IL (below ~8 Å), the breakdown of some of the considered stacks will be driven by the degradation of the HK layer, see Fig. 3(c).

Besides providing a clear indication about the first layer to degrade and fail in a bilayer IL/HK dielectric stack, the proposed FoM and the results in Figs. 2 and 3 allow understanding the role of material parameters on the degradation dynamics, which is critical for the improvement of device reliability. Once the weak layer is identified, the analysis performed here can be used to understand how the material properties of the stack can be improved to extend device lifetime and reliability margins. Noticeably, the proposed approach is general and can be also applied for understanding the forming/degradation dynamics of devices comprising a multilayer dielectric stack, such as memory capacitors [42], resistive random-access memories (RRAMs) [43], and memristors [44].

In order to prove the validity of the proposed FoM we used the Ginestra® [25] modeling framework to simulate the degradation dynamics of two SiO_x/HfO_2 dielectric stacks, whose thicknesses, materials properties and IL/HK degradation indexes are reported in Table 4 [stack #1 and #2 respectively correspond to points 2 and 4 in Fig. 2(c)]. From the calculated degradation indexes, dielectric breakdown is expected to be driven by the degradation of the SiO_x IL in stack #1 ($DI_{IL/HK} = 0.7$), and of the HK in stack #2 ($DI_{IL/HK} = 1.07$). Simulations are performed considering a constant voltage stress (CVS) with stress voltages (V_{STRESS}) of 3.1 V and 1.6 V, selected to induce the same equivalent electric field, $F_{EOT} = V_{STRESS}/EOT$. Simulations stop as soon as the gate current reaches 10 μA.

Simulations results shown in Figs. 4 and 5 respectively for the 12 Å/30 Å SiO_x/HfO_2 and 8 Å/20 Å SiO_x/HfO_2 devices provide a detailed understanding of the degradation process in the bilayer gate dielectric stack. They show the evolution of oxygen vacancies distribution (along the thickness and in the X, Y plane), the 2D temperature map in the X, Y plane, and the current driven by traps in the X, Y plane. As expected, the two devices considered exhibit rather different degradation dynamics.

In the case of stack #1, oxygen vacancy traps are first generated only into the IL, Fig. 4(b), consistently with the calculated $DI_{IL/HK}$ of 0.7. The device is in the so-called Stress-Induced Leakage Current (SILC) stage, characterized by uniform degradation, Fig. 4(b), temperature profile, Fig. 4(f), and current distribution, Fig. 4(j). Traps continue to be generated uniformly in the IL volume until the formation of a BD spot with a larger local concentration of oxygen vacancies (up to 10^{21} cm^{-3}), Fig. 4(c), bringing the device into the soft/progressive BD stage (SBD/PBD) stage. Besides causing a small increase of local temperature, Fig. 4(g), and current, Fig. 4(k), this event determines a significant redistribution of the internal electric field, since now the applied stress voltage falls almost entirely on the unbroken HfO_2 layer. This triggers a massive defect generation in the HK, Fig. 4(d), eventually leading to the BD of the entire dielectric stack (hard BD phase). Note that the defect generation in the HK is localized almost entirely in correspondence of the initial IL BD spot and is accompanied by a significant increase in the local temperature, Fig. 4(h), and current, driven mainly by the BD filament, Fig. 4(l).

Table 4
Thicknesses and properties of the SiO_x and HfO_2 layers considered in the breakdown simulations shown in Figs. 4 and 5.

stack	t_{IL}	t_{HK}	EOT	κ_{IL}	κ_{HK}	$F_{BD,IL}$	$F_{BD,HK}$	$DI_{IL/HK}$
#1	12 Å	30 Å	17.6 Å	3.9	21	15MV/cm	4MV/cm	0.7
#2	8 Å	20 Å	8.9 Å	6	21	15MV/cm	4MV/cm	1.07

Table 3
Relative dielectric constant (κ_{HK}), zero-field bond breakage activation energy (E_A), active dipole moment (p_0) and bond polarization factor (b) reported in the literature for different HK material, and the corresponding calculated breakdown strength ($= E_A/b$) and IL/HK degradation index (for $F_{BD,IL}$ = 15MV/cm and three different κ_{IL} values as in Fig. 3).

HK material	κ_{HK}	E_A (eV)	p_0 (eÅ)	b (eÅ)	$F_{BD,HK}$ (MV/cm)	$DI_{IL/HK}$ (κ_{IL} = 3.9)	$DI_{IL/HK}$ (κ_{IL} = 6)	$DI_{IL/HK}$ (κ_{IL} = 9)	Reference
HfO_2	25	6.15	10.2	91.8	6.7	0.35	0.54	0.81	[30]
HfO_2	25	1.54	4.4	39.6	3.9	0.60	0.92	1.38	[30]
HfO_2	21	2.87	5.22	40	11.48	0.39	0.60	0.90	[23]
HfO_x	21	1.75	5.22	40	6.85	0.64	0.98	1.47	[23]
HfO_x	22	2.1	4.3	34.4	6.1	0.44	0.67	1.01	[45]
HfAlO(9:1)	18.9	1.90	3.5	24.38	7.79	0.40	0.61	0.92	[45]
Al_2O_3	9	2.30	4.6	16.87	13.63	0.48	0.73	1.10	[45]
Al_2O_3	10	2.40	4	16	15	0.39	0.60	0.90	[40]
ZrO_2	25	1.80	1.78	16	11.25	0.21	0.32	0.48	[46]
ZrO_2	25	2.42	4.28	38.5	6.29	0.37	0.57	0.86	[47]

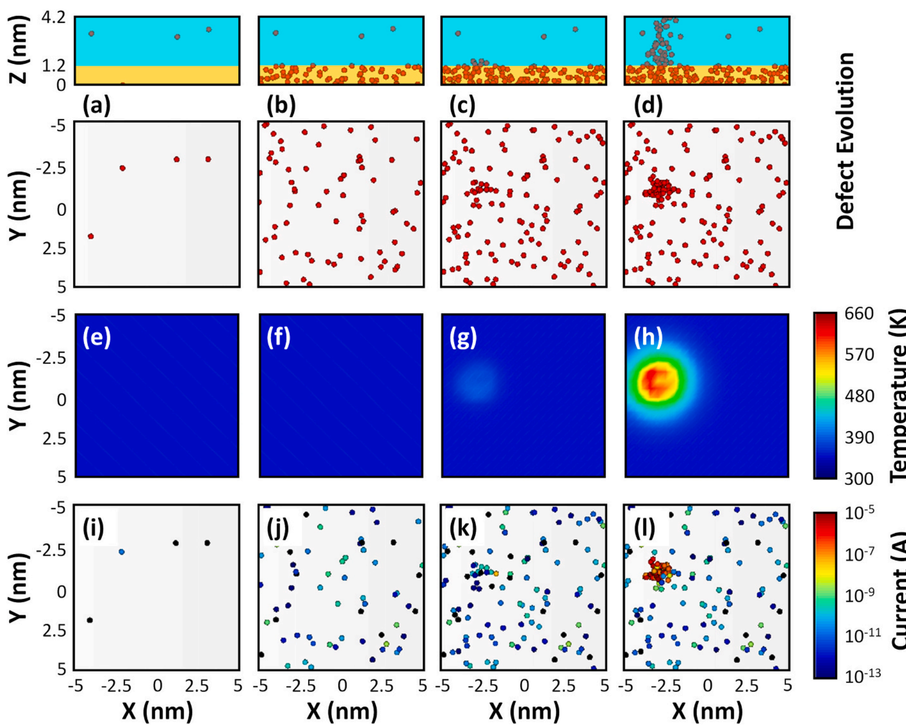

Fig. 4. Evolution of (from top to bottom): (a)-(d) distribution of oxygen vacancies (red spheres) along the thickness and in the X, Y plane; (e)-(h) 2D (X, Y) temperature map; (i)-(l) 2D (X, Y) map of the current driven by oxygen vacancy traps. All maps are shown for subsequent phases of the degradation process (from left to right: fresh device, SILC, SBD/PBD, and HBD) as simulated at 300 K with a stress voltage of 3.1 V on the 12 Å/30 Å SiO_x/HfO_2 stack. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

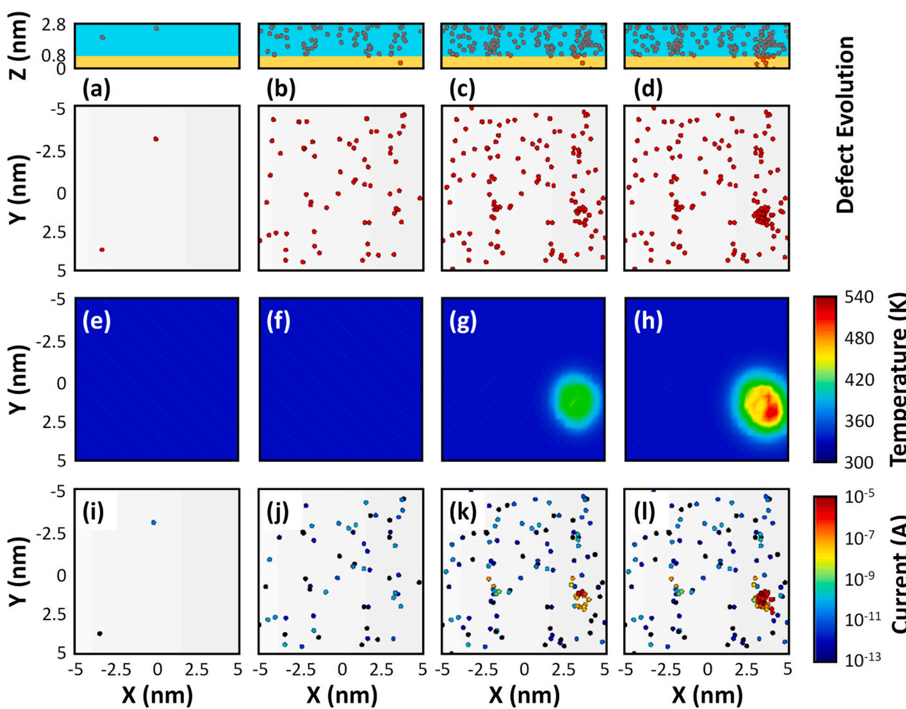

Fig. 5. Evolution of (from top to bottom): (a)-(d) distribution of oxygen vacancies (red spheres) along the thickness and in the X, Y plane; (e)-(h) 2D (X, Y) temperature map; (i)-(l) 2D (X, Y) map of the current driven by oxygen vacancy traps. All maps are shown for subsequent phases of the degradation process (from left to right: fresh device, SILC, SBD/PBD, and HBD) as simulated at 300 K with a stress voltage of 1.6 V on the 8 Å/20 Å SiO_x/HfO_2 stack. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

The results of the simulated CVS on stack #2 are shown in Fig. 5. Differently from the case of stack #1 and in agreement with the value of the defined FoM ($DI_{IL/HK} = 1.07$), in this case the degradation starts in the HK layer, Fig. 5(b). Once traps start to be generated, the evolution of the degradation is similar to what discussed already for stack #1, although the role of the IL and HK layers is inverted. Stress-induced oxygen vacancies are generated uniformly within the entire HfO_2 volume, Fig. 5(b), until the formation of one or more SBD spots, Fig. 5(c), that typically drive more current than the rest of the device, Fig. 5(k). Eventually, the current flowing through one of these SBD spots reaches a value high enough to determine an increase in the local power dissipation and temperature, Fig. 5(g). This, in turn, increases the local trap generation rate, thus forcing subsequent oxygen vacancies to be created preferentially nearby the hot spot. This triggers a thermally driven positive feedback that quickly leads to the breakdown of the entire stack, with the propagation of the HK BD spot into the underlying region of the IL, Fig. 5(d).

It is worth to underline that the simulation results shown in Figs. 4

and 5 are just a single statistical example. Although the general behavior will be the same for all nominally equivalent devices, some variations are expected in the final configurations of the generated traps, for example in terms of size, shape and number of initial SBD spots as well as in terms of size and shape of the final HBD spot. Nevertheless, the results shown in Figs. 4 and 5 confirm the validity of the proposed FoM, the IL/HK degradation index, as a simple end efficient way to understand what layer of a bilayer gate dielectric stack is expected to degrade and break first.

5. Conclusions

We presented a new Figure of Merit, the IL/HK degradation index, that allows to understand what layer of a bilayer gate dielectric stack is expected to degrade and break first when subjected to electrical stress. The dependence of the FoM on IL and HK material parameters has been investigated and its validity has been demonstrated by means of accurate physics-based simulations of the degradation process. The proposed IL/HK degradation index can be easily used to understand the role of material parameters on the degradation dynamics of the gate dielectric stack, providing critical insights for device reliability improvement.

CRediT authorship contribution statement

Andrea Padovani: Conceptualization, Methodology, Investigation, Writing – original draft, Visualization. **Paolo La Torraca:** Investigation, Writing – review & editing, Visualization.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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References

[1] M.T. Bohr, R.S. Chau, T. Ghani, K. Mistry, The high-k solution, IEEE Spectr. 44 (10) (October 2007) 25–35, https://doi.org/10.1109/MSPEC.2007.4337663.
[2] G. Moore, Cramming more components onto. Integrated circuits (reprint), Proc. IEEE 86 (1) (January 1998) 82–85, https://doi.org/10.1109/JPROC.1998.658762.
[3] R. Degraeve, T. Kauerauf, M. Cho, et al., Degradation and breakdown of 0.9 nm EOT SiO2/ALD HfO2/metal gate stacks under positive constant voltage stress, Proc. IEEE IEDM (Dec. 2005) 1–4, https://doi.org/10.1109/IEDM.2005.1609364.
[4] T. Nigam, A. Kerber, P. Peumans, Accurate model for time dependent dielectric breakdown of high-k metal gate stacks, in: Proc. IEEE Int. Rel. Phys. Symp., Apr. 2009, pp. 523–530, https://doi.org/10.1109/IRPS.2009.5173307.
[5] K. Okada, H. Ota, T. Nabatame, et al., Dielectric breakdown in high-k gate dielectrics—Mechanism and lifetime assessment, in: Proc. IEEE Int. Rel. Phys. Symp., Apr. 2007, pp. 36–43, https://doi.org/10.1109/RELPHY.2007.369865.
[6] E. Cartier, A. Kerber, Stress-induced leakage current and defect generation in nFETs with HfO2/TiN gate stacks during positive-bias temperature stress, in: Proc. IEEE Int. Rel. Phys. Symp., Apr. 2009, pp. 486–492, https://doi.org/10.1109/IRPS.2009.5173301.
[7] T. Fenfen, Y. Hong, T. Bo, T. Zhaoyun, X. Yefeng, X. Jing, W. Qingpu and Y. Jiang, “TDDB characteristic and breakdown mechanism of ultra-thin SiO2/HfO2 bilayer gate dielectrics,” J. Semicond. Vol. 35, no. 6, p. 064003. DOI: https://doi.org/10.1088/1674-4926/35/6/064003.
[8] G. Bersuker, D. Heh, C. Young, et al., Breakdown in the metal/highk gate-stack: Identifying the ‘weak link’ in the multilayer dielectric, in: Proc. IEEE IEDM, Dec. 2008, pp. 791–794, https://doi.org/10.1109/IEDM.2008.4796816.
[9] M. Porti, L. Aguilera, X. Blasco, et al., Reliability of SiO2 and high-k gate insulators: a nanoscale study with conductive atomic force microscopy, Microelectron. Eng. 84 (3) (Mar. 2007) 501–505, https://doi.org/10.1016/j.mee.2006.10.073.
[10] M. Rafik, G. Ribes, D. Roy, et al., SiO2 interfacial layer as the origin of the breakdown of high-k gate-stacks and progressive breakdown of ultrathin oxides, J. Vac. Sci. Technol. B 27 (Feb. 2009) 472–475, https://doi.org/10.1116/1.3077185.
[11] S. Tous, E.Y. Wu, E. Miranda, et al., A strong analogy between the dielectric breakdown of high-k gate-stacks and progressive breakdown of ultrathin oxides, J. Appl. Phys. 109 (12) (Jun. 2011), https://doi.org/10.1063/1.3592285, pp. 124115-1–124115-10.
[12] Do-Young Choi, Kyong Taek Lee, Chang-Ki Baek, Chang Woo Sohn, Hyun Chul Sagong, Eui-Young Jung, Jeong-Soo Lee, Interfacial-layer-driven dielectric degradation and breakdown of HfSiON/SiON gate dielectric nMOSFETs, IEEE Electron Device Lett. 32 (10) (October 2011) 1319–1321, https://doi.org/10.1109/LED.2011.2161861.
[13] N. Raghavan, K.L. Pey, K. Shubhakar, et al., Role of grain boundary percolative defects and localized trap generation on the reliability statistics of high-k gate dielectric stacks, in: Proc. IEEE IRPS, Apr. 2012, https://doi.org/10.1109/IRPS.2012.6241862, pp. 6A.1.1–6A.1.11.
[14] A. Padovani, N. Raghavan, L. Larcher, K.L. Pey, Identifying the first layer to fail in dual-layer SiOx/HfSiON gate dielectric stacks, IEEE Electr. Dev. Lett. 34 (10) (October 2013) 1289–1291, https://doi.org/10.1109/LED.2013.2275182.
[15] A. Padovani, L. Larcher, Time-dependent dielectric breakdown statistics in SiO2 and HfO2 dielectrics: insights from a multi-scale modeling approach, in: Proc. IEEE Int. Rel. Phys. Symp., March 2018, https://doi.org/10.1109/IRPS.2018.8353552.
[16] B.H. Lee, C. Kang, R. Choi, et al., Stress field analysis to understand the breakdown characteristics of stacked high-k dielectrics, Appl. Phys. Lett. 94 (16) (Apr. 2009), https://doi.org/10.1063/1.3122924, pp. 162904-1–162904-3.
[17] J.-F. Damelencourt, O. Renault, D. Samour, A.-M. Papon, C. Leroux, F. Martin, S. Marthon, M.-N. Séméria, X. Garros, Electrical and physico-chemical characterization of HfO_2/SiO_2 gate oxide stacks prepared by atomic layer deposition, Solid State Electron. 47 (10) (October 2023) 1613–1616, https://doi.org/10.1016/S0038-1101(03)00170-9.
[18] F. Giustino, P. Umari, A. Pasquarello, Dielectric effect of a thin SiO_2 interlayer at the interface between silicon and high-k oxides, Microelectron. Eng. 72 (1–4) (Apr 2004) 299–303, https://doi.org/10.1016/j.mee.2004.01.011.
[19] G. Bersuker, D. Heh, C.D. Young, L. Morassi, A. Padovani, L. Larcher, K.S. Yew, Y. C. Ong, D.S. Ang, K.L. Pey, W. Taylor, Mechanism of high-k dielectric-induced breakdown of the interfacial SiO2 layer, in: Proc. IEEE Int. Rel. Phys. Symp., May 2010, pp. 373–378, https://doi.org/10.1109/IRPS.2010.5488800.
[20] G. Bersuker, C.S. Park, J. Barnett, P.S. Lysaght, P.D. Kirsch, C.D. Young, R. Choi, B. H. Lee, B. Foran, K. van Benthem, S.J. Pennycook, P.M. Lenahan, J.T. Ryan, The effect of interfacial layer properties on the performance of Hf-based gate stack devices, J. Appl. Phys. 100 (12) (2006), 094108, https://doi.org/10.1063/1.2362905.
[21] D. Heh, C.D. Young, G.A. Brown, P.Y. Hung, A. Diebold, E.M. Vogel, J.B. Bernstein, G. Bersuker, Spatial distributions of trapping centers in HfO2/SiO2 gate stack, IEEE Transact. Electr. Dev. 54 (6) (June 2007) 1338–1345, https://doi.org/10.1109/TED.2007.896371.
[22] C.D. Young, Y. Zhao, D. Heh, R. Choi, B.H. Lee, Gennadi Bersuker, Pulsed id–vg methodology and its application to electron-trapping characterization and defect density profiling, IEEE Transact. Electr. Dev. 56 (6) (June 2009) 1322–1329, https://doi.org/10.1109/TED.2009.2019384.
[23] A. Padovani, L. Larcher, G. Bersuker, P. Pavan, Charge transport and degradation in HfO_2 and HfO_x dielectrics, IEEE Electr. Device Lett. 34 (5) (May 2013) 680–682, https://doi.org/10.1109/LED.2013.2251602.
[24] L. Vandelli, A. Padovani, L. Larcher, R.G. Southwick III, W.B. Knowlton, G. Bersuker, A physical model of the temperature dependence of the current through SiO_2/HfO_2 stacks, IEEE Trans. Electr. Dev. 58 (9) (2011) 2878–2887, https://doi.org/10.1109/TED.2011.2158825.
[25] Applied Materials Ginestra®. https://www.appliedmaterials.com/eu/en/semiconductor/19-software.html.
[26] J. Strand, L. Larcher, A. Padovani, P. La Torraca, A.L. Shluger, Dielectric breakdown in HfO2 dielectrics: using a multiscale modelling to identify the critical physical process involved in oxide degradation, J. Appl. Phys. 131 (2022), 234501, https://doi.org/10.1063/5.0083189.
[27] A. Padovani, L. Larcher, O. Pirrotta, L. Vandelli, G. Bersuker, Microscopic modeling of HfOx RRAM operations: from forming to switching, IEEE Transact. Electr. Dev. 62 (6) (2015) 1998–2006, https://doi.org/10.1109/TED.2015.2418114.
[28] A.K. Vijh, Inverse correlation between dielectric strength and dielectric constant for anodic oxides on valve metals, J. Mater. Sci. Lett. 7 (1988) 245–246, https://doi.org/10.1007/BF01730185.
[29] J. McPherson, J.-Y. Kim, A. Shanware, H. Mogul, J. Rodriguez, Trends in the ultimate breakdown strength of high dielectric-constant materials, IEEE Trans. Electr. Dev. 58 (8) (August 2003) 1771–1778, https://doi.org/10.1109/TED.2003.815141.
[30] J. McPherson, J.-Y. Kim, A. Shanware, H. Mogul, Thermochemical description of dielectric breakdown in high dielectric constant materials, Appl. Phys. Lett. 82 (13) (March 2003) 2121–2123, https://doi.org/10.1063/1.1565180.
[31] G. Richard, I.I.I. Southwick, Mark C. Elgin, Gennadi Bersuker, Rino Choi, William B. Knowlton, Preliminary study of the breakdown strength of TiN/HfO2/SiO2/Si MOS gate stacks, in: International Integrated Reliability Workshop (IIRW), 2006, pp. 146–147, https://doi.org/10.1109/IRWS.2006.305231.
[32] J.W. McPherson, H.C. Mogul, Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO_2 thin films, J. Appl. Phys. 84 (3) (1998) 1513–1523, https://doi.org/10.1063/1.368217.

[33] G. Bersuker, Y. Jeon, H.R. Huff, Degradation of thin oxides during electrical stress, Microelectron. Reliab. 41 (12) (December 2001) 1923–1931, https://doi.org/10.1016/S0026-2714(01)00120-2.

[34] A. Padovani, B. Kaczer, M. Pešic, A. Belmonte, M. Popovici, L. Nyns, D. Linten, V. V. Afanas'ev, I. Shlyakhov, Y. Lee, H. Park, L. Larcher, A sensitivity map-based approach to profile defects in MIM capacitors from I−V, C−V, and G−V measurements, IEEE Transact. Electr. Dev. 66 (4) (April 2019) 1892–1898, https://doi.org/10.1109/TED.2019.2900030.

[35] A. Padovani, D.Z. Gao, A.L. Shluger, L. Larcher, A microscopic mechanisms of dielectric breakdown in SiO2 films: an insight from multi-scale modeling, J. Appl. Phys. 121 (2017), 155101, https://doi.org/10.1063/1.4979915.

[36] Andrea Padovani, Paolo La Torraca, Jack Strand, Valerio Milo, Luca Larcher, Towards a universal model of dielectric breakdown, in: IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 28-30 March 2023, 2023, https://doi.org/10.1109/IRPS48203.2023.10117846.

[37] K. Huang, A. Rhys, Theory of light absorption and non-radiative transition in F-centres, Proc. R. Soc. Lond. 204A (1950) 406–423, https://doi.org/10.1098/rspa.1950.0184.

[38] C.H. Henry, D.V. Lang, Non radiative capture and recombination by multiphonon emission in GaAs and GaP, Phys. Rev. B 15 (2) (1977) 989–1016, https://doi.org/10.1103/PhysRevB.15.989.

[39] M. Zhang, Z. Huo, Z. Yu, J. Liu, M. Liu, Unification of three multiphonon trap-assisted tunneling mechanisms, J. Appl. Phys. 110 (2011), 114108, https://doi.org/10.1063/1.3662195.

[40] P. La Torraca, F. Caruso, A. Padovani, G. Tallarida, S. Spiga, L. Larcher, Atomic defects profiling and reliability of amorphous Al2O3 metal–insulator–metal stacks, IEEE Transact. Electr. Dev. 69 (7) (July 2022) 3884–3891, https://doi.org/10.1109/TED.2022.3172928.

[41] D.T. Gillespie, A general method for numerically simulating the stochastic time evolution of coupled chemical reactions, J. Comput. Phys. 22 (4) (1976) 403–434, https://doi.org/10.1016/0021-9991(76)90041-3.

[42] R. Karthik, D. Kannadassan, M.S. Baghini, P.S. Mallick, Nanostructured bilayer anodic TiO_2/Al_2O_3 metal-insulator-metal capacitor, J. Nanosci. Nanotechnol. 13 (10) (October 2013), https://doi.org/10.1166/jnn.2013.7767, pp. 6894-6899(6).

[43] F. Zahoor, T.Z.A. Zulkifli, F.A. Khanday, Resistive random access memory (RRAM): an overview of materials, switching mechanism, performance, multilevel cell (mlc) storage, modeling, and applications, Nanoscale Res. Lett. 15 (2020) 90, https://doi.org/10.1186/s11671-020-03299-9.

[44] A. Mikhaylov, et al., Multilayer metal-oxide Memristive device with stabilized resistive switching, Adv. Mater. Technol. 5 (2020) 1900607, https://doi.org/10.1002/admt.201900607.

[45] Mouhamad Alayan, Elisa Vianello, Barbara de Salvo, Luca Perniola, Andrea Padovani, Luca Larcher, Correlated effects on forming and retention of Al doping in HfO2-based RRAM, IEEE Design& Test 34 (3) (June 2017) 23–30, https://doi.org/10.1109/MDAT.2017.2682246.

[46] W.-J. Qi, R. Nieh, R. Onishi, B.H. Lee, L. Kang, Y. Jeon, S. Gopalan, J.C. Lee, Temperature effect on the reliability of ZrO/sub 2/ gate dielectric deposited directly on silicon, in: IEEE International Reliability Physics Symposium (IRPS), San jose, CA, USA, 10-13 April 2010, 2010, https://doi.org/10.1109/RELPHY.2000.843893.

[47] S.W. Chang, C.L. Chen, C. J. W, Kenneth Wu, A new TDDB lifetime bi-model for eDRAM MIM capacitor with ZrO2 high-k dielectrics, in: 15th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, 07-11 July 2008, 2008, https://doi.org/10.1109/IPFA.2008.4588196.