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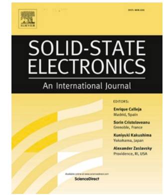

High-k/InGaAs interface defects at cryogenic temperature

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ABSTRACT

Oxide defects in the high-k/InGaAs MOS system are investigated. The behaviour of these traps is explored from room temperature down to 10 K. This study reveals that the exchange of free carriers between oxide states and either the conduction or the valence band is strongly temperature dependant. The capture and emission of electrons is strongly suppressed at 10 K as demonstrated by the collapse of the capacitance frequency dispersion in accumulation for n-InGaAs MOS devices, though hysteresis in the C-V sweeps is still present at 10 K. Phonon assisted tunnelling processes are considered in the simulation of electrical characteristics. The simulated data match very well the experimental characteristics and provide energy and spatial mapping of oxide defects. The multi phonon theory also help explain the impedance data temperature dependence. This study also reveals an asymmetry in the free carrier trapping between n and p type devices, where hole trapping is more significant at 10 K.

1. Introduction

In MOS devices, defects at the oxide/semiconductor interface, and within the oxide, affect device operation in different ways e.g. degradation of the subthreshold slope, 1/f noise, hysteresis or Vt instability [1]. However, the behaviour of these defects at cryogenic temperature is less well understood. Electron-defect interactions at cryogenic temperatures could affect CMOS qubits. In the silicon qubit implementation, the spin encoding quantum dot uses a dielectric gate which could induce charge noise and reduce the coherence time [2]. In addition, the introduction of III-V MOS devices for qubits readout and control circuitry (amplifiers, multiplexers) and operating at cryogenic temperature close to the qubit stage present significant advantages in terms of power dissipation [3,4]. Therefore it is important to understand the electron-oxide defect interactions at cryogenic temperature in the high-k/III-V and other semiconductor systems.

This work provides more insight into the nature of interfacial and oxide defects in the high-k/InGaAs MOS system by exploring their capture and emission properties at different temperatures. We investigate these properties through the dispersion of the capacitance and conductance with frequency and the hysteresis observed in capacitance voltage (C-V) sweeps from room temperature (RT) down to 10 K. The approach adopted relies on comparing the MOS device experimental impedance measurements to the physics based simulated characteristics at different temperatures.

2. Experimental details and simulation framework

2 µm n-type (S at 4×10^{17} cm^{-3}) and p-type (Zn at 4×10^{17} cm^{-3}) $In_{0.53}Ga_{0.47}As$ epitaxial layers were grown by metalorganic vapour-phase epitaxy (MOVPE) on n-doped and p-doped InP (1 0 0) substrates, respectively. The InGaAs surface was treated in 10% $(NH_4)_2S$ passivation and then transferred to the atomic layer deposition (ALD) chamber within a minimum time (~3 min) [5]. 8 nm of Al_2O_3 or 8 nm HfO_2 were nominally deposited by ALD on the InGaAs surface at 300 °C and 250 °C, respectively. The Al_2O_3 thickness determined by TEM was 6 nm [6]. Details of the ALD process can be found in [7]. The Au(90 nm)/Ni(70 nm) metal gate was formed by e-beam evaporation and a lift-off process. The MOS capacitors received a post-metal FGA (5% H_2/95 % N_2) at 300 °C for 30 min. The impedance measurements were carried out in a

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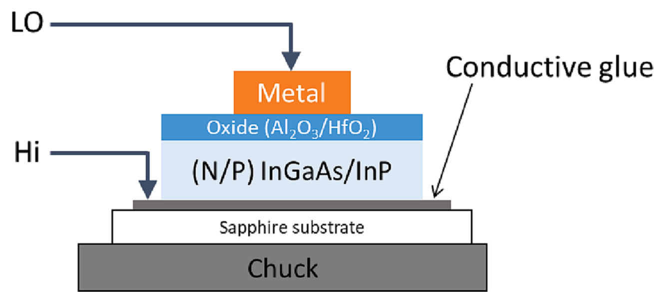

Fig. 1. MOS test structure and setup configuration for cryogenic impedance measurements.

cryogenic probe station using a Keysight E4980 LCR meter or a 4294A impedance analyzer in the configuration shown in Fig. 1.

Device simulations are performed using the defect-centric Ginestra® simulation platform [8], which relies on a kinetic Monte-Carlo engine and a solid physical description of carriers' transport and interactions with electrically active defects [9]. Trapping and trap-assisted transport mechanisms are described in the framework of the multi-phonon theory [10], tightly linked to the atomistic structure of material defects. Ginestra® provides an extremely stable solution at very low-temperatures (10 K and below [11]), as the ones considered in this study.

3. Results and discussion

Fig. 2 shows the experimental C-V characteristics measured on the considered devices at room temperature (RT) and at 10 K. For Au/Ni/Al_2O_3/n-InGaAs/InP MOS stacks, the frequency dispersion exhibited by the C-V characteristic at RT (Fig. 2a) shows a collapse throughout the full voltage range at 10 K (Fig. 2b). A similar frequency dispersion is clearly visible for the Au/Ni/Al_2O_3/p-InGaAs/InP MOS stacks at RT (Fig. 2c), collapsing only in the inversion region at 10 K (Fig. 2d). The similar inversion behaviour of the n-doped and the p-doped stacks at 10 K is well explained by a reduction of the supply rate of minority carriers (either thermally generated through defects in the InGaAs depletion region or diffusing from the neutral region) to such an extent they are no longer able to respond to the fast dynamics of the measurement AC signal. The different accumulation behaviours exhibited at 10 K suggest a different interaction of the carrier in the InGaAs with the Al_2O_3 defects. While the absence of frequency dispersion shown in the n-doped stacks is consistent with the phonon assisted tunnelling of free carriers from the InGaAs conduction band to defects in oxide as described in [12], the significant frequency dispersion present at 10 K for p-doped stacks indicates hole trapping by defects in the Al_2O_3, with time constants in the range 1 ms to 1 us, is still important even at such low temperature.

Fig. 3 shows the experimental C-V and G-V characteristic measured on the considered devices at 300 K and 223 K and the simulations results obtained by using Ginestra®. The experimental results were used for profiling the defect energy and spatial distribution across the Al_2O_3 thickness via the Ginestra® Defect Spectroscopy tool. The defect

Fig. 2. Multi frequency C-V a) measured at room temperature and b) measured at 10 K on Au/Ni/Al_2O_3/n-InGaAs/InP capacitors from 1 kHz up to 1 MHz. c) and d) Au/Ni/Al_2O_3/p-InGaAs/InP C-V characteristics measured at room temperature and 10 K, respectively. Measurement frequency from 100 Hz up to 1 MHz.

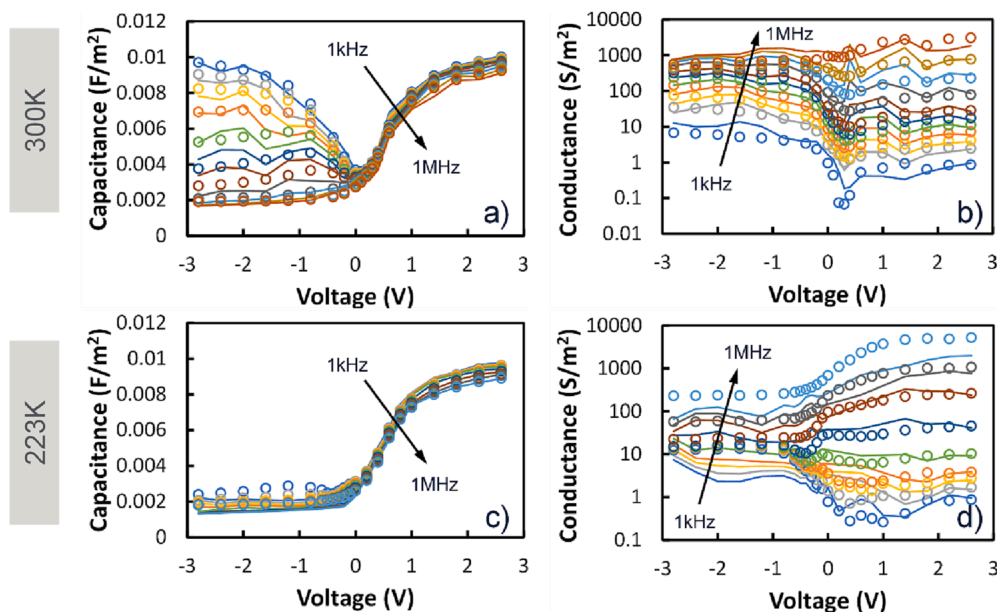

Fig. 3. Experimental (circles) and simulated (lines) multi-frequency C-V characteristics for Au/Ni/Al_2O_3/n-InGaAs/InP a) at RT and c) at −50 °C. b) and d) are the corresponding G-V curves. Measurement frequency: 1 kHz-1 MHz.

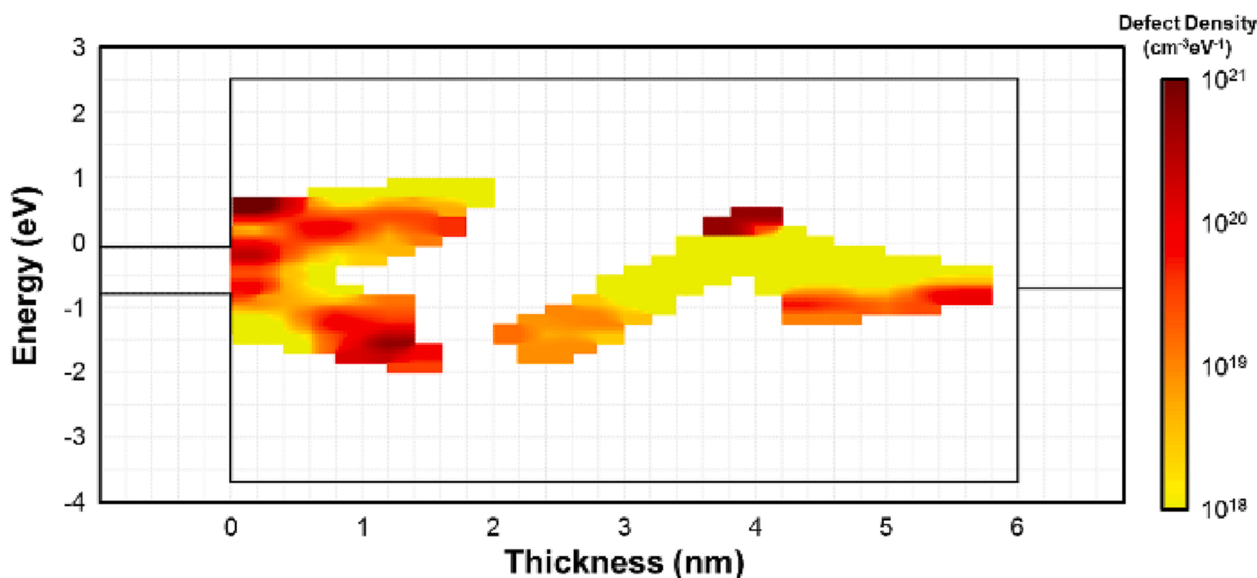

Fig. 4. Defect density distribution in energy and space extracted from the experimental data of Fig. 3. The defect relaxation energy used in the simulation was 1 eV.

relaxation energy used in the simulation was 1 eV. The resulting defect distribution, shown in Fig. 4, is characterized by energy levels consistent with previous results extracted from I to V curve fitting of Al_2O_3 MIMs [13,14]. The resulting C-V and G-V simulations show excellent agreement with the experimental results. This approach enables defect mapping and demonstrates that at the considered conditions (temperatures and measurement frequency) the defects present across the full thickness of the oxide are electrically active and can capture and emit free carriers.

A hysteresis window is observed in the C-V sweep characteristics when the charge trapped in the oxide during the sweep into accumulation is not fully recovered during the reverse sweep.

The hysteresis measured in the C-V sweeps at room temperature is also present at 10 K (Fig. 5). It is interesting to note that, for a given voltage sweep range (−2.5 V to 2.5 V), the hysteresis curve is repeatable and that identical successive hysteresis C-V sweeps were recorder at 10 K (not shown) demonstrating that the trapped charge can be recovered even with very limited thermal energy at 10 K. It is also interesting to note that at the 10 K the capacitance frequency dispersion in accumulation on the n-InGaAs MOS capacitors is fully suppressed while the hysteresis is still present. This observation highlights the role of the field across the oxide in controlling the dynamics of capture and emission of free careers by oxide traps and the measurement time scale (seconds for the hysteresis voltage sweep vs milliseconds for the slowest measurement frequency for the capacitance dispersion). Furthermore, the hysteresis window measured at 10 K is wider than at room temperature, possibly highlighting the hindered charge de-trapping at 10 K as compared to room temperature.

C-V hysteresis simulations (Fig. 6) performed considering the defect distribution in Fig. 4 are in good qualitative agreement with the measurements (Fig. 5) and reproduce well the main experimental features.

First of all, they confirm that the hysteresis is present even at

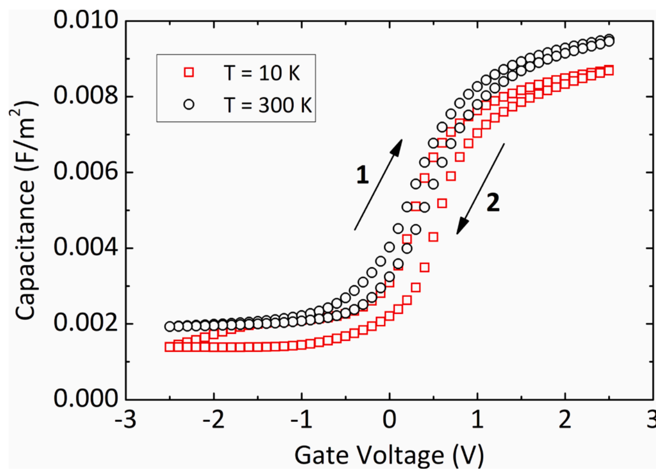

Fig. 5. Measured C-V hysteresis at RT and 10 K for the Au/Ni/Al_2O_3/n-InGaAs/InP MOS capacitor. Measurement frequency: 1 MHz.

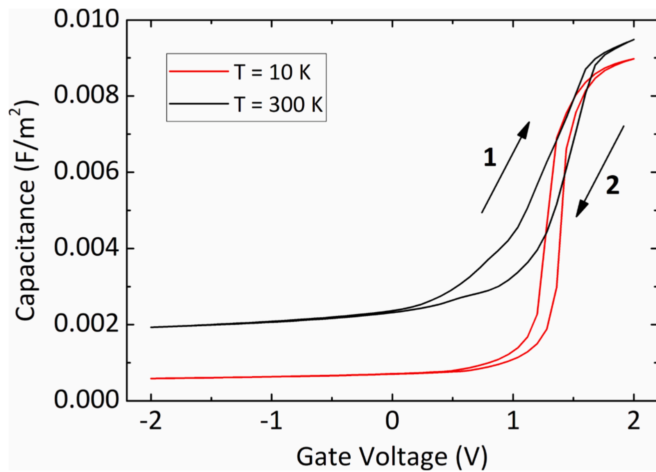

Fig. 6. Simulated CV hysteresis at RT and 10 K for the Au/Ni/Al_2O_3/n-InGaAs/InP MOS capacitor.

cryogenic temperatures, due to the on-set of the nuclear tunneling phenomena (included in the multi-phonon theory) [10,15] that enables and sustains efficient carriers trapping and de-trapping even at extremely low temperatures (contrarily to what generally believed – and hoped for – by the quantum computing community). Simulations also reproduce other noticeable features at low T (vs. RT): reduction of accumulation capacitance, steeper depletion-to-accumulation transition, reduction of the depletion capacitance (due to the much less efficient doping ionization).

Regarding the quantitative mismatch between the experimental and simulated C-V hysteresis, it is important to note that the transient simulation is done using a voltage ramp while for the experimental C-V hysteresis sweep the voltage is incrementally stepped with different time scales from the simulation. Despite these differences, the simulation hysteresis results confirm the experimental observations and provide further insight into oxide defects.

4. Conclusion

We used experiments and simulations to analyse the impedance of the high-k/InGaAs MOS system at cryogenic temperature. The combined approach is first used to profile the space and energy distributions of interface and oxide traps in the considered Au/Ni/Al_2O_3/n-InGaAs/InP MOS capacitor, and then to interpret the hysteretic behaviour exhibited by measured C-V sweep characteristics even at cryogenic temperatures. Results clearly show that, contrarily to what generally believed, oxide traps can efficiently trap and de-trap carriers even at extremely low temperatures, which well explains the persistence of the CV hysteresis down to 10 K.

Unlike standard (experimental) characterisation techniques, the proposed approach provides valuable insights on the behaviour and origin of interface and oxide traps that can be used to understand and predict device behaviour and reliability at cryogenic temperatures.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgement

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References

[1] Fleetwood DM. IEEE International Reliability Physics Symposium. Monterey, USA 2019;2019:1–10.
[2] Maurand R, et al. Nat Commun 2016;7:13575.
[3] Södergren L, et al. Nano Lett 2022;22:3884–8.
[4] Ram MS, et al. IEEE EDL 2022;43:2033–6.
[5] O'Connor E, et al. J Appl Phys 2011;109:024101.
[6] Caruso E, et al. EUROSOI 2018:1–4.
[7] Lin J, et al. Microelectr Eng 2017;78:204–8.
[8] https://www.appliedmaterials.com/eu/en/semiconductor/ginestra-software.html.
[9] Padovani A, et al. IEEE TED 2019;66:1892–8.
[10] Vandelli L, et al. IEEE TED 2011;58:2878–87.
[11] Bellentani L, et al. Phys Rev Appl 2021;16:054034.
[12] Caruso E, et al. IEEE TED 2020;67:4372–8.
[13] La Torraca P, et al. IEEE EDL 2020;42:220–3.
[14] La Torraca P, et al. IEEE TED 2022;69:3884–91.
[15] Michl J, et al. IEEE TED 2021;68:6365–71.