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Materials Design Principles for Large Memory Windows: Coercive Voltage Engineering in Ferroelectric– Dielectric Heterostructures

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ABSTRACT

The integration of dielectric inserts into hafnia-based ferroelectric stacks has emerged as a promising route to expand memory windows in ferroelectric NAND. However, the physical origin of the associated coercive voltage enhancement has remained unclear. Here, we resolve this long-standing question by demonstrating that coercive voltage enhancement originates from resistive voltage division between the ferroelectric and dielectric layers, governed primarily by leakage in both layers. Combining Preisach modeling, defect-based Ginestra simulations, and polarization switching experiments with external leaky dielectrics, we show that minimizing leakage in the dielectric layer - intrinsically through wide-bandgap, low-electron-affinity dielectrics or extrinsically by reducing defect densities - provides a universal design principle for coercive voltage control. Importantly, nucleation-limited switching kinetics remain unchanged across the heterostructures, confirming that the enhancement is driven by resistive voltage division rather than trap-assisted mechanisms. This discovery establishes a straightforward framework for engineering large memory windows using ferroelectric–dielectric heterostructures, thereby enabling multi-level (TLC/QLC) operation in 3D NAND. Beyond memory applications, our findings also explain the contrasting behaviors of fluorite- vs. perovskite-based ferroelectric–dielectric systems, offering fundamental guidance for interfacial materials design in next-generation electronic devices.

1 | Introduction

Charge-trap flash (CTF) NAND technology, while central to non-volatile memory, faces significant scaling challenges, particularly in terms of retention and endurance at reduced z-pitches. As NAND arrays continue to scale, issues such as lateral charge migration become more pronounced, further limiting performance [1]. Ferroelectric (FE)-NAND has emerged as a potential

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alternative to charge-trap flash due to its scalability, higher operating speeds, and low operating voltages. FE-NAND operates by storing information in the bound spontaneous polarization of the ferroelectric layer that can be modulated by the application of an electric field. Due to the bound nature of polarization rather than trapped charges in the case of CTF NAND, FE NAND is expected to be immune to lateral charge migration and enable further z-scaling for 3D NAND applications (Figure 1a).

However, the memory window (MW) in standard ferroelectric field-effect transistors (FEFETs) is limited by the coercive voltage (V_C) of the ferroelectric layer. Given that hafnia-based ferroelectrics, with a coercive field of 0.5–1 MV/cm, are the most common CMOS compatible class of ferroelectrics, the MW is limited to 4 V at 3D NAND compatible thicknesses (20 nm). This is far below the requirements for higher logic operation (TLC and QLC) that are implemented in state-of-the-art 3D NAND arrays. Further, the complex interplay between charge trapping in the channel interlayer (IL) and polarization switching limits the realistic MW of FEFETs to 50–60% of $2V_C$ [2].

It was shown that inserting a dielectric (DE) layer into a hafnia-based ferroelectric gate stack could increase the MW multifold [3–9]. This development gives FE devices the needed MW boost at 3D NAND compatible gate stack thicknesses and low write voltages. As seen in Figure 1b, this dielectric insert can be either on top of the FE stack (Gate Blocking Layer, GBL) or in the middle of the FE layer (Tunnel Dielectric Layer, TDL). A benchmark of the memory windows of these engineered FEFETs, shown in Figure 1c, summarizes the increased MW achieved by inserting dielectric layers into the ferroelectric gate stack. While it is known that the increase in MW is strongly coupled with an increase in the coercive voltage of the engineered ferroelectric gate stack, the mechanism behind this increase remains unclear [2].

One proposed theory states that, in the TDL configuration, the trapped charges between the dielectric and ferroelectric layers form an artificial dipole across the dielectric layer, thereby enhancing the MW [3, 10]. Another theory proposes that there is gate side charge injection, resulting in charge trapping between the GBL and ferroelectric layer [4]. Both these theories rely on charge trapping at the ferroelectric–dielectric interface. Device simulations to support these theories reveal that high trap densities at the FE-DE interfaces have to be assumed to simulate the observed increase in MW [11].

While relatively unexplored in FEFETs, metal-insulator-metal (MIM) capacitors with ferroelectric–dielectric heterostructures have been widely studied especially in the context of negative capacitance. It is worth noting that the addition of a dielectric layer leads to increasing coercive voltage in fluorite-structure ferroelectrics, but in perovskite-type ferroelectric based heterostructures, the addition of the dielectric layer has been associated with lowering of the coercive voltage and has been leveraged for stabilizing negative capacitance [12]. This contrasting behavior points to a fundamental difference in the nature of ferroelectric–dielectric interfaces and switching physics between the two material classes [13]. In perovskite systems, ferroelectric–dielectric heterostructures are governed primarily by Landau–Ginzburg thermodynamics and electrostatic coupling between the ferroelectric and dielectric layers [14, 15].

Against this backdrop, several mechanisms have been proposed to explain the increase in coercive voltage specifically in fluorite-structure ferroelectrics, including leakage-assisted polarization switching [16], negative capacitance [17], charge injection [18], and multi-domain effects [19]. The understanding of negative capacitance and multi-domain effects in fluorite-structure ferroelectrics has evolved since these reports [13, 20, 21]. The leakage assisted polarization switching model in these heterostructures neither directly addresses the coercive field enhancement nor explains the behavior at large dielectric thicknesses. Additionally, the behavior of these heterostructures at higher voltages, where there might be full polarization switching is unclear. Importantly, none of these models consistently explains the enhancement of coercive voltage in TDL based heterostructures, where the insertion of the dielectric in the middle of the ferroelectric gate stack eliminates the possibility of gate side injection and dielectric leakage assisted polarization switching.

In this work, we show that the mechanism behind the increase in V_C is directly linked to the leakage in the dielectric and ferroelectric layers. Using Preisach model based simulations and experiments with external leaky capacitors, we demonstrate increasing coercive voltage with decreasing leakage through the dielectric layer. Further, we attribute the increase in coercive voltage to resistive voltage division between the ferroelectric and dielectric layers. Following that, we explore the design space using a comprehensive model of the heterostructure in Ginestra, a defect-based modeling platform [22] and confirm the trends by benchmarking the coercive voltage of MIMs and memory window of FEFETs with ferroelectric–dielectric heterostructures. Finally, we perform polarization switching measurements and model the switching dynamics with a nucleation-limited switching (NLS) model to demonstrate similar switching kinetics across stand-alone ferroelectrics and ferroelectric–dielectric heterostructures, which supports a voltage division origin of coercive voltage enhancement rather than charge trapping.

2 | Results and Discussions

2.1 | Coercive Voltage Enhancement in Ferroelectric–Dielectric Heterostructures

Metal-insulator-metal capacitors with a standard ferroelectric (19 nm HZO) and ferroelectric–dielectric heterostructures with a tunnel dielectric layer (9.5 nm HZO/ 1 nm Al_2O_3/ 9.5 nm HZO and 8.5 nm HZO/ 3 nm Al_2O_3/ 8.5 nm HZO) and a gate blocking layer (19 nm HZO/ 1 nm Al_2O_3) were fabricated as outlined in Figure S1. The transmission electron micrographs (TEM) in Figure 2 confirm the insertion of the dielectrics in the heterostructures.

The polarization-voltage (P–V) characteristics measured at 1 kHz show a coercive voltage window ($2V_C$) of 3.9 V for the standard 19 nm HZO capacitor. The capacitance–voltage (C–V) characteristics shows the butterfly shaped C–V loops with a dielectric constant close to 40. The insertion of an 1 nm Al_2O_3 layer, both at the top and in the middle of the ferroelectric layer is demonstrated to increase the coercive voltage window ($2V_C$) up to 7.67 and

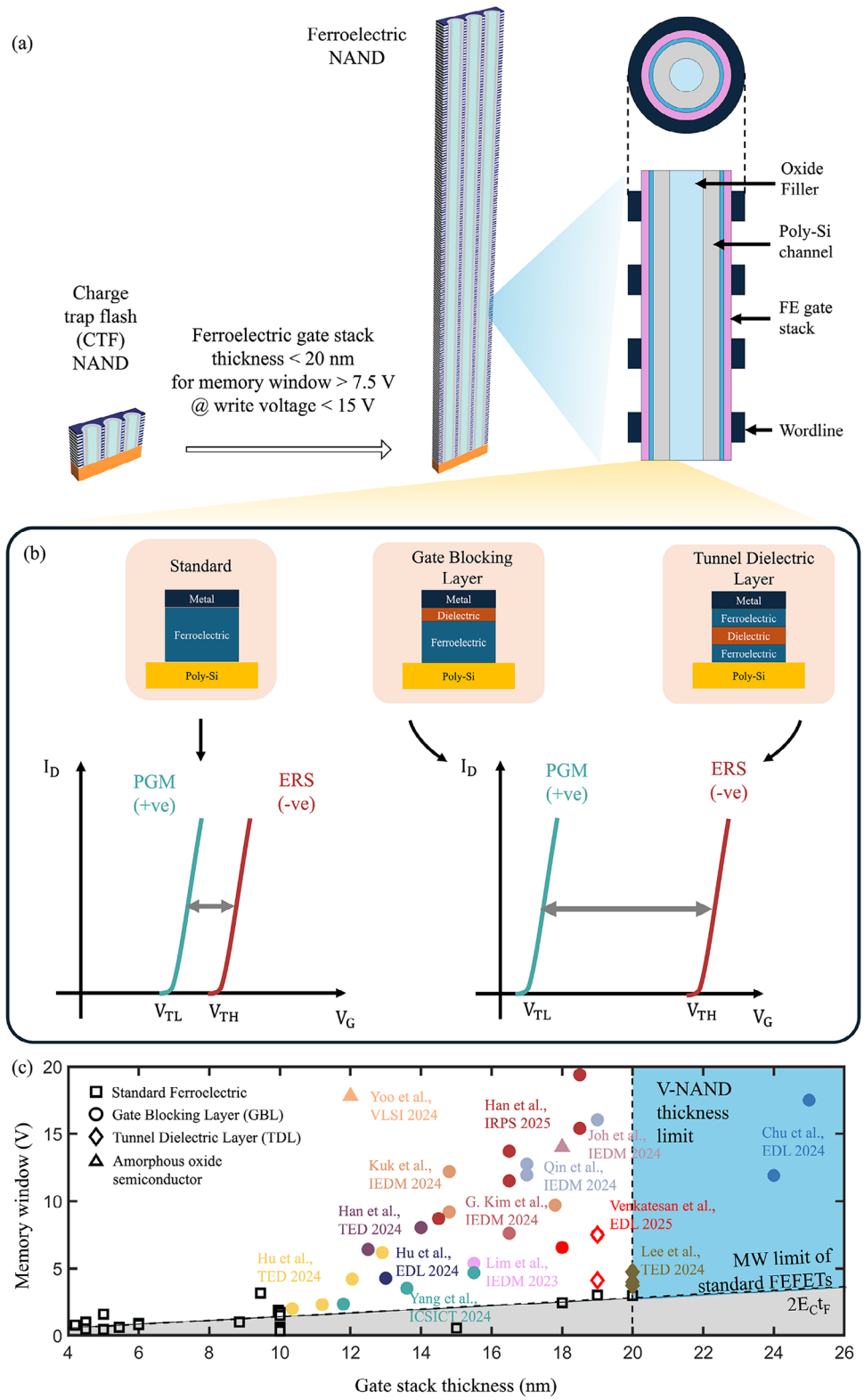

FIGURE 1 | (a) Ferroelectrics have emerged as potential alternatives to replace the charge trap layer in 3D NAND devices to enable continued z-scaling. However their memory window (MW) is limited by the coercive voltage of the ferroelectric layer. (b) Dielectric inserts in ferroelectric gate stacks lead to an enhanced coercive voltage window ($2V_C$), thereby enabling large memory window operation. There are two common types of dielectric inserts: Tunnel Dielectric Layer (TDL), where the dielectric is inserted in the middle of the gate stack, and Gate blocking layer (GBL), where the dielectric is inserted next to the gate/top electrode. (c) A benchmark of the memory windows of the FEFETs with different ferroelectric gate stacks with dielectric inserts showing up to 5× improvement in memory window over the standard FEFETs.

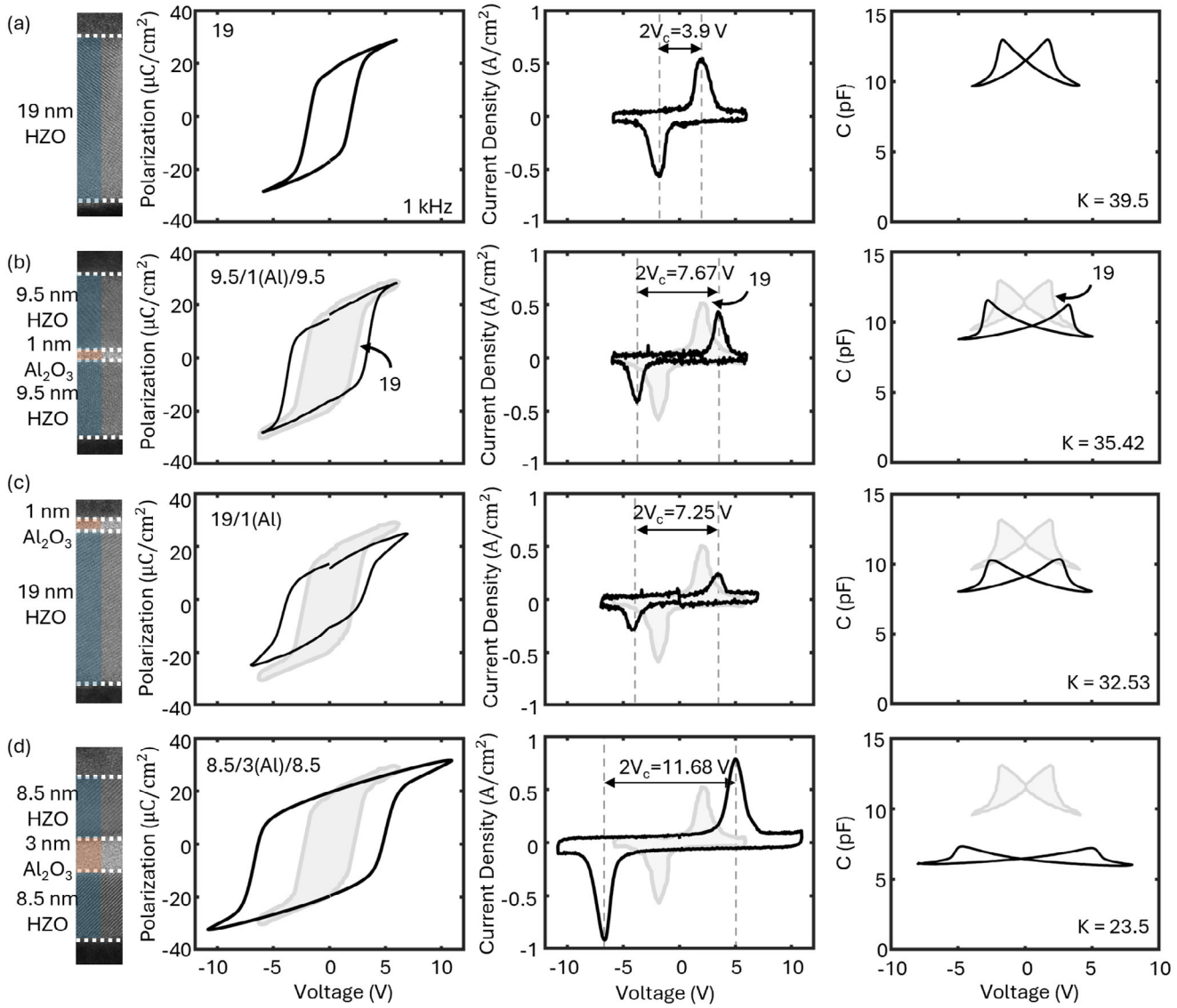

FIGURE 2 | The polarization-voltage characteristics, corresponding switching current, and capacitance-voltage characteristics are shown for reference (a) HZO (19 nm), (b) TDL: 9.5 nm/ 1 nm(Al)/9.5 nm and (c) 8.5 nm/ 3 nm(Al)/8.5 nm and (d) GBL: 19 nm/ 1 nm(Al) capacitors with W electrodes. The insertion of dielectric is shown to enhance the coercive voltage window $2V_C$ over the references 19 nm HZO. Additionally, the $2V_C$ of the GBL 19/1(Al) and TDL 9.5/1(Al)/9.5 gate stacks with the same FE and DE thickness is shown to be comparable, indicating that the position of the dielectric has minimal impact on the V_C enhancement.

7.25 V, respectively (Figure 2b,c). This, alongside the comparable dielectric constants indicates that the location of the dielectric has minimal influence on the coercive voltage enhancement.

Increasing the dielectric thickness to 3 nm, as in 8.5/3(Al)/8.5, further confirms the coercive voltage enhancement from the insertion of the dielectric, exhibiting a coercive voltage window of 11.68 V (Figure 2d).

2.2 | Modeling Leaky Ferroelectric–Dielectric Heterostructures

Leaky ferroelectric heterostructures can be modeled as shown in Figure 3 and Figure S2a where the FE-DE interface is modeled using a non-linear capacitor C_{int} [23]. In the case of an ideal FE-DE interface, the capacitors and leakage paths are independent and parallel to each other, and the potential at the FE-DE interface is determined by capacitive division. However, such a model does not explain the enhanced V_C in FE-DE heterostructures. Nominally, the interface capacitor captures the charge trapping due to band alignment issues and trap states. As long as, $C_{int} > 2C_{FE}$, the interface can be approximated as an equipotential surface similar to having an internal metallic layer at the FE-DE interfaces. We experimentally confirmed the accuracy of this model by fabricating a 8.5/3(Al)/8.5 heterostructure intercalated with TiN metal layers. The P–V and C–V characteristics are found to be similar to that of the 8.5/3(Al)/8.5 heterostructure with no intercalation (Figure S3).

In order to understand the origin of this coercive voltage enhancement, we model the heterostructures as individual leaky

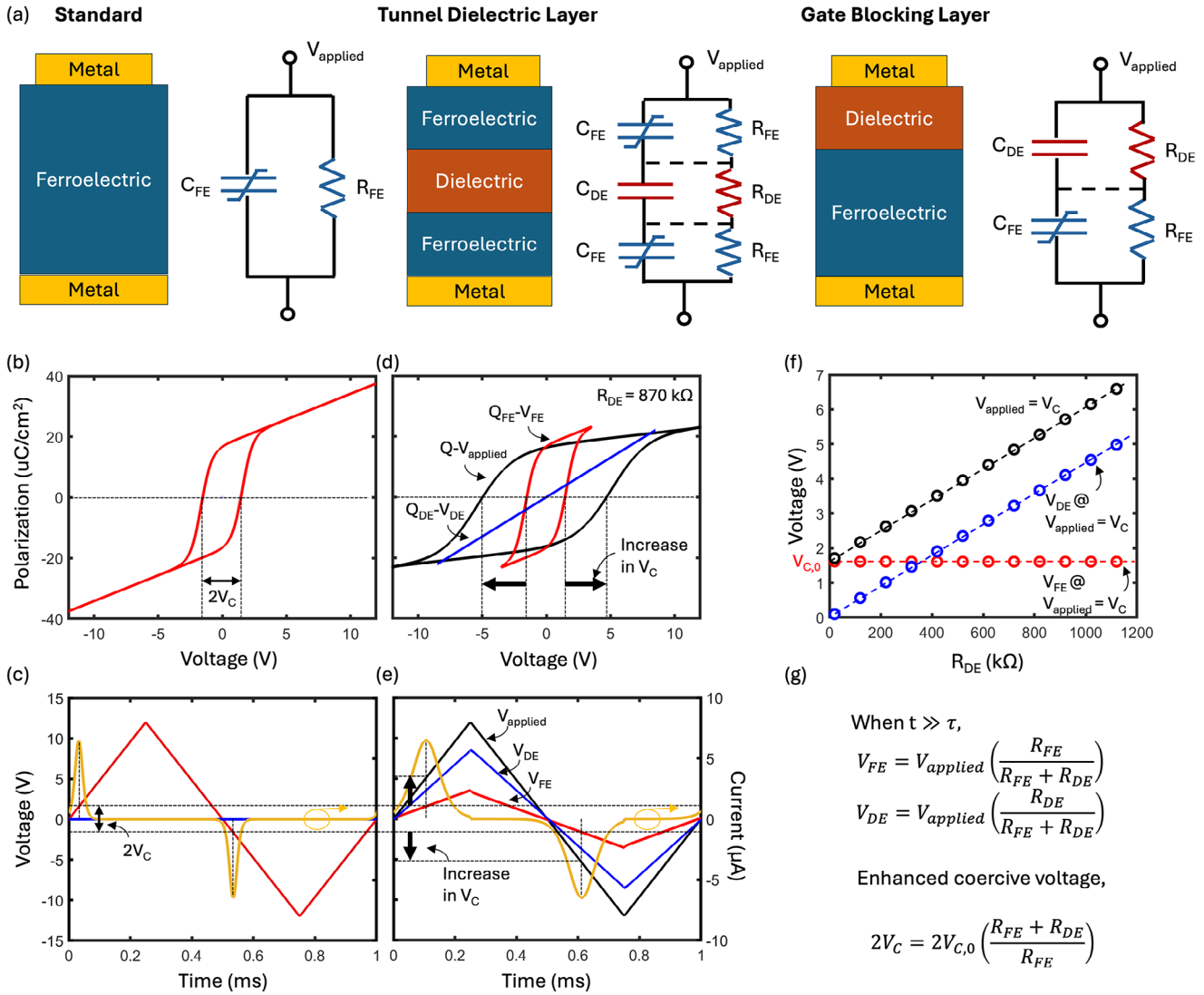

FIGURE 3 | (a) The capacitor gate stacks with the standard and FE-DE heterostructures (TDL and GBL) along side their equivalent circuit model where a parallel resistor is used to simulate leakage through these layers. Simulated P–V characteristics of (b) stand-alone 17 nm HZO and (d) leaky FE-DE heterostructure with R_{DE} = 870 kΩ, R_{FE} = 350 kΩ and C_{DE} equivalent to that of a 3 nm Al_2O_3 layer. The heterostructure exhibits more than twice the coercive voltage of the standalone HZO. The voltage across different layers and the switching current for both cases are shown in (c) and (e), respectively. It is observed that the voltage division between the ferroelectric and dielectric layers are governed by the leakage resistors. (f) Evolution of the effective coercive voltage (V_C) and the voltage across the FE and DE layers when $V_{applied} = V_C$, showing that the FE switches when the field across the FE equals the intrinsic coercive voltage $V_{C,0}$ and the enhancement in the effective coercive voltage arises from the voltage drop across the dielectric layer. (g) The equations governing the resistive voltage division between the two layers and an expression for the effective coercive voltage window ($2V_C$).

capacitors connected in series. The ferroelectric characteristics are modeled using the Preisach model and a resistor (R_{FE}) is introduced in parallel to simulate leakage. The dielectric insert is modeled similarly as a linear capacitor (C_{DE}) with a leakage resistor (R_{DE}) in parallel, see Figure 3a. Figure 3b,d shows the P–V and switching current characteristics of the standalone ferroelectric layer (extracted from a 17 nm HZO MIM capacitor) with R_{FE} = 350 kΩ simulated using the Preisach model. The leaky dielectric layer with a 3 nm Al_2O_3 is simulated with leakage resistor of R_{DE} = 870 kΩ. The simulated P–V loop shows the enhanced coercive voltage. The components of voltage across the ferroelectric (V_{FE}) and the dielectric (V_{DE}) layer are shown in Figure 3f. It is observed that the increased coercive voltage originates as a result of the voltage division between the FE and DE layer. The linear nature of voltage division across the layers indicates the resistive nature of the voltage division. This is in line with the analytical solutions for the circuit, which suggest that for $t >> \tau$, the voltage division is largely governed by the leakage resistors. Here $\tau = RC$ is the time constant of the circuit. Thus, the voltage across the ferroelectric and dielectric layers can be approximated as $V_{FE} = (R_{FE}/(R_{DE}+R_{FE}))\cdot V_{applied}$ and $V_{DE} = (R_{DE}/(R_{DE}+R_{FE}))\cdot V_{applied}$, respectively. Hence, the effective coercive voltage of the heterostructure is given by,

$$V_C = \left(1 + \frac{R_{DE}}{R_{FE}}\right)\cdot V_{C,0} \quad (1)$$

where $V_{C,0}$ is the intrinsic coercive voltage of the standalone ferroelectric layer. This is confirmed from the components of the effective coercive voltage, V_C, plotted in Figure 3e.

To validate this model experimentally, we externally connected leaky dielectrics to 17 and 19 nm HZO capacitors (Figure 4a). These thicknesses were chosen to be equal to the total ferroelectric thicknesses in the FE-DE heterostructures used in this study. The leaky dielectric capacitors were emulated using ceramic capacitors with capacitance corresponding to 1 and 3 nm Al_2O_3 layers in parallel with resistors. The resistance, equivalent to R_{DE}, was varied from tens to hundreds of kΩ. It is observed that the coercive voltage increases as R_{DE} is increased, similar to the prediction from the model. Figure 4b shows the simulated P–V loops with different R_{DE} based on Preisach model parameters extracted from 19 and 17 nm HZO P–V loops. Figure 4c shows the experimentally measured P–V loops for the corresponding R_{DE} showing a close match of coercive voltages with the simulation. This is further confirmed in Figure 4d, where the experimentally measured coercive voltage windows at different R_{DE} are in close agreement with those from simulations. This further confirms that less leaky dielectrics lead to increased coercive voltage enhancement. Importantly, this enables us to provide an approximate expression for the effective coercive voltage window, $2V_C = (1 + R_{DE}/R_{FE}) \cdot 2V_{C,0}$.

While a simplistic circuit representation of the FE-DE heterostructure enables us to effectively describe coercive voltage enhancement, the leakage in dielectric and ferroelectric thin films is complex and cannot be described by linear resistors. To this end, we use Ginestra, a defect-based modeling platform to simulate these heterostructures with intercalated metals to explore the influence of different material properties of the ferroelectric and dielectric layers [22].

2.3 | Design Space for Coercive Voltage Enhancement

Initially, TDL and GBL based FE-DE heterostructures are simulated to study the effect of the location of the dielectric on enhanced coercive voltages. The simulated P–V loops with 6.5/5(Al)/6.5 and 13/5(Al) reveal minimal difference further confirming that the location of the dielectric has little to no effect on the coercive voltage (Figure 5a).

Importantly, the increase in the coercive voltage window with increasing dielectric thickness as shown in Figure 5b, further confirms that reducing leakage results in increased coercive voltage. The linearity of this increase also substantiates that the mechanism is indeed resistive voltage division, Figure 5b.

Following this, we simulate the impact of the dielectric constant of the dielectric insert, demonstrating minimal impact at low dielectric constants (< 20). At high dielectric constants, the ferroelectric loop slants indicating that the capacitive component dominates the voltage division (Figure 5c).

In a dielectric layer thicker than 1.5–2 nm, the leakage mechanism is largely dominated by trap-assisted tunneling (TAT). We vary the trap density in the dielectric layer to understand the influence of increasing leakage in the dielectric layer (Figure 5d and Figure S5b). It is observed that the coercive voltage shrinks as the leakage increases, further affirming that controlling leakage in the dielectric layer is essential to engineering large coercive voltages in FE-DE heterostructures.

We simulate P–V characteristics using different dielectric materials: Al_2O_3, Si_3N_4, HfO_2, and SiO_2 (Figure 5e). The material properties are summarized in Figure S6. The ultrahigh coercive voltage achieved with the SiO_2 insert is attributed to the low electron affinity ($\chi_{SiO2} = 0.95$ eV). Figure S4f shows the increase in coercive voltage with decreasing electron affinity. Low electron affinities effectively translate to reduced leakage through the dielectric layers enabling large coercive voltages (Figure S5c). Similar trends are confirmed at different dielectric thicknesses, with insertion of SiO_2 resulting in the largest coercive voltage increases with increasing dielectric thicknesses (Figure 5f). It is worth noting that while the coercive voltage increases, the switching behavior between all the FE-DE heterostructures are similar.

Simulated P–V characteristics with varying coercive fields (E_C) and remanent polarizations (P_r) are shown in Figure S4g,h. The effective coercive voltage of the heterostructure shows minimal dependence on the remanent polarization while increasing the coercive field of the ferroelectric layer increases the effective coercive voltage of the FE-DE heterostructure.

Through this detailed exploration of the influence of the material properties of the dielectric and ferroelectric layers on the effective coercive voltage of the heterostructures, we establish that less leaky dielectrics promote enhanced coercive voltages. The leakage in a dielectric layer can be minimized either extrinsically, by reducing the defect density in the dielectric layer through optimized process design, or intrinsically, by choosing a large bandgap materials with low electron affinities. The strong dependence of coercive voltage enhancement on the material properties determining leakage over the capacitive component of the dielectric layer (like dielectric constant) affirms the leakage-governed nature of polarization switching in these heterostructures.

2.4 | Polarization Switching Dynamics

One of the key differences between a charge trapping mediated mechanism and leakage/resistive mechanism is their frequency response. For instance, the speed of trapping and detrapping mechanisms limit operating speed of ferroelectric field-effect transistors, while leakage driven mechanisms are not limited in speed. The polarization switching kinetics are measured through positive-up-negative down (PUND) measurements. The switching kinetics are modeled using a nucleation limited switching (NLS) model as described in Ref. [24].

Figure 6a shows the switching kinetics with a NLS fit for a standalone 19 nm-thick FE layer (top) and the 8.5/3(Al)/8.5 (bottom) heterostructure. The parameters extracted from the NLS fit are provided in Figure S9. The probability density functions of the switching times of grains at different fields, shown in Figure 6b, indicate that 8.5/3(Al)/8.5 heterostructure switches at comparable or faster times than a standalone ferroelectric of comparable

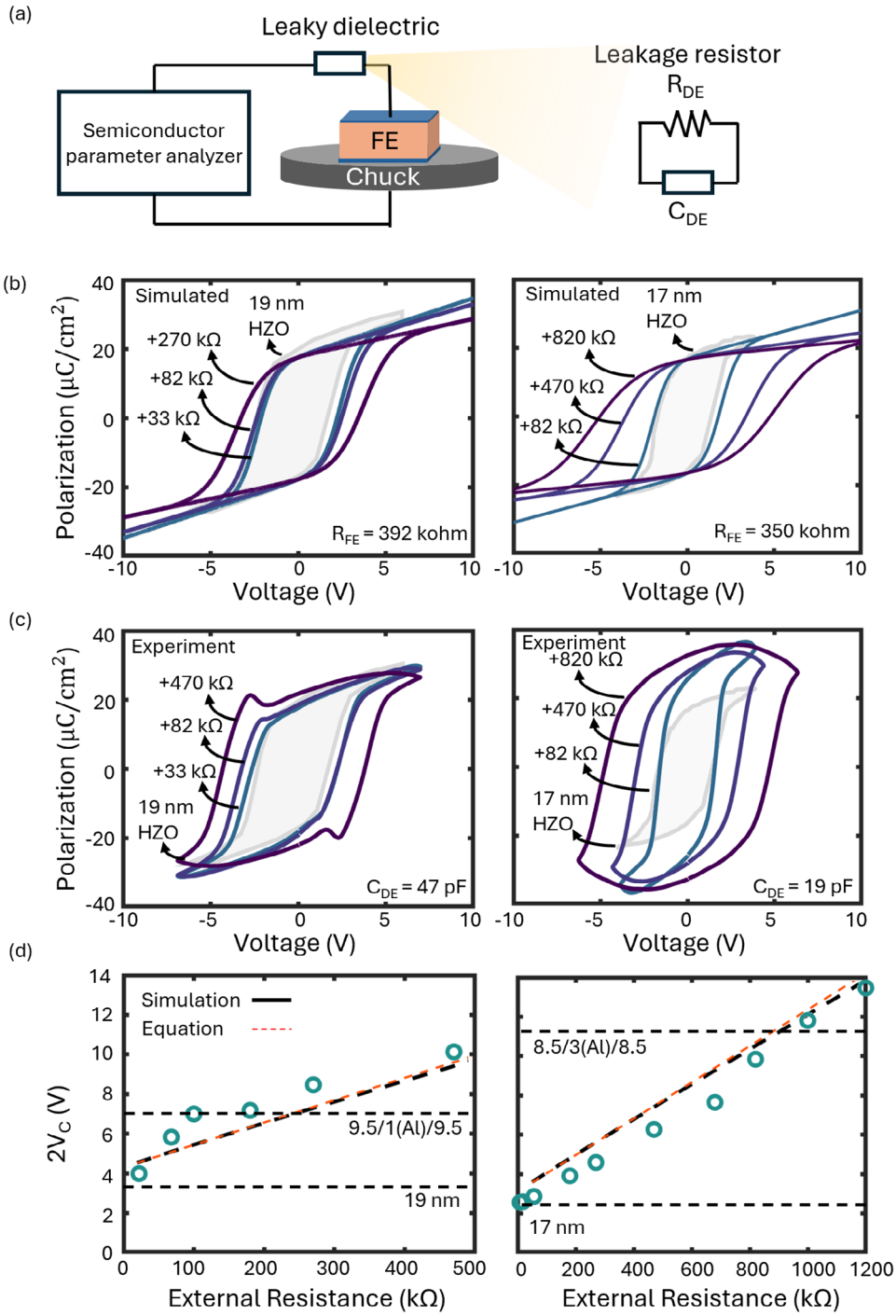

FIGURE 4 | To validate the model, we started with 17 and 19 nm reference capacitors and added a leaky dielectric externally. (a) The leaky dielectric was emulated using a ceramic capacitor with a resistor in parallel. The capacitor was chosen to match the 1 and 3 nm Al_2O_3 layers. The leaky resistor was changed to simulate the changing leakages in the dielectric layer. It was observed from (b) simulated and (c) experimentally measured P–V characteristics that the $2V_C$ increases as R_{DE} is increased. (d) A summary of the experimentally measured coercive voltage windows are shown along with the simulation results. The expression for the coercive voltage window is shown to be in good agreement with both the simulation and experimental results. The 19 nm HZO with 48 pF dielectric capacitor and 240 kΩ leakage resistor is shown to match the effective coercive voltage windows $2V_C$ of the GBL 19/1(Al) and TDL 9.5/1(Al)/9.5 gate stacks. Further, 17 nm HZO with a 19 pF dielectric capacitor and ~900 kΩ leakage resistor matches the effective coercive voltage window $2V_C$ of 8.5/3(Al)/8.5 heterostructure.

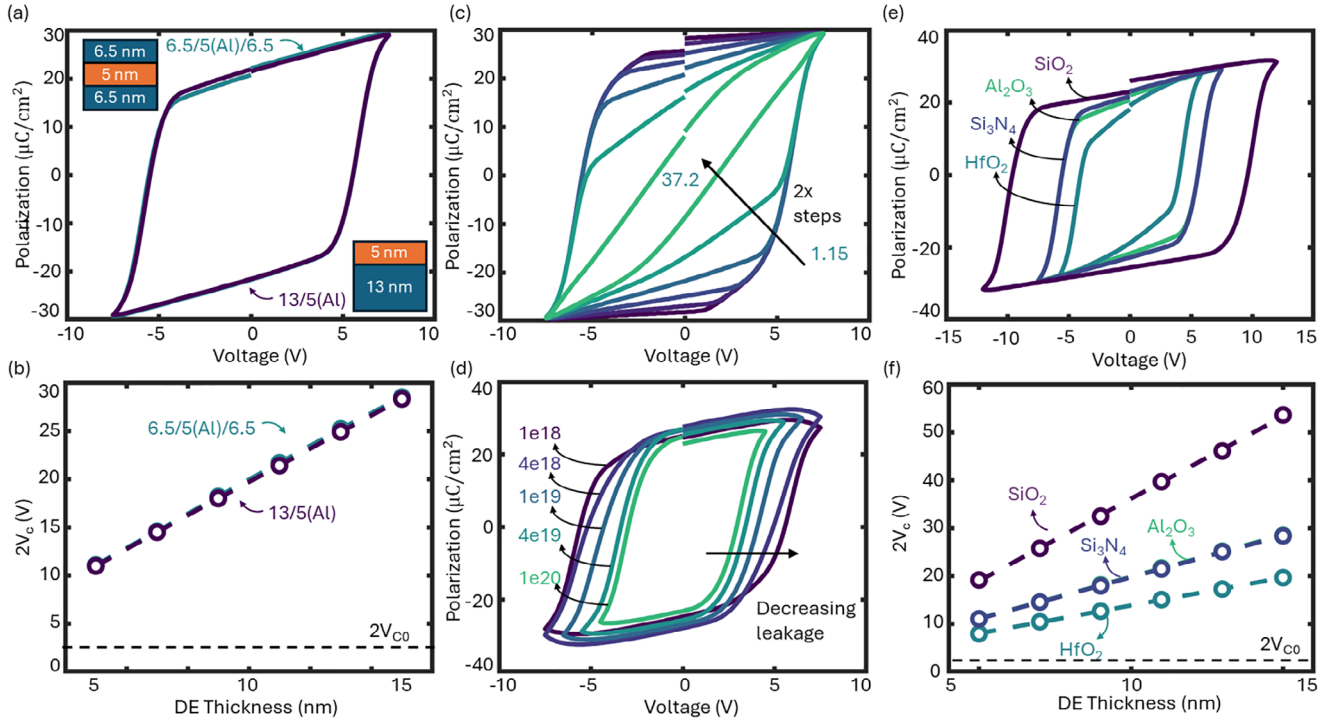

FIGURE 5 | Ginestra based simulations are used to simulated the influence of material level properties. (a) P–V characteristics of 6.5/5(Al)/6.5 and 13/5(Al) heterostructures exhibit similar enhanced coercive voltages and reveal that the location of the dielectric has minimal influence on the coercive voltage. (b) The coercive voltage window of the heterostructure increases linearly with dielectric thickness for both configurations. (c) Dielectric constant of the dielectric layer has minimal influence on the coercive voltage of the heterostructure for lower values. Values higher than 20 show slanting of the P–V characteristics. (d) Increasing trap density in the dielectric layer is shown to decrease the coercive voltage of the heterostructure, similar to that observed with decreasing the resistance of the dielectric layer. (e,f) Simulated P–V characteristics with different dielectric materials show that SiO_2 enables the largest coercive voltages due to its low electron affinity and large band gap.

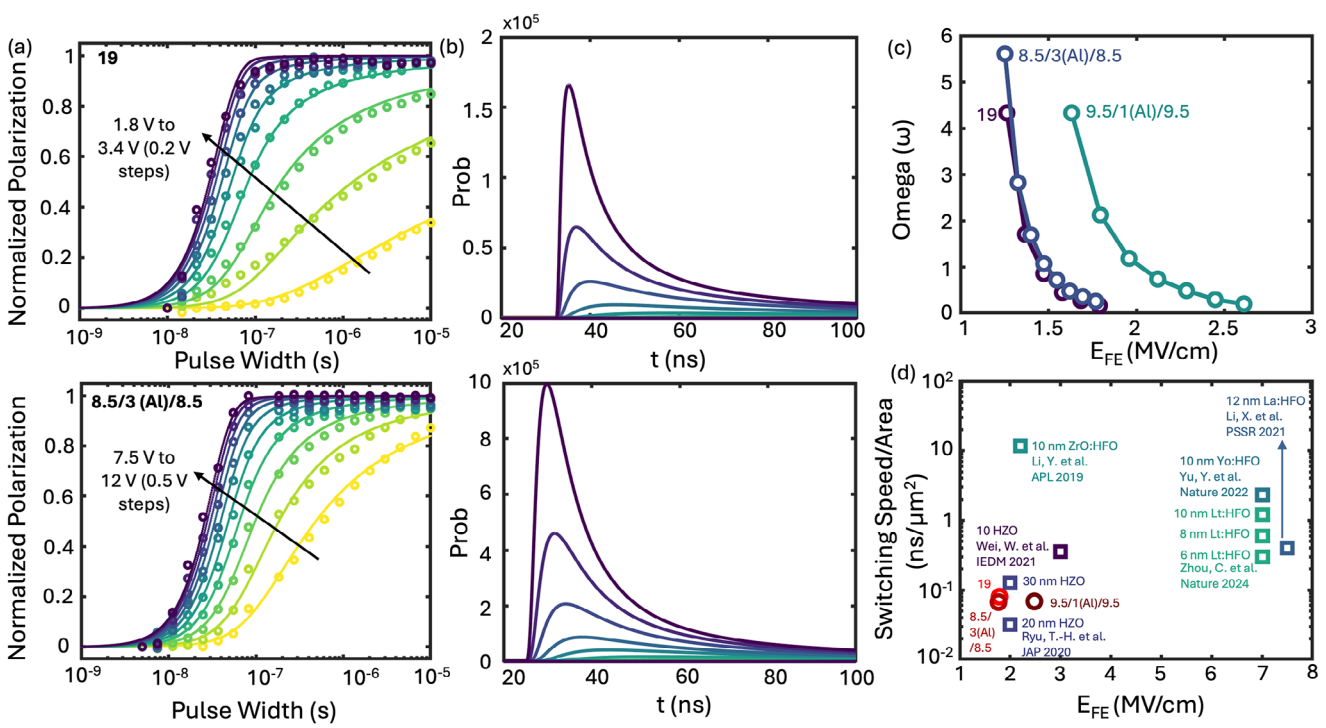

FIGURE 6 | (a) Polarization switching kinetics of the standalone ferroelectric (19) and FE-DE heterostructure (8.5/3(Al)/8.5) fitted with the NLS model. (b) Probability distribution of the switching times at different electric fields. (c) Full-width at half maximum of the P.D.F. for the standard FE and FE-DE heterostructures. (d) Area scaled switching times for different ferroelectrics and FE-DE heterostructures.

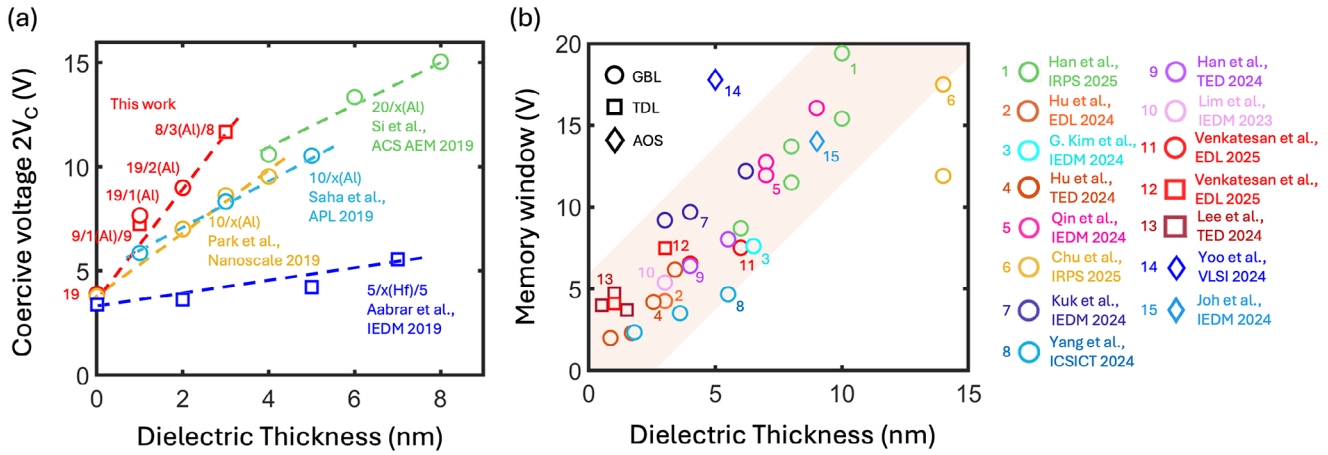

FIGURE 7 | The model is validated through a benchmark of the (a) $2V_C$ and (b) MW of engineered MIMs and FEFETs where increasing the dielectric thickness is shown to increase the $2V_C$[16–19] and MW [3–6, 8, 9, 31–39].

thickness (bottom vs. top). The full width at half maximum (ω) extracted from these distributions for different fields across the ferroelectric layer conveys a similar trend among standard FE capacitors and FE-DE heterostructures (Figure 6c). The field across the ferroelectric in FE-DE heterostructures is extracted based on the leaky FE-DE model presented in Figure 4d at R_{DE} calibrated to match the coercive voltage of the heterostructures.

The switching speed of FE capacitors along with the FE-DE heterostructures described above is shown in Figure 6d, confirming that these FE-DE heterostructures switch at speeds comparable to or better than the standard FE capacitors. This further affirms the leakage-governed nature of this coercive voltage enhancement.

2.5 | Universality of the Model

Figure 7a shows a benchmark of the coercive voltages from FE-DE heterostructures reported across the literature. The linear increase in coercive voltage with increasing dielectric thicknesses validates the universality of our model across FE-DE heterostructures with different process flows, material choices, and dielectric thicknesses.

Importantly, the discussions on coercive voltage enhancement in ferroelectric capacitors can be extended to the memory window of the engineered FEFETs with TDL and GBL gate stacks, as the enhancement has been shown to result from resistive voltage division rather than charge trapping. That said, it is worth noting that we assume the location of the dielectric to have minimal influence on the material properties of the heterostructures. For instance, we assume the top and bottom ferroelectrics in a TDL based heterostructure to crystallize, similar to a single thick ferroelectric layer of combined thickness in a GBL based heterostructure.

A benchmark of the memory window of FEFETs with FE-DE heterostructures in Figure 7b shows a trend of increasing MW with increasing dielectric thickness irrespective of the choice of materials or configuration of the device (TDL or GBL).

While this model provides an effective tool to investigate memory window enhancement, reliability concerns need to be addressed carefully. Polarization switching in hafnia-based ferroelectrics is intrinsically governed by a complex interplay of defects, domains, and microstructural heterogeneity, where oxygen vacancies, phase coexistence, and grain-scale disorder control nucleation-limited switching and broaden coercive field distributions, while defect-assisted transport and leakage directly couple to polarization switching dynamics in ferroelectric thin films [25–29]. Past studies, especially those pertaining to retention, have observed a large variation in the behavior of FEFETs with the location of dielectric inserts [10, 30]. Additionally, high-k dielectric inserts between ferroelectric and low-k materials have been shown to be effective in mitigating retention loss [31, 32]. These highlight the need for integrating the understanding about coercive voltage enhancement in FE-DE heterostructures with the complex trap dynamics of FEFETs.

Apart from providing a platform for engineering FE-DE heterostructures for enhanced MW for FE-NAND applications, we address a key scientific question about the behavior of fluorite-structure based FE-DE heterostructures in general, explaining the increased coercive voltages in these devices, contrary to perovskite based FE-DE heterostructures. That said, in this work, we model the ferroelectric–dielectric interface as an equipotential surface and the model explains the observed coercive voltage enhancement across a wide range of experiments. However, the fundamental understanding about the FE-DE interface is yet to be explored.

3 | Conclusion

In conclusion, we identify resistive voltage division between ferroelectric and dielectric layers as the origin of coercive voltage enhancement in hafnia-based ferroelectric–dielectric heterostructures, resolving a long-standing mechanistic debate. A simple circuit model of leaky capacitors in series reproduces experimental P–V characteristics and yields an analytical expression directly linking effective coercive voltage to the leakage resistances of the constituent layers. External leaky dielectric

experiments and defect-based Ginestra simulations confirm that suppressing dielectric leakage leads to predictable and scalable increases in coercive voltage, independent of dielectric placement within the stack.

Importantly, nucleation-limited switching analysis demonstrates that the fundamental switching kinetics remain unaltered, confirming that the enhancement is due to leakage-governed voltage division rather than trap-assisted mechanisms. These findings establish a predictive design framework in which dielectric bandgap, electron affinity, and defect density emerge as key control parameters for coercive voltage engineering.

Beyond immediate applications in multi-level ferroelectric NAND (TLC/QLC), this framework reconciles the contrasting behaviors of fluorite- and perovskite-based heterostructures and highlights how simple electrical models can capture complex ferroelectric–dielectric heterostructures. By bridging detailed materials physics with a universal circuit-based description, this work provides both a fundamental understanding of ferroelectric–dielectric heterostructures and practical design principles for next-generation ferroelectric devices.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.

Supporting File: aelm70292-sup-0001-SuppMat.pdf.