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ALD-Derived WO_{3-x} Leads to Nearly Wake-Up-Free Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ at Elevated Temperatures

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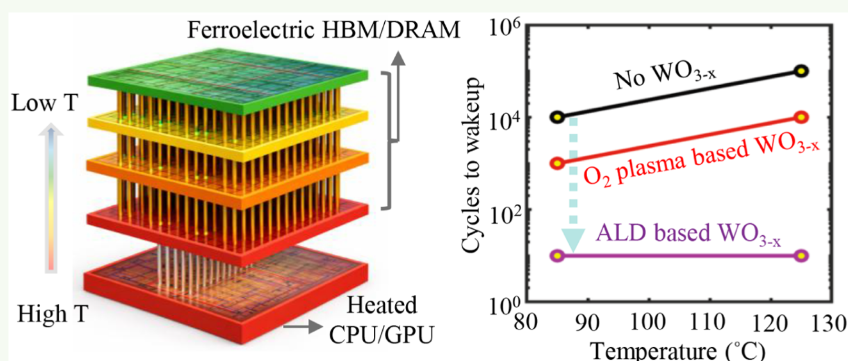

ABSTRACT: Breaking the memory wall in advanced computing architectures will require complex 3D integration of emerging memory materials such as ferroelectrics—either within the back-end-of-line (BEOL) of CMOS front-end processes or through advanced 3D packaging technologies. Achieving this integration demands that memory materials exhibit high thermal resilience, with the capability to operate reliably at elevated temperatures, such as 125°C, due to the substantial heat generated by front-end transistors. However, silicon-compatible HfO_2-based ferroelectrics tend to exhibit antiferroelectric-like behavior in this temperature range, accompanied by a more pronounced wake-up effect, posing significant challenges to their thermal reliability. Here, we report that by introducing a thin tungsten oxide (WO_{3-x}) layer—known as an oxygen reservoir—and carefully tuning its oxygen content, ultrathin $Hf_{0.5}Zr_{0.5}O_2$ (5 nm) films can be made robust against the ferroelectric-to-antiferroelectric transition at elevated temperatures. This approach not only minimizes polarization loss in the pristine state but also effectively suppresses the wake-up effect, reducing the required wake-up cycles from 10^5 to only 10 at 125°C, a qualifying temperature for back-end memory integrated with front-end logic, as defined by the JEDEC standard. First-principles density functional theory (DFT) calculations reveal that WO_3 enhances the stability of the ferroelectric orthorhombic phase (o-phase) at elevated temperatures by increasing the tetragonal-to-orthorhombic phase energy gap and promoting favorable phonon mode evolution, thereby supporting o-phase formation under both thermodynamic and kinetic constraints.

KEYWORDS: *ferroelectric memory, HfO_2-based ferroelectrics, oxygen reservoir layer, ALD deposited WO_{3-x}, high-temperature operation, nearly wake-up-free, memory-on-logic, 3D integration*

INTRODUCTION

AI is fueling advances across domains such as high-performance computing, cloud infrastructure, mobile platforms, autonomous vehicles, and augmented reality, yet the massive data sets and complex models driving these applications are turning training and inference into critical memory and reliability challenges. Ferroelectric memory technologies, such as ferroelectric NAND (FE-NAND), ferroelectric random access memory (Fe-RAM), and ferroelectric field-effect transistors (FeFETs), have become leading contenders for nonvolatile memory solutions across various segments of the memory hierarchy.[1−3] Recently, significant advancements in ferroelectric memories have been achieved, including the demonstration of a high-capacity dual-layer FE 1T-1C memory chip with a 32 Gb capacity and DRAM-comparable performance, as well as emerging three-dimensional integration of ferroelectric devices, exemplified by vertically stacked multilayer ferroelectric architectures for high-density

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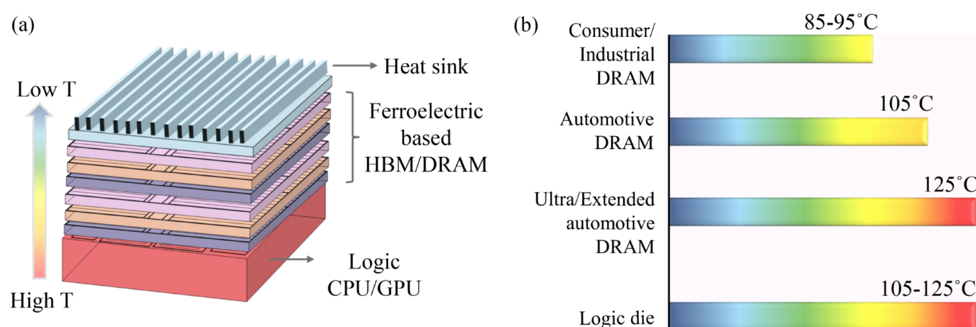
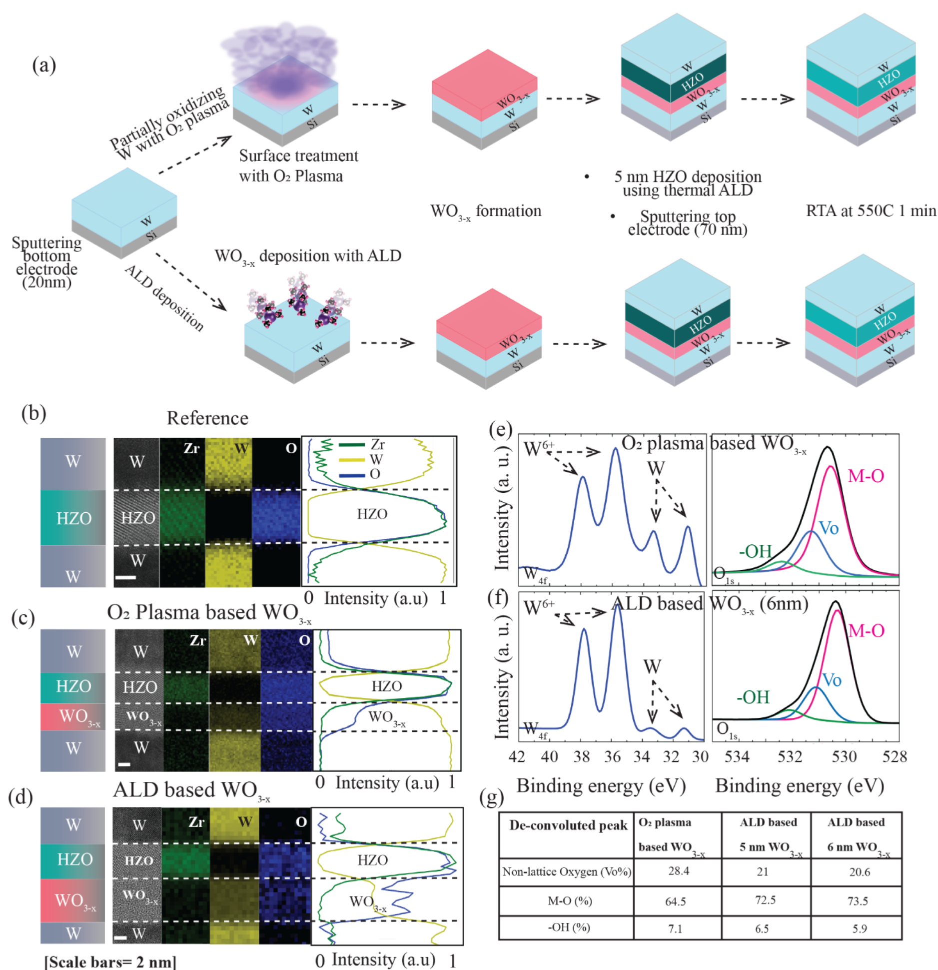


Figure 1. Importance of high-temperature performance enhancement of ferroelectric memories. (a) Schematic of 3D integration of memory on a logic architecture. Memories away from the heat sink get heated due to the heated logic die. (b) Operating temperatures of Micron DRAMs based on different applications.



De-convoluted peak	O₂ plasma based WO_{3-x}	ALD based 5 nm WO_{3-x}	ALD based 6 nm WO_{3-x}
Non-lattice Oxygen (Vo%)	28.4	21	20.6
M-O (%)	64.5	72.5	73.5
-OH (%)	7.1	6.5	5.9

Figure 2. Device structures and material characterization of ferroelectric capacitors. (a) Fabrication process of O_2 plasma- and ALD-based WO_{3-x} devices. (b−d) Cross-sectional STEM images of (b) reference and (c) O_2 plasma- and (d) ALD-based 6 nm WO_{3-x} devices along with their EDS characterization. Material-count map coming from Zr (green), W (yellow), and O (blue) and the corresponding line scans for (b) reference, (c) O_2 plasma, and (d) ALD devices. The line scans on the right of each material count map further confirm the layers and their interfaces. XPS spectra obtained from W 4f and O 1s orbitals of WO_{3-x} from (e) O_2 plasma- and (f) ALD-based 6 nm WO_{3-x} samples. (e,f) Magenta, blue, and green curves in the O 1s plot are the deconvoluted peaks corresponding to M−O, nonlattice oxygen (V_o), and −OH, respectively. (g) Table showing the percentage obtained from the deconvoluted peaks of the O 1s scan of different samples.

integration.[4,5] Despite advantages such as nonvolatility and high charge density, ferroelectric materials require a deeper understanding to ensure reliable operation, particularly under elevated temperatures.[6]

As the semiconductor industry advances toward 3D-IC integration, the intermediate step of memory-on-logic has demonstrated benefits comparable to those of a full technology node improvement. This memory-on-logic configuration shortens the communication distance between logic and memory, delivering up to 22% higher performance and 36% lower power consumption.[7] However, thermal management poses a critical challenge. With an increasing number of stacked dies, tiers

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located farther from the heat sink and closer to heat-generating logic layers experience substantial thermal buildup due to thermal resistance and crosstalk[8] (Figure 1a). Since logic dies are generally capable to operate at 105−125°C,[9] memories must also be qualified to operate reliably at 125°C according to the JEDEC JESD22-A108 standard for 3D-IC qualification. Figure 1b summarizes the maximum operating temperature specifications of Micron DRAMs across different application scenarios.[10] These specifications highlight the need for robust high-temperature performance, which is essential for enabling reliable integration of ferroelectric memories into emerging heterogeneous and monolithic 3D (H3D and M3D) systems and memory-on-logic architectures. Unfortunately, HfO_2-based ferroelectrics, which form the foundation of many next-generation memory devices, remain highly vulnerable to degradation at elevated temperatures. It is well-established that increasing temperature induces an orthorhombic-to-tetragonal phase transition in ferroelectric materials, leading to pinching of the polarization loops and a gradual decrease in remnant polarization.[11−17] Consequently, ferroelectricity can be lost under thermal stress, severely limiting device reliability.[16,18−20] Although there have been lots of studies done on improving wakeup behavior and orthorhombic phase enhancement at room temperature using strategies like different atomic layer deposition (ALD) techniques,[21] electrode engineering,[22−25] controlling oxygen flow during deposition,[26] high-temperature cycling,[27] and interface engineering,[28−30] systematic efforts to improve wakeup effect and pristine state polarization at elevated temperatures remain scarce in the literature.[31]

Among various strategies to enhance ferroelectric device performance, interface engineering has shown particular promise. Several interfacial layers have been explored to improve endurance, leakage, and polarization characteristics. For example, NbO_2 and TiO_2 have been used for endurance enhancement,[32−34] Pt has been employed to reduce leakage and wake-up effects,[26] and TiON and WN_x have been investigated for boosting polarization.[29,35,36] More recently, WS_2 has demonstrated improvements in both polarization and endurance.[37] In particular, WO_x has gained attention as an effective oxygen reservoir for improving different properties of ferroelectric capacitors at room temperature.[21,28,38−45] However, its potential for enhancing ferroelectric performance at elevated temperatures remains largely unexplored.[46−48]

In this study, we demonstrate that incorporating WO_{3-x} as an interfacial oxygen reservoir layer significantly enhances the high-temperature performance of $Hf_{0.5}Zr_{0.5}O$ (HZO)-based capacitors. WO_{3-x} is introduced at the interface between the bottom electrode and the HZO film, either by oxidizing the electrode via the O_2 plasma treatment or through atomic layer deposition (ALD). This interface engineering approach increases the ability to retain the orthorhombic phase in HZO, suppressing the emergence of antiferroelectric behavior in pristine devices under thermal stress. As a result, the number of bipolar cycles required to achieve wake-up is significantly reduced in WO_{3-x}-incorporated devices. First-principles density functional theory (DFT) calculations indicate that the presence of WO_3 stabilizes the ferroelectric o-phase at elevated temperatures through a combination of effects: an increased tetragonal−orthorhombic phase energy gap in the Helmholtz free energy landscape and enhanced X_2' phonon mode coupling. These effects arise from the lower entropy and lattice anisotropy induced by WO_3, which together favor the orthorhombic $Pca2_1$ phase formation under both thermodynamic and kinetic considerations. This stabilization of ferroelectric behavior under thermal stress enhances the temperature resilience of the device. Our results provide a promising pathway for achieving thermally robust ferroelectric memories, such as Fe-RAMs and Fe-FETs, enabling their deployment in emerging 3D memory-on-logic architectures where elevated temperatures present a significant reliability challenge.

RESULTS AND DISCUSSION

Experiment

Figure 2a illustrates the fabrication process flow of ferroelectric capacitors incorporating WO_{3-x} as an oxygen reservoir layer introduced via two distinct methods. In the first approach, partial oxidation of the sputtered W bottom electrode on Si was carried out using an O_2 plasma treatment within the atomic layer deposition (ALD) chamber, resulting in the formation of an approximately 4 nm thick WO_{3-x} layer at the W surface. In the second approach, a plasma-enhanced ALD (PE-ALD) technique was employed to directly deposit 5 and 6 nm thick WO_{3-x} layers on the W electrode. For the reference device, the HZO layer was deposited directly on the bottom W electrode without any intermediate WO_{3-x} layer. Further details of the fabrication procedure are described in the Methods section.

Scanning transmission electron microscopy (STEM) images of the cross-section of the fabricated devices are presented in the leftmost panel of Figure 2b−d, corresponding to the reference and O_2 plasma- and ALD-based WO_{3-x} device structures, respectively. To verify the formation of WO_{3-x} at the bottom interface in both the O_2 plasma- and ALD-based devices, energy-dispersive X-ray spectroscopy (EDS) was carried out. Elemental mapping confirmed the presence of distinct W and O signals at the interface in these devices, validating the successful formation of a WO_{3-x} layer. In contrast, the reference device exhibited no such signals, indicating the absence of an interfacial WO_{3-x} layer.

To assess the stoichiometry of WO_{3-x} films synthesized via an O_2 plasma treatment and atomic layer deposition (ALD), X-ray photoelectron spectroscopy (XPS) analysis was conducted, as shown in Figure 2e and f. The W 4f spectra from both samples exhibit prominent W^{6+} peaks, confirming the successful formation of WO_{3-x}. The O 1s spectra were deconvoluted to quantify the contributions from lattice and nonlattice oxygen species, with the extracted component ratios summarized in Figure 2g. Notably, the O_2 plasma-based WO_{3-x} film shows a significant contribution from nonlattice oxygen, corresponding to an oxygen vacancy (V_o) concentration of approximately 28.4%. In contrast, the ALD-deposited WO_{3-x} films with 5 and 6 nm thicknesses exhibit a comparatively lower V_o concentration of 21%. The full XPS spectrum for 5 nm ALD-grown WO_{3-x} is provided in Figure S1. These results indicate that while both methods yield substoichiometric WO_{3-x}, the plasma process of the O_2 introduces a higher density of oxygen vacancies. Furthermore, these findings underscore that the deposition technique, rather than film thickness, plays a critical role in governing WO_{3-x} stoichiometry, which in turn significantly impacts the electrical behavior of the devices, as elaborated in Figure 3.

Figure 3 presents the polarization−voltage ($P-V$) characteristics of all fabricated devices, along with the extracted coercive voltage and remnant polarization values from $P-V$ and positive-up negative-down (PUND) measurements, respectively. To decouple ferroelectric switching from leakage effects, PUND

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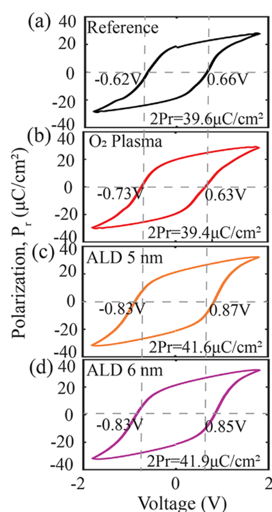

Figure 3. Electrical characterization at room temperature. $P-V$ loops after 10^5 cycles from (a) reference and (b) O_2 plasma- and ALD-based (c) 5 nm and (d) 6 nm WO_{3-x} devices. $2P_r$ values are extracted from PUND measurement.

measurements were performed. All devices demonstrated comparable remnant polarization ($2P_r$), confirming that the incorporation of WO_{3-x} does not compromise the ferroelectric polarization. Additionally, WO_{3-x} plays a beneficial role in enhancing device endurance, both at room and at higher temperatures, as shown in Figure S2 and supported by previous studies.[39,41] A detailed analysis of temperature-dependent endurance improvements due to WO_{3-x} incorporation can be found in earlier work.[46] Moreover, the inclusion of WO_{3-x} does not adversely affect the imprint and retention behavior, as illustrated in Figures S3 and S4.

The coercive voltage of the O_2 plasma-based device closely matches that of the reference device, whereas the ALD-deposited WO_{3-x} devices exhibit a higher coercive voltage (Figure 3). This behavior indicates that the ALD-deposited WO_{3-x} is less conductive compared to the plasma-based counterpart, thereby dropping more voltage across the WO_{3-x} layer and requiring a higher switching voltage for the overlying HZO layer. This increase in the coercive voltage is consistent with the comparatively lower conductivity measured in these devices (Figure S5), and the lower oxygen vacancy (V_o) concentration observed in the ALD samples from the XPS analysis in Figure 2e−g. Given that oxygen vacancies significantly affect the electrical conductivity of WO_3 films,[45,49]

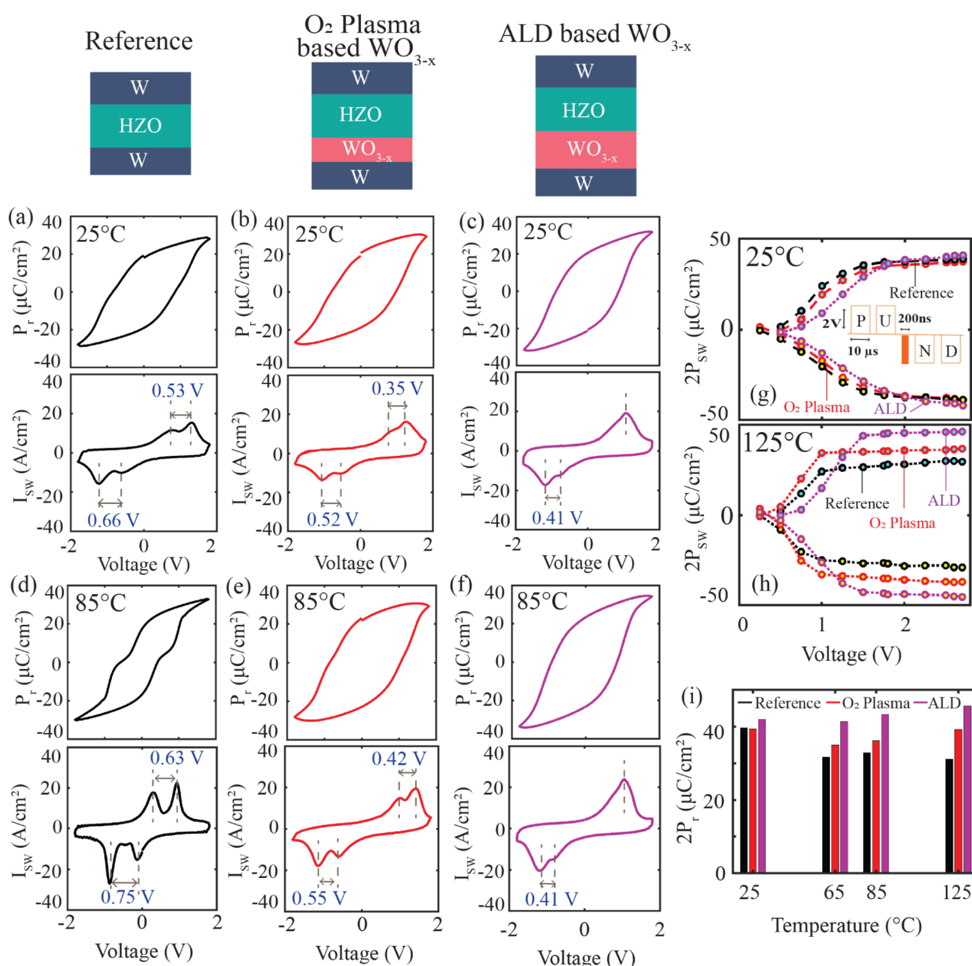

Figure 4. Temperature-dependent polarization and switching current characteristics at the pristine state. $P-V$ and $I_{SW}-V$ characteristics at (a−c) 25 and (d−f) 85°C from (a,d) reference and (b,e) O_2 plasma- and (c,f) ALD-based WO_{3-x} devices, respectively. (g,h) Polarization switched with 200 ns pulses at different voltages measured at 25 and 125°C, respectively, on pristine devices. (i) $2P_r$ obtained from PUND measurement with 2 V/10 μs square pulses at different temperatures in the pristine state.

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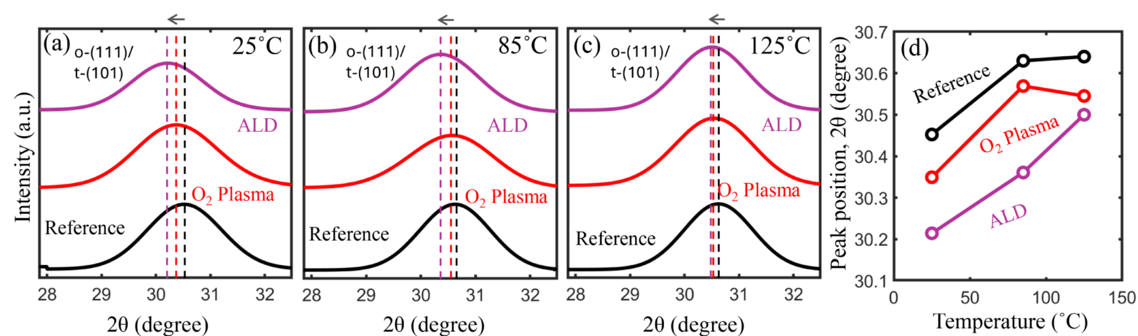

Figure 5. Grazing incident X-ray diffraction (GI-XRD) from the HZO film of reference and O_2 plasma- and ALD-based 6 nm WO_{3-x} samples at (a) 25, (b) 85, and (c) 125°C. (d) Dominant peak (o-111/t-101) position of all the samples at different temperatures obtained from (a)−(c).

Figure 6. Temperature and cycling-dependent $P-V$ and $I_{SW}-V$ characteristics. $I_{SW}-V$ characteristics at (a,c,e) 85 and (b,d,f) 125°C from pristine to 10^5 cycles for (a,b) the reference, (c,d) the O_2 plasma-based WO_{3-x}, and (e,f) the ALD-based WO_{3-x} devices. Green asterisks denote the number of cycles required to remove the antiferroelectric-like double peak behavior. $P-V$ loops from pristine to 10^5 cycles at (g,i,k) 85 and (h,j,l) 125°C of (g,h) reference, (i,j) O_2 plasma-based WO_{3-x}, and (k,l) ALD-based WO_{3-x} devices.

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Table 1. Comparison of Ferroelectric Properties at High Temperature (HT) with Prior Works

	[29]	[16]	[17]	[25]	[45]	This work
Film thickness (nm)	10	10	7	3	12	**5**
Write voltage (V)	3.5	2.2	2.1	1	3	**1.8**
Electric field (MV/cm)	3.5	2.2	3	3.3	2.5	**3.6**
Pristine $2P_r$ ($\mu C/cm^2$)	26	15.1	16	5	32.94	**41.94**
Pristine $2P_r$ at HT ($\mu C/cm^2$)	–	7 (120°C)	13.56 (125°C)	11.81 (85°C)	24.95 (100°C)	**45.57 (125°C)**
Cycles to wakeup at HT	10^3 (100°C)	10^6 (100°C)	10^4 (100°C)	10^3 (85°C)	10^6 (100°C)	**10 (125°C)**

the reduced V_o content in ALD-deposited layers leads to decreased conductivity.

The polarization−voltage (P−V) and switching current−voltage (I_{SW}−V) characteristics of all three devices in their pristine states were measured across a wide range of temperatures, as shown in Figure 4. At room temperature, both the reference and the O_2 plasma-based WO_{3-x} devices exhibit similar P−V and I_{SW}−V responses, while the ALD-deposited WO_{3-x} device shows marginally enhanced ferroelectric behavior (Figure 4a−c). Upon increasing the temperature to 85°C, the reference device that lacks any WO_{3-x} interfacial layer exhibits a pronounced antiferroelectric-like response, evidenced by a well-defined double-peak structure in the I_{SW}−V curve (Figure 4d), indicating that the transition away from the orthorhombic ferroelectric phase initiates well before the targeted operating temperature (125°C) is reached.

In contrast, the O_2 plasma-based device demonstrates improved thermal stability of ferroelectricity, evidenced by reduced separation of switching current peaks compared to the reference device at 85°C (Figure 4e). A smaller separation between same-direction switching peaks indicates reduced antiferroelectric-like behavior.[50] Further enhancement in thermal robustness is observed for devices with ALD-based WO_{3-x} for the 6 nm layer (Figure 4f) and similarly for the 5 nm variant (Figure S6). These devices show a minor residual switching peak on the negative voltage side across all temperatures, suggesting that the WO_{3-x} incorporation effectively suppresses or delays the onset of the antiferroelectric phase transition.

This trend is validated by PUND measurements performed under varying temperature conditions in pristine states. Using 200 ns square pulses of varying amplitudes, the switched polarization ($2P_{SW}$) was extracted. At room temperature, all devices exhibit comparable saturated polarization values under pristine conditions (Figure 4g). However, at 125°C, the reference device shows a significant drop in polarization relative to that of the WO_{3-x}-containing devices (Figure 4h), indicating temperature-induced degradation of ferroelectricity in the absence of WO_{3-x}. This observation is further reinforced by long-pulse (10 μs/2 V) PUND measurements across a wide temperature range on pristine devices, where the extracted $2P_r$ values confirm that ferroelectric properties deteriorate significantly in the reference device, while devices with WO_{3-x} maintain polarization more effectively (Figure 4i). These results highlight the crucial role of WO_{3-x} in stabilizing the ferroelectric orthorhombic phase at elevated temperatures in the pristine state, thereby preserving ferroelectric properties and suppressing unwanted phase transitions.

To confirm the stabilization of the ferroelectric o-phase with the incorporation of WO_{3-x} at elevated temperatures, grazing incidence X-ray diffraction (GI-XRD) measurements of the HZO layer in reference and O_2 plasma- and ALD-based WO_{3-x} samples were performed at 25, 85, and 125°C. As shown in Figure 5a, the major o-(111)/t-(101) diffraction peak through Gaussian fitting from the samples having WO_{3-x} is shifted toward lower angles compared to the reference device, indicating a greater orthorhombic phase fraction. This observation aligns with the known peak positions of the o-(111) and t-(101) phases in HZO, located at approximately 30.4° and 30.8°, respectively. At 85°C, the peak separation between these samples decreases; however, the samples having WO_{3-x} still exhibit a discernible shift toward the orthorhombic phase, suggesting that a greater proportion of the orthorhombic phase is retained relative to the reference sample (Figure 5b). This behavior persists at 125°C, as shown in Figure 5c. The phase fractions of the o- and t-phases, extracted from the deconvolution of the o-(111)/t-(101) peaks measured at 125°C, are shown in Figure S7. The evolution of the peak positions with temperature for all of the samples is summarized in Figure 5d.

These results clearly demonstrate that the incorporation of WO_{3-x} helps maintain a higher orthorhombic phase fraction in HZO across a wide temperature range. And one of the reasons for this could be better lattice matching between orthorhombic $Pca2_1$ HZO and monoclinic WO_3 compared to that with W (Table S1). The monoclinic phase of WO_3 is chosen for comparison, as this phase is confirmed by STEM imaging of the O_2 plasma device (Figure S8). Additionally, the optimized V_o concentration in ALD-deposited WO_{3-x} is likely to promote enhanced o-phase stability in HZO compared to O_2 plasma-based WO_{3-x}, as prior studies have shown that stabilization of the o- phase in HZO is maximized within an optimal vacancy window in WO_{3-x}, whereas both excessively vacancy-rich and near-stoichiometric (vacancy-poor) conditions lead to reduced o-phase content.[45,51] The enhanced ferroelectric o-phase stability plays a critical role in suppressing the transition to antiferroelectric-like behavior at elevated temperatures, thereby contributing to improved ferroelectric performance.

The influence of electrical cycling on the switching behavior, with and without the presence of a WO_{3-x} interfacial layer at elevated temperatures, is studied in Figure 6. For the reference device, which lacks WO_{3-x}, a significant number of 10^4 cycles at 85°C and 10^5 cycles at 125°C are required to suppress the characteristic double peaks in the I_{SW} response and achieve clean ferroelectric switching (Figure 6a,b). In contrast, the O_2 plasma-based WO_{3-x} device exhibits stable ferroelectric switching behavior earlier than the reference, showing a single peak in the I_{SW} profile after just 10^3 and 10^4 cycles at 85 and 125°C, respectively (Figure 6c,d).

Remarkably, for the ALD-based 6 nm WO_{3-x} device, as few as 10 cycles are sufficient for the transition to pure ferroelectric switching at both 85 and 125°C (Figure 6e,f). This phenomenon is true for the ALD-based 5 nm WO_{3-x} device as well (Figure S9). The substantial reduction in wake-up cycles observed in the ALD-based WO_{3-x} compared to those in the O_2 plasma-based WO_{3-x} devices is consistent with the inherently

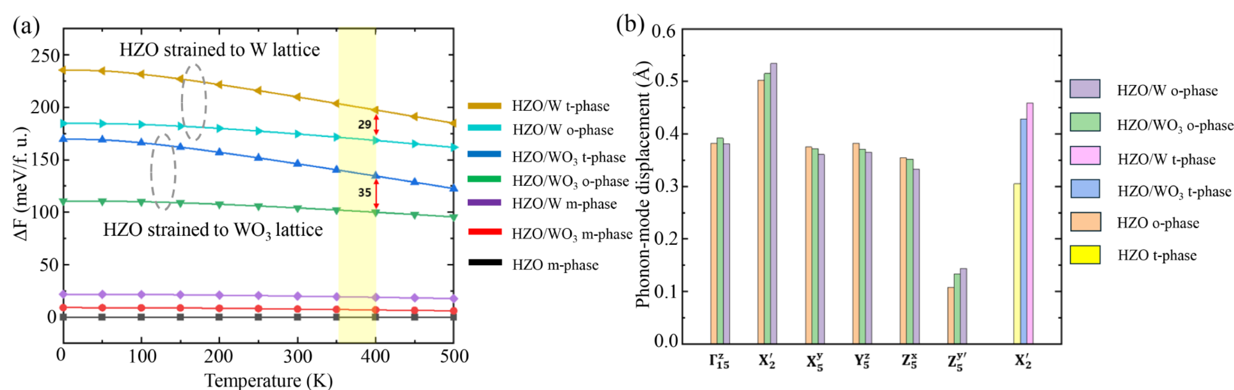

Figure 7. Density functional theory (DFT) analysis. (a) Helmholtz free energy difference (ΔF) for the 5 nm HZO film, relative to the m-phase. The yellow region and red arrow indicate the high-temperature operating range and free energy difference between t- and o-phases under W- and WO_3-induced strain. (b) Phonon mode analysis under tensile strain induced by W and WO_3, where the enhancement of the soft X_2' mode in the t-phase induces the phase transition to the o-phase.

gentler nature of the ALD process, which proceeds through self-limiting surface reactions and minimizes plasma-induced surface and interfacial defect generation. Collectively, these results underscore the critical role of the WO_{3-x} interfacial layer in enhancing the thermal and electrical stabilities of the ferroelectric phase. The corresponding $P-V$ loops at 85 and 125°C after different cycling stages are shown in Figure 6(g–l) for the reference, O_2 plasma and 6 nm ALD WO_{3-x} devices, and in Figure S10 for the 5 nm ALD WO_{3-x} device, further corroborating these trends. It is worth noting that once pure ferroelectric switching is achieved in the ALD-based WO_{3-x} devices at high temperatures after 10 bipolar cycles, it remains well preserved upon cooling to room temperature (Figure S11). Table 1 presents a benchmark of the 6 nm ALD WO_{3-x} device against prior studies of high-temperature ferroelectric capacitor behavior. The results indicate that the ALD WO_{3-x} device achieves superior pristine polarization and undergoes significantly fewer wake-up cycles during an elevated-temperature operation compared with recent reports. The $2P_r$ values of this work are obtained from the PUND measurement of Figure 4i.

The leakage current density and trap generation rate during electrical cycling of all devices at different temperatures are presented in Figure S12. Although all the devices including the reference device show a similar trap generation rate at room temperature, WO_{3-x} containing devices show a significantly lower trap generation rate during electrical cycling at elevated temperatures, irrespective of the WO_{3-x} deposition method (Figure S12(d–f)). This reduced trap generation is attributed to the oxygen-reservoir function of the WO_{3-x} layer, which contributes to the improved endurance (as shown in Figure S2) observed in these devices.[47]

Density Functional Theory (DFT)

To investigate the origin of the stabilization of ferroelectric properties at elevated temperatures in the presence of WO_{3-x}, density functional theory (DFT) calculations were performed to compare the stability of the orthorhombic $Pca2_1$ phase in HZO when deposited on W and WO_3. In this analysis, the atomic structure of bulk HZO was strained to match the lattice parameters of W and WO_3, as illustrated in Table S1. Although the tungsten oxide layer in the fabricated ferroelectric capacitors is substoichiometric, the HZO lattice is strained to the WO_3 lattice for the calculation, as the dominant feature in the W 4f XPS spectra corresponds to the W^{6+} oxidation state. Furthermore, WO_{3-x} containing oxygen vacancies does not exhibit a single well-defined periodic lattice constant due to the configurational disorder introduced by these vacancies. To account for oxygen deficiency, lattice mismatch calculations were carried out using a WO_3 supercell containing a single oxygen vacancy, as summarized in Table S1. The mismatch values indicate that oxygen vacancies can tune the cell-averaged mismatch while primarily introducing local strain inhomogeneity.[52] However, the key thermodynamic and kinetic trends discussed herein remain qualitatively unchanged.

Figure 7a presents the Helmholtz free energy of HZO in the monoclinic (m-), tetragonal (t-), and o- phases, each strained to match the lattice parameters of W and WO_3, respectively. The yellow-shaded region indicates the high operating temperature range of interest (65–125°C). Within this range, the energy difference between the t- and o-phases of HZO strained to the WO_3 lattice increases by approximately 20% compared to that strained to the W lattice, thereby favoring formation of the o-phase in the WO_3 case. This behavior arises because W, having a cubic structure, induces a more cubic-like configuration in HZO, resulting in a higher entropy relative to the WO_3 lattice (as reflected by the slope of the Helmholtz free energy curve). Consequently, the energy gap between the t- and o-phases is larger for WO_3 at elevated temperatures. While W exhibits a greater lattice mismatch and thus higher surface energy than WO_3, the increase in surface energies for both the o- and t-phases is comparable, yielding only a minor overall effect on the Helmholtz free energy.

Although the m-phase remains the thermodynamically most stable state even at a film thickness of 5 nm (i.e., exhibiting the lowest Helmholtz free energy), the kinetic barrier for the t → o phase transition is substantially lower than that for the t → m transition. Consequently, under kinetic constraints, the system preferentially transforms into the o-phase rather than the m-phase,[53] in agreement with the calculations presented in Table S2. During cooling, the high-energy barrier similarly suppresses the formation of the m-phase, leading to the preferential development of the o-phase, which possesses a Helmholtz free energy lower than that of the t-phase. This trend is further supported by Figure 7a, where the o-phase remains more stable than the t-phase even at elevated operating temperatures, making it the energetically favorable configuration.

As shown in Figure 7b, the t-phase of HZO exhibits only the X_2' oxygen phonon mode, which drives the cubic-to-tetragonal phase transition. When strain is applied to match the lattice

constant of WO_3, corresponding to an approximately 1.7% increase in the lattice constant along the x-direction relative to the pristine structure, the X_2' phonon mode in the t-phase is enhanced. This enhancement brings its value closer to that of the o-phase, indicating that the t → o phase transition becomes more accessible. Under the W lattice, the larger lattice mismatch produces a greater amplitude of the X_2' mode compared to the WO_3 case, leading, as shown in Table S2, to a lower t → o transition energy barrier. Overall, while the larger strain induced by W reduces the transition barrier relative to WO_3, the o-phase in the WO_3 case remains thermodynamically more stable than the t-phase due to the combined effects of surface energy at the 5 nm thick HZO and the large entropy associated with the larger in-plane lattice matched to the W cubic structure under nonequibiaxial strain (as described in Figure S13). These results are consistent with previous phase stabilization studies for the ZrO_2−WO_3 interface.[42]

The polarization switching barrier of HZO strained to the W and WO_3 lattices was further calculated and found to be lower in the WO_3-strained case (Figure S14). This difference arises because in the switching pathway the transition state corresponds to the t-phase, which exhibits a longer lattice constant along the x-direction than along the y-direction. For W, the structure is more cubic-like, with nearly identical lattice constants in both directions, leading to a higher switching barrier. In contrast, the anisotropy in the WO_3-strained lattice reduces the barrier height. This energy barrier difference contributes to improved overall switching kinetics in devices incorporating WO_3 or WO_{3-x} as the interfacial layer.

CONCLUSION

In this study, we demonstrated the critical role of the WO_{3-x} interfacial layer in enhancing the thermal stability and ferroelectric performance of ultrathin $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based capacitors. The incorporation of WO_{3-x}, regardless of the deposition method and with carefully tuned oxygen vacancies, effectively suppressed the transition toward antiferroelectric-like behavior at elevated temperatures and enabled nearly wake-up-free operation with significantly fewer bipolar cycles. This improvement is attributed to the reduced relative Helmholtz energy for the orthorhombic phase in the presence of WO_{3-x}, which favors the retention of ferroelectric properties, even under thermal stress. These findings offer a promising pathway toward the realization of robust ferroelectric memories suitable for 3D memory-on-logic architectures, where reliable high-temperature operation is essential.

METHODS

Device Fabrication

Ferroelectric HZO capacitors were fabricated on p^+ Si(100) substrates with a doping concentration of 10^{20} cm^{-3}. A 20 nm W bottom electrode was deposited by using a Unifilm sputter system at a deposition rate of 200 Å. A 5 nm HZO layer was deposited using the Kurt J. Lesker ALD tool at 250°C using TDMAH and TDMAZ precursors for Hf and Zr, and H_2O as the oxidant in the Th-ALD process,directly on W in the case of reference sample. For the O_2 plasma sample, the W electrode was oxidized to form a WO_{3-x} interfacial layer through 10 cycles of oxygen plasma treatment in the ALD chamber prior to HZO deposition, ensuring no vacuum break. For the ALD WO_{3-x} samples, 20 and 30 cycles of ALD were used to deposit 5 and 6 nm WO_{3-x} layers, respectively, before depositing HZO in the Veeco Fiji G1 ALD system with a Bis(*tert*-butylimino)bis(dimethylamino) (BTBMW) tungsten precursor and O_2 plasma (300 W power, 40 sccm O_2 flow, and 5 s plasma exposure per cycle) as the oxidant at 250°C. A 70 nm W top electrode was sputtered onto all devices, followed by rapid thermal annealing (RTA) at 550°C for 1 min in N_2 atmosphere. Finally, standard photolithography and dry etching were used to define 50 μm × 50 μm capacitor structures.

Energy-Dispersive X-ray Spectroscopy (EDS)

The EDS maps were collected using a Bruker E3DS detector with a 60 mm^2 window on cross-sectional focused ion beam (FIB)-prepared samples in a Hitachi HD-2700 STEM. The spectra were then read via Hyperspy, and background subtractions were performed by selecting one window before and one window after the peaks of interest. Peaks corresponding to Zr−Kα, W-Lα, and O−Kα were used for mapping. To denoise the spectra, principal component analysis (PCA) was first applied, retaining four components, and then Online Robust Non-negative Matrix Factorization (ORNMF) was performed using these four components identified. Line scans were created at the center of the horizontal direction (x-axis) for each map with a width of 40 pixels.

X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) was conducted after depositing WO_{3-x} (either by ALD or using O_2 plasma) on a sputtered bottom W electrode on a Si substrate. A Thermo K-alpha XPS system with an Al Kα X-ray source and a beam spot size of 200 μm was used for the scan. The flood gun was always on during data acquisition. XP emission peaks are charge-corrected to the carbon 1s peak which is set at 284.8 eV. XP emission backgrounds are subtracted with the Shirley algorithm, and the peaks are fitted with the Powell algorithm, with a convergence level <0.0001.

Grazing Incidence X-ray Diffraction (GI-XRD)

After the removal of the top electrode of the devices using W etchant, GIXRD scan was done using a RIGAKU Smartlab XE diffractometer equipped with a Cu Kα source (40 kV, 50 mA) and a HyPix-3000HE detector. In-situ high-temperature data are collected on the RIGAKU Reactor X stage. Data were acquired in the range of 27°−34°, with an incidence angle of 0.5°, a scanning step of 0.04°, and a scanning speed of 0.05°/min. O and T peaks are constrained to have a Gaussian shape and the same fwhm during deconvolution.

Electron Microscopy

Cross-sectional samples for scanning transmission electron microscopy (STEM) imaging and EDS were prepared using a Thermo Fisher Helios 5CX FIB/SEM equipped with a high-energy Focused Ion Beam (FIB) using Gallium-69 and operated at an accelerating voltage between 0.1 and 30 kV. The final polishing was performed at 10 pA and 2 kV. A Hitachi HD-2700 aberration- corrected STEM/SEM was used to capture STEM images, operated at a 200 kV accelerating voltage and a 27 mrad convergence semiangle. The spatial resolution was about 1.3 Å.

Electrical Measurements

Electrical measurements were performed using a Cascade Microtech Summit 1200K semiautomated probe station, equipped with a Keysight B1500 semiconductor device analyzer. A 20 μs triangular pulse with an amplitude of 1.8 V was applied to measure the P−V and I_{SW}−V characteristics. For bipolar cycling, 200 ns pulses with an amplitude of 1.8 V were used. PUND measurements were conducted using 10 μs trapezoidal pulses, each with 10 μs rise and fall times. All measurements were done on 50 μm × 50 μm devices.

Density Functional Theory (DFT)

Density functional theory (DFT) calculations were performed using the Vienna Ab initio Simulation Package (VASP).[54−57] The electron−core interactions were described using the local density approximation (LDA)[58,59] in conjunction with Blöchl's projector augmented wave (PAW) method.[57,60] A plane-wave cutoff energy of 500 eV was employed, and k-point meshes were sampled using the Monkhorst−Pack (MP)[61] method with an 8 × 8 × 8 grid for conventional unit cells. Atomic positions were fully relaxed until the total energy and interatomic forces converged to less than 10^{-8} and 0.01 eV/Å, respectively. Vibrational free energies were obtained using the finite displacement method as implemented in Phonopy,[62] which enabled

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accurate computation of the Helmholtz free energy. The surface energies were calculated using slab models comprising more than 8 layers with a vacuum region thicker than 15 Å. For slab calculations, the k-point meshes of the MP method with a $6 \times 6 \times 1$ grid were used. The film thickness was set to 5 nm. The Helmholtz free energy F was calculated using the following relation:

$$F = U + F^{vib} + \gamma\Omega$$

where U is the internal energy of the bulk system, F^{vib} is the vibrational free energy, γ is the surface energy, and Ω is the surface area.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.5c02359.

> XPS of 5 nm ALD-based WO_{3-x}; endurance; imprint; retention; conductivity; pristine $P-V$ and $I_{SW}-V$ characteristics of 5 nm ALD-based WO_{3-x} device; deconvoluted GI-XRD peaks of 125°C measurement; lattice mismatch% of HZO with W, WO_3, and single vacancy-contained WO_3; STEM image of WO_3; $I_{SW}-V$ and $P-V$ of 5 nm ALD WO_{3-x} device at 85 and 125° C; $I_{SW}-V$ of 6 nm ALD-based WO_{3-x} device when cooled back to RT from 85 and 125° C; leakage and trap generation rate with cycling; energy barrier of HZO phase transition; vibrational entropies of W and WO_3; switching barrier energy with and without WO_3. (PDF)

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Author Contributions

[∇]N.A. and J.C. contributed equally to this work. N.A. designed and performed the experiments and analyzed the results. J.C. and C.H.K. performed DFT calculations and analysis. S.S. and Y.-H.K. fabricated the devices. S.S., J.C., M.T., C.Z., and P.G.R. assisted with the experiments and data analysis. A.K. and J.H.L. supervised the research. N.A. and J.C. wrote the manuscript with the inputs from all the authors.

Notes

The authors declare no competing financial interest.

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