Impedance Spectroscopy of Ferroelectric Capacitors and Ferroelectric Tunnel Junctions

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***Abstract*— Ferroelectric devices are currently considered as a viable option for ultra-low power computing, thanks to their ability to act as memory units and synaptic weights in brain-inspired architectures. A common methodology to assess their response in different conditions (especially the role of material composition and charge trapping in ferroelectric switching) is impedance spectroscopy. However, test devices may be affected by the parasitic impedance of the metal lines contacting the electrodes of the device, which may alter the measured response and the results interpretation. In this work, we investigate the frequency response at different voltages of ferroelectric tunnel junction (FTJ) having a metal-dielectric-ferroelectric-metal (MDFM) stack, starting from the analysis of single layer capacitors (MFM and MDM). A simple but reliable method, validated by physics-based simulations, is proposed to estimate and remove the parasitic access impedance contribution, revealing the intrinsic device response. The method is used to quantify the intrinsic device-level variability of FTJs and to highlight for the first time the relation between the thickness of the dielectric layer, the phase composition of the ferroelectric, and the magnitude of the peak in the frequency response, usually thought as related to charge trapping only.**

Keywords – Ferroelectric Tunnel Junction, Capacitance, Small signal model, Neuromorphic.

I. INTRODUCTION

Ultra-low power computing is becoming an ever-increasing urge in order to manage the enormous amount of data in all sectors in an efficient and sustainable way. Thus, innovative circuit designs [1]–[3] and emerging memory concepts [4]–[6] are currently actively investigated to overcome the CMOS limitations and comply with the high density and fast data storage needs, building the foundations for logic in memory [7]–[9] and brain-inspired computing [10]–[12]. Among the explored solutions, some of the candidates to lead the required technological transition can be found in ferroelectric hafnium zirconium oxide (HZO) based devices [13]–[15] combining low power consumption, fast access speeds, high-scalability, and non-volatility. In particular, ferroelectric tunnel junction (FTJ) memories, studied in this work, consist in a metal-dielectric-ferroelectric-metal (MDFM) stack which allows for a non-destructive read-out [16], [17] and a good ability to replicate synaptic plasticity in neuromorphic circuits [18]–[20]. The device remnant polarization can be read by sensing the leakage current upon the application of a small voltage pulse and is used to store information. Depending on the desired application, these devices can be used at different speeds and voltage ranges [21], [22]; a detailed and comprehensive electrical characterization is then required for a dependable introduction of these elements in actual circuits.

A common methodology to investigate their response in different conditions (especially the role of each layer of the MDFM stack and charge trapping in ferroelectric switching) is impedance spectroscopy [23]. In particular, a common parameter used to estimate the trapped charge response is the G_p/ω peak [24], where G_p is the equivalent conductance in the total admittance of the device under test ($Y(\omega) = j\omega C_p // G_p$) obtained performing capacitance-frequency/conductance-frequency (C-f/G-f) measurements. However, especially in lab-level samples, test devices may be strongly affected by the parasitic impedance of the metal lines contacting the electrodes of the device, which may alter the measured response and the interpretation of the results [25].

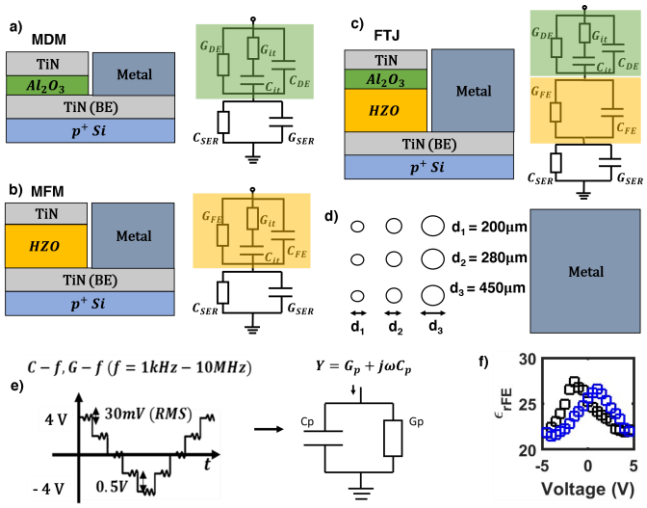

Fig. 1 – Sectional schematic and relative small-signal model of our (a) MDM, (b) MFM, and (c) FTJ. For each device, the BE is in common and can be reached by a common metal pad. d) Top view, showing devices with different area. e) Multi-voltage C-f/G-f measure. For each bias, a small ac signal (30mV) with frequencies from 1kHz to 10MHz is superimposed. The total measured admittance ($Y(\omega) = j\omega C_p//G_p$) is analysed with the models a-b-c. f) Example of $\epsilon_{r_{FE}}(V)$ extracted by the model for different polarizations (-3V to +3V in blue, +3V to -3V in black).

In this work, we extend our previous results on FTJ model validation [26], that can be also used to get insights into aging mechanisms [27], by investigating the frequency response at different voltages by means of multi-voltage C-f/G-f measurements (Fig. 1e) on FTJs having an MDFM stack, comparing the results with the analysis of single layer capacitors (MFM and MDM). The small signal models for each stack (Fig. 1 a-b-c) account for: *i)* separate leakage and capacitance paths for each layer *ii)* a first order traps contribution and *iii)* an equivalent parasitic impedance (Z_{SER}) in series with the device. The extracted Z_{SER} parameters (C_{SER} and G_{SER}), validated by physics-based simulation with Ginestra® simulation platform [28], are then removed to

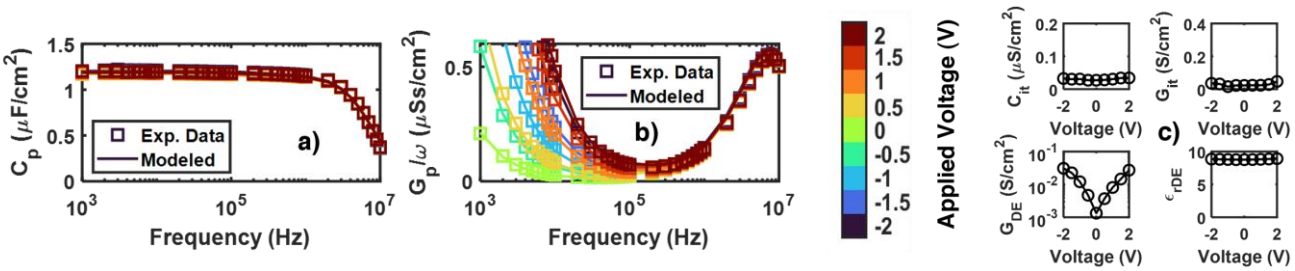

Fig. 2 – a-b) Experimental C_p and G_p/ω values (symbols) and model predictions (lines) at different voltages for an MDM capacitor with t_{DE} = 6nm. c) Voltage dependence of the extracted model parameters, i.e., the small-signal trap response (C_{it} and G_{it}), G_{DE}, and ϵ_{rDE}.

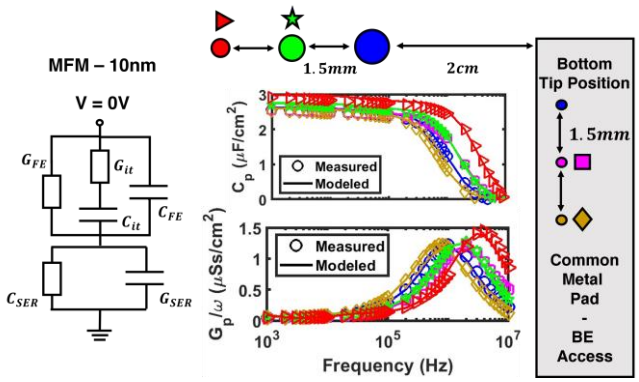

Fig. 3 – MFM variability obtained by measuring capacitors with different areas and different bottom probe positions. Experimental data (symbols) at 0V are reproduced by the small-signal model (lines). Devices with different areas (blue, green, red) are measured with the same bottom tip position (blue), while the device with the largest area (blue) is measured with three different bottom tip positions (blue, magenta, amber).

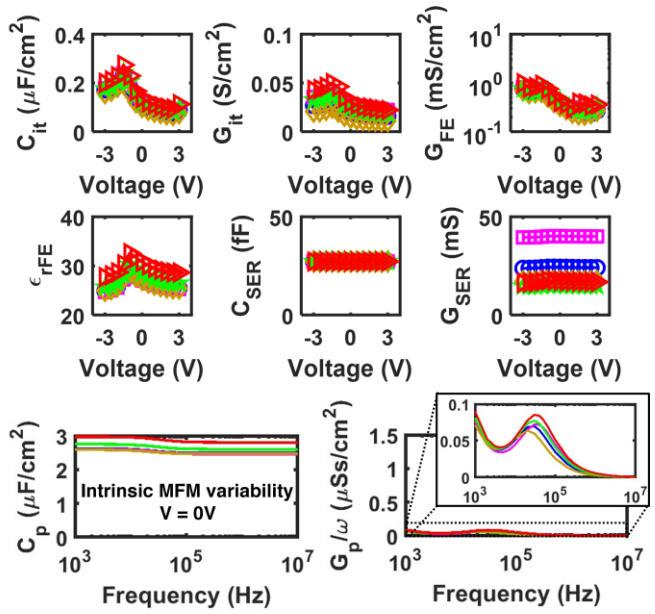

Fig. 4 – Extracted MFM model parameters and intrinsic response of Fig. 3 devices, obtained by removing the series impedance component (C_{SER} and G_{SER}) from the MFM model.

reveal the actual intrinsic response and the device-to-device variability.

The paper is organized as follows: Section II presents the details of the experiments and the studied devices, together with their small-signal model and considered physical properties. In Section III we analyse the results obtained by measuring single-layer capacitors (MDM and MFM), the validation of the extracted Z_{SER}, and the intrinsic device-level variability. In Section IV we show the outcomes from the same study on FTJs. In Section V we then compare and discuss the relation found by varying the dielectric and ferroelectric thicknesses (t_{DE} and t_{FE}) in intrinsic FTJ devices. Conclusions follow.

II. Device and Experiments

We study MFM, MDM, and FTJ frequency response by performing multi-voltage C-f/G-f measurements, as shown in Fig. 1e. The FTJs consist of a TiN/Al_2O_3(DE)/HZO(FE)/TiN stack, with 10nm HZO and different dielectric thicknesses (2-2.5-3-3.5nm). MFM has t_{FE} = 10nm while MDM have t_{DE} = 6-8-10nm. Details of the fabrication process are reported in [16]. The cross-sectional schematics and their top view are shown in Fig. 1a-b-c-d. All devices, provided by NaMLab, cons in capacitors with a shared bottom TiN electrode (BE) that can be contacted via a metal pad. C-f/G-f measurements are executed by applying a stair-case voltage ramp (MFM: [-3 +3] V, MDM: [-2 +2] V, FTJ: [-4 4] V, step 0.5 V), superposing, for each bias, a 30mV RMS ac signal with frequency sweeping from 1kHz to 10MHz. For all devices, we limited the bias to a safe range, in order to prevent device degradation and, ultimately, device breakdown. Fig. 1a-b-c shows also, for each device, the compact small-signal model used to map the total measured admittance (the parallel of an overall measured capacitance, C_p, and conductance, G_p) to specific layer-related parameters, Fig. 1e. The model accounts for a capacitance and conductance path for each layer (to separately consider the leakage of each layer), and a series impedance Z_{SER} (C_{SER}, G_{SER}) to model the parasitic impedance of the access metal lines, which cannot be removed with open-circuit and/or short-circuit compensation [25], which are however performed before the measurements. A C_{it}-G_{it} branch is also inserted between the TiN electrodes (for MFM and MDM) to model to the first order the presence of interface defects at the parasitic TiON / TiAlO layers caused by post-deposition annealing [16], [29]. To simplify the overall FTJ model, we included only a single C_{it}-G_{it} branch across DE to consider the equivalent effect of all interface's defects (M-DE, DE-FE, FE-M), as they are most likely mainly located at the DE-FE interface [30], [31]. Different other attempts in positioning this branch have been tried, without meaningful and relevant results [26]. Though the model can, with no a priori constraints, reproduce the expected voltage dependence of all parameters for different polarizations (e.g., the typical butterfly-shaped ferroelectric permittivity, ϵ_{rFE}, vs. voltage relation [29], Fig. 1f), the MFM and FTJ results are hereafter reported, for simplicity, only for positive polarization (i.e.,

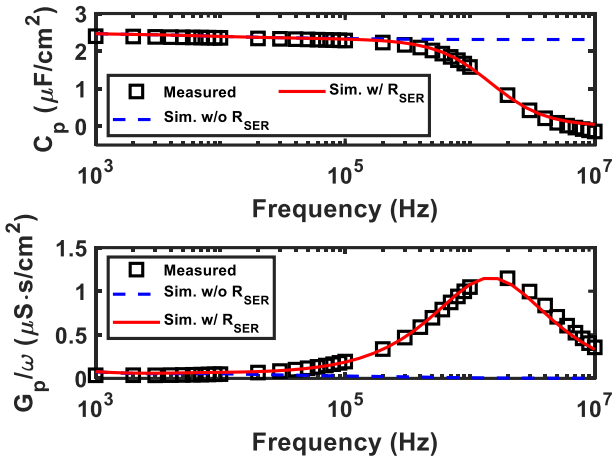

Fig. 5 – Validation of G_{SER}. Simulations of an MFM structure shows that a series conductance with a value corresponding to the extracted G_{SER} ($1/R_{SER}$) allows reproducing the measured C_p and G_p/ω profiles.

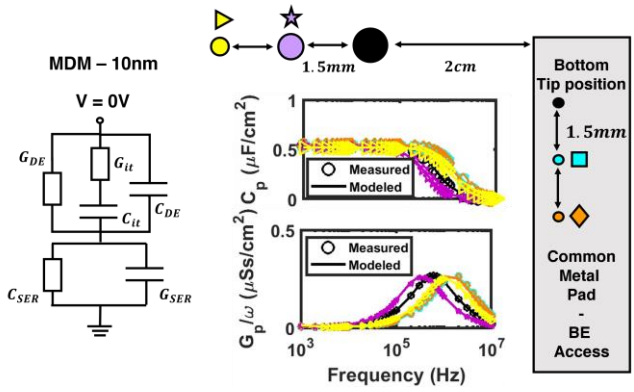

Fig. 6 – MDM with t_{DE} = 10nm measured device to device variability obtained by measuring capacitors with different areas and different bottom probe positions. Experimental data (symbols) at 0V are reproduced by the small-signal model (lines). Devices with different areas (black, purple, yellow) are measured with the same bottom tip position (black), while the device with the larger area (black) is measured with three different bottom tip positions (black, cyan, orange).

+3(4)V→-3(4)V). Notice that ϵ_{rFE} represents an effective permittivity, accounting for both orthorhombic (i.e., ferroelectric) and non-orthorhombic phases present in the FE [25], [32].

Fig. 2a-b shows the experimental C_p and G_p/ω profiles (symbols) at different voltages and the related modeling results (lines) for an MDM with t_{DE} = 6nm. Although the MDM model is able to account for the leakage (expressed as the conductance G_{DE}) voltage dependance (Fig. 2c), from now on only trends in the [0 1] V range are presented since we will focus, for simplicity, on DE parameters comparison at 0V. Furthermore, the small signal trap response is found to be weakly influenced by applied bias, which makes investigating larger voltage ranges superfluous.

III. Single Layer Capacitors

To study the materials and defects response, we initially investigate the MFM and MDM devices. Fig. 3 shows the measurement results of different MFM (symbols) at 0V, in terms of C_p and G_p/ω, together with the modeled profiles (lines). To highlight the impact of the access impedance, we measured the same device changing the tip position on the metal pad (i.e., different current paths to the capacitor), as well

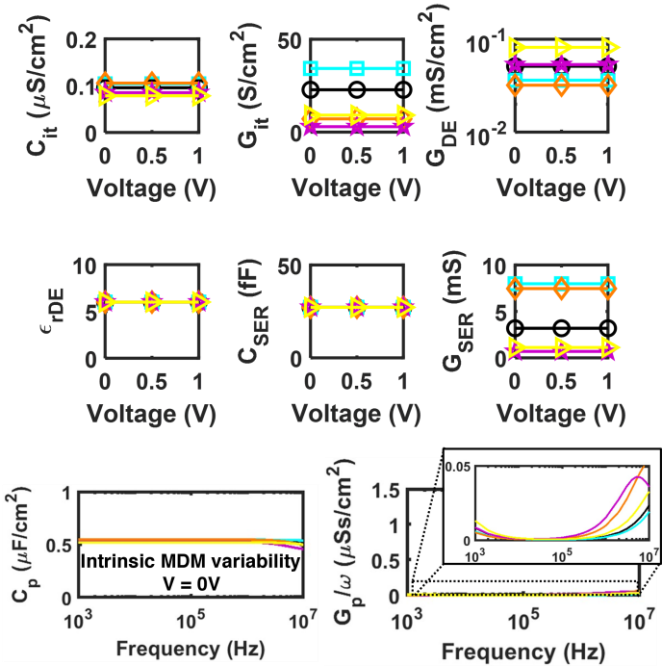

Fig. 7 – Extracted MDM model parameters and intrinsic response of Fig. 6 devices, obtained by removing the series impedance component from the MDM model.

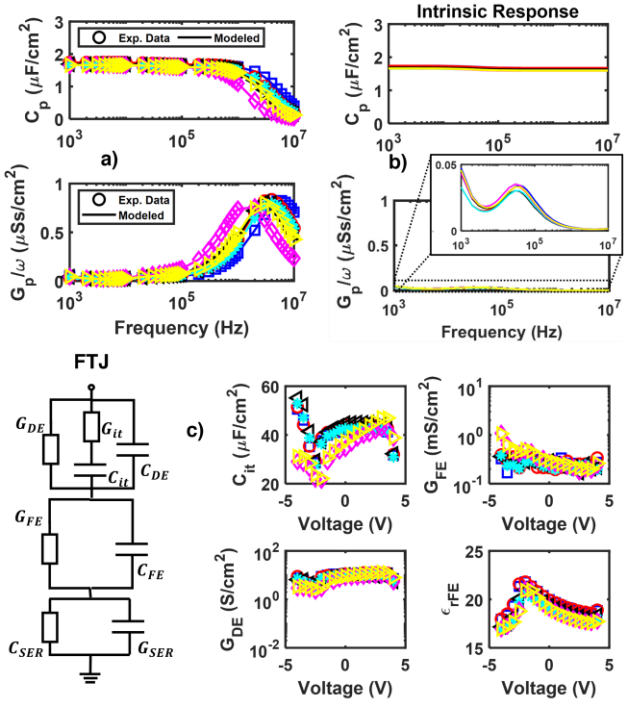

Fig. 8 – a) FTJ measured device to device variability, comparing FTJs with t_{DE} =2.5nm, with different areas and bottom tip positions. b) Intrinsic FTJ frequency response, revealing the actual variability. c) FTJ small signal model and extracted parameters of interest.

as devices with different areas keeping the tip position on the metal pad fixed. Fig. 4 reports the extracted parameters for each voltage, emphasizing a strong device-level variability only in the series conductance (G_{SER}). Removing Z_{SER} from the model and keeping the other parameters fixed, it is possible to derive the intrinsic MFM C_p and G_p/ω profiles (Fig. 4). Results show that: *i*) the intrinsic device-level dispersion is much smaller than what observed in Fig. 3; *ii*)

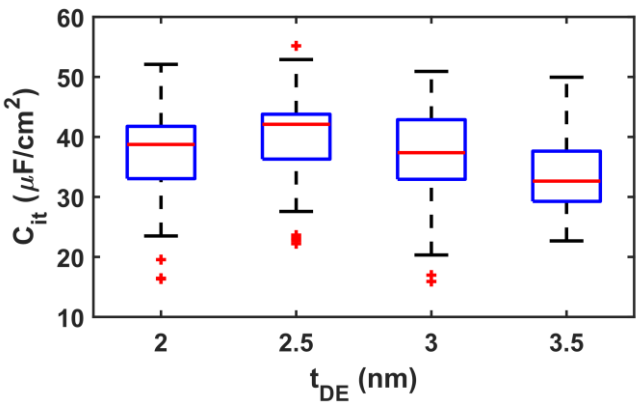

Fig. 9 – Comparison of extracted C_{it} vs. t_{DE} in FTJs. For each t_{DE}, the reported C_{it} ranges consider the parameter voltage dependence and include device-to-device variability (as in Fig. 8). No trend is found.

the high-frequency C_p roll-off is due to the access impedance and the intrinsic C_p profile is, as expected, frequency-independent [33]; *iii*) the peak in the intrinsic G_p/ω profile, usually related to defects response [24], was hidden by the access impedance. The real one is much lower than that observed in Fig. 3 and occurs at lower frequencies. Notably, the extracted Z_{SER} value is validated by independent C-f/G-f simulations of a 10nm MFM using Ginestra® simulation platform [28]. Results in Fig. 5, for simplicity only at 0V using ϵ_{rFE}(0V) = 26 (from model extraction), show that the measured C_p and G_p/ω profiles can be only reproduced by including a parasitic conductance equal to the extracted G_{SER}, while simulations without the parasitic conductance show very similar profiles to those of the intrinsic MFM in Fig. 4. The same experiments are also repeated for different MDM stacks (Fig. 6-7), revealing the intrinsic behavior of these capacitors, which show a defects response in the G_p/ω profile at much higher frequencies compared to the MFM. Differently form Fig. 2, which reports results for MDM with t_{DE} = 6nm, Fig. 7 shows that 10nm MDMs present much lower (as expected) G_{DE}s in [0 1] V. The trend is almost constant with the applied bias most probably because of the noise floor limitation of the measurement setup, and indeed G_{DE} increases at larger voltages (not shown) in agreement with the trends in Fig. 2. As for thinner MDM, traps response is still weakly dependent on bias.

IV. Ferroelectric Tunnel Junctions

Results on MFM and MDM structures allow now to better interpret the response measured on FTJs. Fig. 8a reports the results for an FTJ with t_{DE} = 2.5nm at 0V, for devices with different areas and tips positions. Also in this case, it is possible to extract the intrinsic profiles, reported in Fig. 8c. As expected, G_{FE} values (Fig. 8b) are similar to those of the MFM, since t_{FE} is 10nm for both devices, while the similarity of G_p/ω peaks (frequency and peak values) with those in MFM devices shows that the intrinsic FTJ response is much more sensitive to defects in the FE rather than to those in the DE or at the FE/DE interface.

V. Discussion

Repeating the experiments for FTJs with different t_{DE}, it is possible to compare the extracted parameters and devices response with those of the MFM and MDM capacitors. As

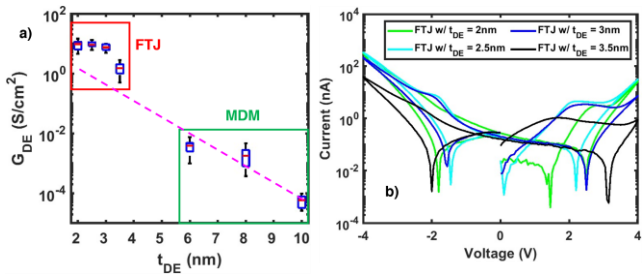

Fig. 10 – a) G_{DE} vs. t_{DE} in MDM and FTJs. FTJs present higher than expected G_{DE} values, highlighting the increase (and saturation) of DE defectivity with reducing its thickness. b) Slow IV measurements (execution time = 132s) with a reduced capacitive (dV/dt) contribution emphasize the current similarity for FTJ with $t_{DE} \leq$ 3nm, confirming the findings in (a).

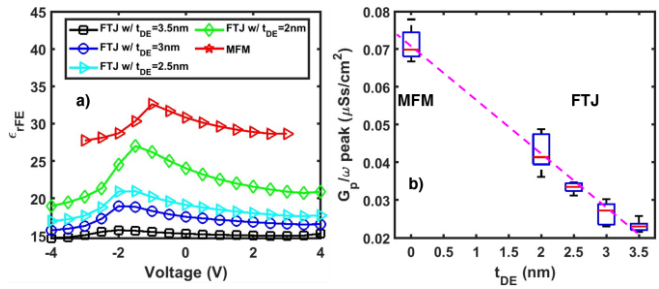

Fig. 11 – a) Extracted ϵ_{rFE} voltage dependence for MFM and FTJs with different t_{DE}. Thicker DE corresponds to lower and more compact profiles. This suggests a relation between larger t_{DE} and a stronger inhibition of the orthorhombic phase formation, confirmed also by b) in which the trend of G_p/ω peaks vs. t_{DE} is shown.

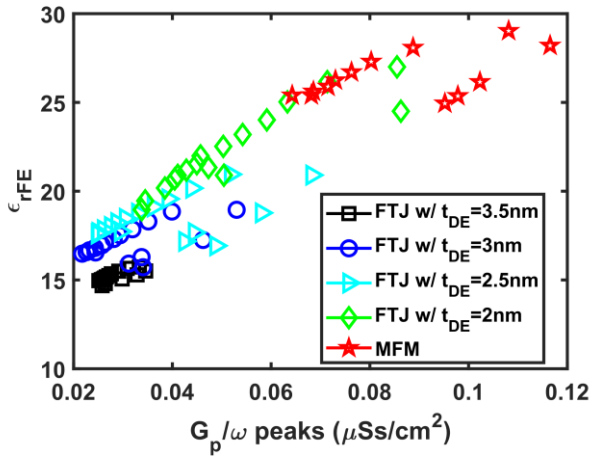

Fig. 12 – ϵ_{rFE} vs. G_p/ω peaks for MFM and FTJs with different t_{DE} shows a linear trend.

reported in Fig. 9, the extracted C_{it} values show no trend with t_{DE}, indicating a negligible relation between the DE-FE interface impurities and DE thickness.

Fig. 10a reports the G_{DE} vs. t_{DE} exponential trend obtained by interpolating the values extracted for different MDM capacitors, compared with those extracted from FTJs. The latter show higher than expected values with a very mild dependence on t_{DE}. This is also confirmed by ultra-low frequency IV measurements (execution time = 132s), Fig. 10b, which reveal that FTJs with $t_{DE} \leq$ 3nm all have similar leakage. This confirms that the ultra-thin DE layer in FTJs is highly defective and dominated by impurities probably out-diffusing from the interfaces with the top TiN electrode and the FE.

However, t_{DE} is found to modulate the FE properties, specifically the voltage dependence of ϵ_{rFE} and the G_p/ω peak.

Fig. 11a shows that increasing t_{DE} results in lower and more compact ϵ_{rFE} profiles, suggesting that a thicker DE can inhibit the orthorhombic phase formation during the annealing process, affecting the switching. Furthermore, the effect of t_{DE} is also visible in the analysis of the G_p/ω peaks at 0V, as reported in Fig. 11b, suggesting an inverse relation between t_{DE} and ferroelectric domain response.

The extracted trend, confirmed by the comparison with the MFM case, shows that the G_p/ω peak is not only related to defects as usually thought [24], but is also related to the FE phase composition. A linear relation is found between the G_p/ω peaks and ϵ_{rFE} for all t_{DE}, as shown in Fig. 12, stressing the role of FE properties on G_p/ω response [27]. Thus, extra care must be adopted when assessing the interface trap density based on G_p/ω peaks [24].

VI. Conclusions

In this work, we introduced and validated an advanced FTJ small-signal compact model that accounts for separate leakage contributions in the FE and DE layers, the contribution of a parasitic series impedance, and non-uniform crystalline FE phase. The model correctly reproduces measurements taken on different devices in different conditions and with different tips position, allowing a more refined investigation on sample layout and material properties effects on the entire device under measurement. In particular, the possibility to isolate and remove the parasitic impedance between the actual device and the bottom tip, validated by physics-based simulation in Ginestra® simulation platform [28], allows the analysis of the desired intrinsic devices properties and variability.

Results are obtained by comparing the study of single layer MFM and MDM capacitor with MDFM FTJs. The insertion of t_{DE} in FTJs, although weakly effective in leakage control due to the found high defectivity, is revealed to be a possible cause for inhibiting the ferroelectric orthorhombic phase formation in HZO layer. The latter, that is strictly related to ϵ_{rFE}, is also found to be approximately linearly related to the peak value of the G_p/ω vs. f curve, suggesting that the typically adopted estimation methods for interface trap density may be misleading.

Acknowledgments

The authors would like to express gratitude to NaMLab for providing the devices. They also acknowledge Applied Materials Italy for their support with Ginestra® device simulation software [28]. The work is funded by the H2020 BeFerroSynaptic (GA 871737) project. The content reflects the authors' results, but not necessarily the opinion of the EC.

References

[1] G. Indiveri and S. C. Liu, "Memory and Information Processing in Neuromorphic Systems," *Proceedings of the IEEE*, vol. 103, no. 8. 2015. doi: 10.1109/JPROC.2015.2444094.

[2] T. Zanotti, F. M. Puglisi, and P. Pavan, "Smart Logic-in-Memory Architecture for Low-Power Non-Von Neumann Computing," *IEEE Journal of the Electron Devices Society*, vol. 8, 2020, doi: 10.1109/JEDS.2020.2987402.

[3] W. Wan *et al.*, "A compute-in-memory chip based on resistive random-access memory," *504 | Nature |*, vol. 608, 2022, doi: 10.1038/s41586-022-04992-8.

[4] M. le Gallo and A. Sebastian, "An overview of phase-change memory device physics," *Journal of Physics D: Applied Physics*, vol. 53, no. 21. 2020. doi: 10.1088/1361-6463/ab7794.

[5] F. Zahoor, T. Z. Azni Zulkifli, and F. A. Khanday, "Resistive Random Access Memory (RRAM): an Overview of Materials, Switching Mechanism, Performance, Multilevel Cell (mlc) Storage, Modeling, and Applications," *Nanoscale Research Letters*, vol. 15, no. 1. 2020. doi: 10.1186/s11671-020-03299-9.

[6] M. Lanza *et al.*, "Memristive technologies for data storage, computation, encryption, and radio-frequency communication," *Science*, vol. 376, no. 6597. American Association for the Advancement of Science, Jun. 03, 2022. doi: 10.1126/science.abj9979.

[7] S. Kvatinsky, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based material implication (IMPLY) logic: Design principles and methodologies," *IEEE Trans Very Large Scale Integr VLSI Syst*, vol. 22, no. 10, 2014, doi: 10.1109/TVLSI.2013.2282132.

[8] E. Lehtonen and M. Laiho, "Stateful implication logic with memristors," 2009. doi: 10.1109/NANOARCH.2009.5226356.

[9] T. Zanotti, P. Pavan, and F. M. Puglisi, "micromachines Multi-Input Logic-in-Memory for Ultra-Low Power Non-Von Neumann Computing," 2021, doi: 10.3390/mi12101243.

[10] G. Indiveri *et al.*, "Neuromorphic silicon neuron circuits," *Frontiers in Neuroscience*, no. MAY. 2011. doi: 10.3389/fnins.2011.00073.

[11] D. Gandolfi, F. M. Puglisi, G. M. Boiani, G. Pagnoni, K. J. Friston, and J. Mapelli, "Emergence of associative learning in a neuromorphic inference network," 2022, doi: 10.1088/1741-2552/ac6ca7.

[12] D. v Christensen *et al.*, "2022 roadmap on neuromorphic computing and engineering," *Neuromorphic Computing and Engineering*, vol. 2, no. 2, 2022, doi: 10.1088/2634-4386/ac4a83.

[13] R. Materlik, C. Kunneth, and A. Kersch, "The origin of ferroelectricity in Hf1-xZrxO2: A computational investigation and a surface energy model," *J Appl Phys*, vol. 117, no. 13, 2015, doi: 10.1063/1.4916707.

[14] S. J. Kim, J. Mohan, S. R. Summerfelt, and J. Kim, "Ferroelectric Hf0.5Zr0.5O2 Thin Films: A Review of Recent Advances," *JOM*, vol. 71, no. 1. 2019. doi: 10.1007/s11837-018-3140-5.

[15] R. Yang, "In-memory computing with ferroelectrics," *Nature Electronics*, vol. 3, no. 5. 2020. doi: 10.1038/s41928-020-0411-2.

[16] B. Max, M. Hoffmann, S. Slesazeck, and T. Mikolajick, "Direct Correlation of Ferroelectric Properties and Memory Characteristics in Ferroelectric Tunnel Junctions," *IEEE Journal of the Electron Devices Society*, vol. 7, 2019, doi: 10.1109/JEDS.2019.2932138.

[17] B. Max, T. Mikolajick, M. Hoffmann, and S. Slesazeck, "Retention characteristics of Hf0.5Zr0.5O2-based ferroelectric tunnel junctions," 2019. doi: 10.1109/IMW.2019.8739765.

[18] S. Oh, H. Hwang, and I. K. Yoo, "Ferroelectric materials for neuromorphic computing," *APL Mater*, vol. 7, no. 9, 2019, doi: 10.1063/1.5108562.

[19] L. Bégon-Lours *et al.*, "Scaled, Ferroelectric Memristive Synapse for Back-End-of-Line Integration with Neuromorphic Hardware," *Adv Electron Mater*, vol. 8, no. 6, 2022, doi: 10.1002/aelm.202101395.

[20] T. Ali *et al.*, "Impact of the Ferroelectric and Interface Layer Optimization in an MFIS HZO based Ferroelectric Tunnel Junction for Neuromorphic based Synaptic Storage," 2021. doi: 10.1109/SNW51795.2021.00032.

[21] M. Dragoman, M. Aldrigo, D. Dragoman, S. Iordanescu, A. Dinescu, and M. Modreanu, "HfO2-Based Ferroelectrics Applications in Nanoelectronics," *Physica Status Solidi - Rapid Research Letters*, vol. 15, no. 5, 2021, doi: 10.1002/pssr.202000521.

[22] K. Y. Hsiang *et al.*, "Ferroelectric HfZrO2with Electrode Engineering and Stimulation Schemes as Symmetric Analog Synaptic Weight Element for Deep Neural Network Training," *IEEE Trans Electron Devices*, vol. 67, no. 10, 2020, doi: 10.1109/TED.2020.3017463.

[23] A. R. West, D. C. Sinclair, and N. Hirose, "Characterization of Electrical Materials, Especially Ferroelectrics, by Impedance Spectroscopy," Kluwer Academic Publishers, 1997.

[24] Y. Qu, J. Li, M. Si, X. Lyu, and P. D. Ye, "Quantitative Characterization of Interface Traps in Ferroelectric/Dielectric Stack Using Conductance Method," *IEEE Trans Electron Devices*, vol. 67, no. 12, 2020, doi: 10.1109/TED.2020.3034564.

[25] L. Benatti and F. M. Puglisi, "Understanding the Reliability of Ferroelectric Tunnel Junction Operations using an Advanced Small-Signal Model," in *IEEE International Integrated Reliability Workshop Final Report*, 2021, vol. 2021-October. doi: 10.1109/IIRW53245.2021.9635621.

[26] L. Benatti and F. M. Puglisi, "Impedance Investigation of MIFM Ferroelectric Tunnel Junction using a Comprehensive Small-Signal Model," *IEEE Transactions on Device and Materials Reliability*, 2022, doi: 10.1109/TDMR.2022.3182941.

[27] L. Benatti, P. Pavan, and F. M. Puglisi, "Combining Experiments and a Novel Small Signal Model to Investigate the Degradation Mechanisms in Ferroelectric Tunnel Junctions," in *IEEE International Reliability Physics Symposium Proceedings*, 2022, vol. 2022-March, pp. P61–P65. doi: 10.1109/IRPS48227.2022.9764602.

[28] "https://www.appliedmaterials.com/products/applied-mdlx-ginestrasimulation-software."

[29] S. J. Kim *et al.*, "Ferroelectric TiN/Hf0.5Zr0.5O2/TiN Capacitors with Low-Voltage Operation and High Reliability for Next-Generation FRAM Applications," 2018. doi: 10.1109/IMW.2018.8388832.

[30] K. Ni *et al.*, "Critical Role of Interlayer in Hf0.5Zr0.5O2 Ferroelectric FET Nonvolatile Memory Performance," *IEEE Trans Electron Devices*, vol. 65, no. 6, 2018, doi: 10.1109/TED.2018.2829122.

[31] K. Toprasertpong, M. Takenaka, and S. Takagi, "Direct Observation of Interface Charge Behaviors in FeFET by Quasi-Static Split C-V and Hall Techniques: Revealing FeFET Operation," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2019, vol. 2019-December. doi: 10.1109/IEDM19573.2019.8993664.

[32] M. Y. Kao *et al.*, "Variation Caused by Spatial Distribution of Dielectric and Ferroelectric Grains in a Negative Capacitance Field-Effect Transistor," *IEEE Trans Electron Devices*, vol. 65, no. 10, 2018, doi: 10.1109/TED.2018.2864971.

[33] B. Lin, G. Choe, J. Hur, A. I. Khan, S. Yu, and H. Wang, "Experimental RF Characterization of Ferroelectric Hafnium Zirconium Oxide Material at GHz for Microwave Applications," in *Device Research Conference - Conference Digest, DRC*, 2021, vol. 2021-June. doi: 10.1109/DRC52342.2021.9467202.