

# Hole Virtual Gate Model Explaining Surface-Related Dynamic $R_{ON}$ in p-GaN Power HEMTs

Nicolò Zagni<sup>1</sup>, Member, IEEE, Giovanni Verzellesi<sup>2</sup>, Senior Member, IEEE, Alessandro Bertacchini<sup>2</sup>, Member, IEEE, Mattia Borgarino<sup>2</sup>, Ferdinando Iucolano, and Alessandro Chini<sup>2</sup>

**Abstract**—Dynamic on-resistance ( $R_{ON}$ ) affects the stability of p-GaN power HEMTs. In Schottky-gate HEMTs, dynamic  $R_{ON}$  is associated to either electron trapping at device surface or dynamic effects occurring in the buffer. However, in p-GaN HEMTs the floating p-GaN region can have an additional role on dynamic  $R_{ON}$ , due to removal/injection of holes from/into the barrier with relatively long time constants, which can be erroneously interpreted as a reliability issue. In this letter, we present a model to explain the dynamic  $R_{ON}$  due to surface-related effects in p-GaN power HEMTs. The model, called ‘hole virtual gate’, attributes the experimentally observed  $R_{ON}$  instability due to negative/positive gate bias stress (NGS/PGS) to the charging/discharging of surface traps in the AlGaN barrier by the removal/injection of holes through the gate metal/p-GaN Schottky junction. We verify the validity of the model by means of calibrated numerical simulations, that correlate the activation energy  $E_A \approx 0.4$  eV of both  $R_{ON}$  increase/decrease during NGS/PGS to the thermal ionization energy of traps in the barrier.

**Index Terms**—p-GaN HEMTs, dynamic  $R_{ON}$ , hole virtual gate, gate bias stress, barrier traps, reliability.

## I. INTRODUCTION

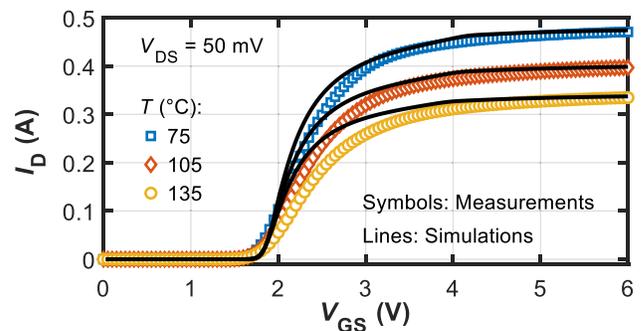
**D**YNAMIC on-resistance ( $R_{ON}$ ) is the most detrimental trapping-related effect for GaN-based devices that need to be employed in power switching converters as it determines an undesirable increase in conduction losses [1].

Manuscript received 17 January 2024; revised 23 February 2024; accepted 7 March 2024. Date of publication 11 March 2024; date of current version 26 April 2024. This work has been carried out in the framework of the European Project Gallium Nitride for Advanced Power Applications (GaN4AP). The project has received funding from the Electronic Component Systems for European Leadership Joint Undertaking (ECSEL JU), under Grant Agreement No.101007310. This Joint Undertaking receives support from the European Union’s Horizon 2020 research and innovation programme, and Italy, Germany, France, Poland, Czech Republic, Netherlands. The review of this letter was arranged by Editor G. H. Jessen. (Corresponding author: Nicolò Zagni.) Nicolò Zagni, Mattia Borgarino, and Alessandro Chini are with the Department of Engineering “Enzo Ferrari,” Università di Modena e Reggio Emilia, 41125 Modena, Italy (e-mail: nicolo.zagni@unimore.it).

Giovanni Verzellesi and Alessandro Bertacchini are with the Department of Sciences and Methods for Engineering (DISMI) and the EN&TECH Center, University of Modena and Reggio Emilia, 42122 Reggio Emilia, Italy.

Ferdinando Iucolano is with STMicroelectronics, 95121 Catania, Italy. Color versions of one or more figures in this letter are available at <https://doi.org/10.1109/LED.2024.3375912>.

Digital Object Identifier 10.1109/LED.2024.3375912



**Fig. 1.** Typical  $I_D$ - $V_{GS}$  curves obtained at  $V_{DS} = 50$  mV and  $T = 75, 105, 135$  °C, see legend. Simulated  $I_D$ - $V_{GS}$  curves obtained under the same experimental conditions are also reported, showing the good agreement obtained with experimental data.

In Schottky-gate GaN HEMTs, dynamic  $R_{ON}$  effects have been attributed to either electron trapping at the device surface (i.e., layers above the channel) – explained by the concept of virtual gate [5] – or electron [2], [3] and/or hole trapping [4] in the buffer (i.e., layer below the channel). Moreover, in p-GaN HEMTs, which is the common commercial technology option for normally-OFF operation (i.e., positive threshold voltage,  $V_T$ ) [6], the floating p-type region in the gate stack becomes a source of device instability in terms of both  $V_T$  [7], [8], [9], [10] and  $R_{ON}$  [11], [12], [13].

In this letter, we propose a model called ‘hole virtual gate’ to explain the experimentally observed dynamic  $R_{ON}$  after the application of negative/positive gate bias stress (NGS/PGS). A preliminary interpretation of gate-bias induced  $R_{ON}$  instability was provided in [11], which however lacked a quantitative model to support it. Here, the hole virtual gate model is quantitatively validated by means of numerical device simulations that reproduce the data when considering hole traps in the AlGaN barrier at 0.4 eV above the valence band edge.

## II. DEVICE CHARACTERIZATION

Devices under test (DUT’s) are 650-V p-GaN power HEMTs with Schottky gate contact. Typical drain current ( $I_D$ ) vs gate-to-source bias ( $V_{GS}$ ) characteristics at  $V_{DS} = 50$  mV at  $T = 75, 105, 135$  °C are reported in Fig. 1. The setup presented in [11] was employed to characterize the dynamics of  $R_{ON}$  instability at different temperatures.

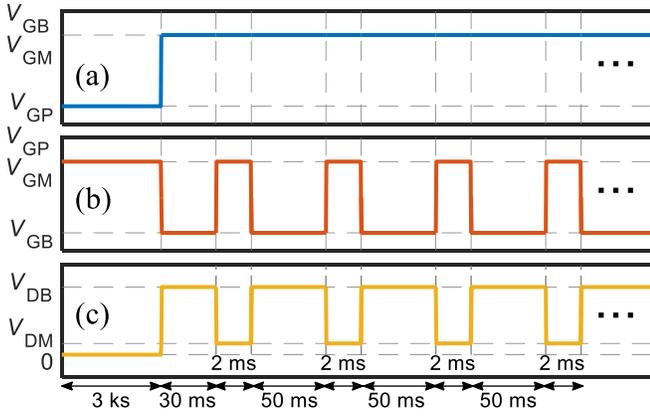


Fig. 2. Sketch of the waveforms applied at the gate and drain terminals for the characterization of  $I_D/R_{ON}$  transients in the case of (a) NGS, (b) PGS, (c) GDS. Initialization at  $(V_{GP}, 0)$  is carried out in 3 ks. Then,  $(V_{GB}, V_{DB})$  (see Fig. 3 for the values in each case) is applied for another 3 ks during which  $R_{ON}$  is periodically probed at  $(V_{GM}, V_{DM}) = (6, 0.05)$  V for 2 ms every 50 ms (the first sensing is done after 30 ms).

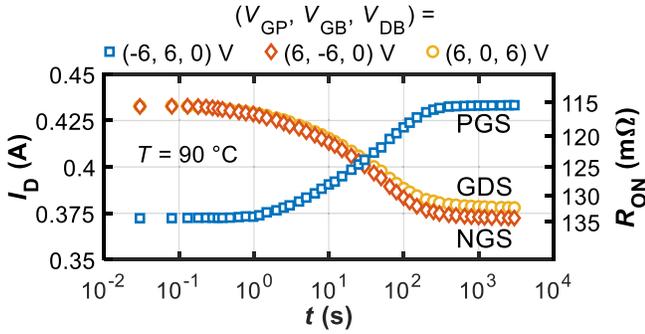


Fig. 3.  $I_D/R_{ON}$  vs time transient characterization for three different  $(V_{GP}, V_{GB}, V_{DB})$  combinations (see legend) at  $T = 90$  °C.

First, a 3-ks initialization step, performed at fixed gate bias  $(V_{GP})$ , ensures that traps are in a steady state prior to the subsequent  $I_D/R_{ON}$  transient characterization. Then,  $V_{GS}$  is set to a baseline bias  $(V_{GB})$  for 3 ks and  $I_D/R_{ON}$  is sampled every 50 ms at  $V_{GM} = 6$  V for 2 ms [11]. Fig. 2 illustrates the waveforms used during the transients characterization. Fig. 3 shows the experimental results obtained from this characterization for  $(V_{GP}, V_{GB}) = (+6, -6)$  and  $(-6, +6)$  V, which will be referred to as NGS and PGS, respectively. As can be noted,  $R_{ON}$  increases (decreases) during the NGS (PGS) transient substitute by with of  $\approx 17\%$ , from 115 to 135 m $\Omega$ , with relatively long time constant  $\approx 40$  s ( $T = 90$  °C). The  $V_{GS} < 0$  V bias condition is not incurred in power switching converters, because p-GaN HEMTs have  $V_T > 0$  V and are in the OFF-state for  $V_{GS} = 0$  V. Nevertheless, this condition is useful for two main reasons: (i) it allows to narrowing down the instability mechanisms to the exchange of carriers between the device and the gate terminal only; and (ii) it serves as a proxy for the OFF-state (in which  $V_{GD,OFF} \ll 0$  V) [1], [14]. The latter point is further confirmed by Fig. 3, showing the transient labeled as GDS (Gate Drain Stress) with  $V_{GB} = 0$  V and  $V_{DB} = +6$  V (taken after 50-minute initialization at  $V_{GP} = +6$  V with  $V_{DS} = 0$  V), which has a dynamic similar to the transient acquired during the NGS. Notice that, during both stress and measurement bias conditions are such

that self-heating can be completely neglected. For this reason,  $I_D/R_{ON}$  transients are only influenced by trap dynamics and not by the temperature dependence of static  $R_{ON}$ .

### III. HOLE VIRTUAL GATE MODEL

The observed dynamic  $R_{ON}$  can be attributed to charge/discharge of hole traps present in the AlGaIn barrier [11], [13]. Hole extraction (injection) during NGS (PGS) modulates the density of negatively charged traps in the gate-drain access region of the barrier, this in turn reflecting on the 2-DEG density underneath and thus  $R_{ON}$ . This mechanism is analogous to the ‘virtual gate’ effect related to the injection (extraction) of electrons from the gate contact in normally-ON Schottky-gate HEMTs [5]. However, in p-GaN HEMTs, it is the extraction (injection) of holes that affects  $R_{ON}$ . Numerical device simulations, carried out with SDevice<sup>TM</sup> [15], validate the model. The experimental  $I_D - V_{GS}$  curves reported in Fig. 1 were used to calibrate the simulation parameter set. More details regarding the adopted models can be found in our previous works [4], [16], [17]. Gate leakage is accounted for by thermionic emission occurring at the gate metal/p-GaN Schottky diode and hole tunneling [18]. Barrier traps are energetically located 0.4 eV above the AlGaIn valence band edge. This value was set to reproduce the extracted activation energy ( $E_A$ ) of the measured  $I_D$  transients shown in Figs. 4(b) and 5(b). Previously, we observed that the extracted  $E_A$  range is compatible with Mg out-diffused in the barrier during epitaxial growth (see [11] and references within). The modeling of traps in the simulation setup reflects this hypothesis, by assuming an exponentially decaying trap density profile within the barrier.

Figures 4(a) and 5(a) compare the experimental and simulated  $I_D/R_{ON}$  transients obtained during NGS and PGS, respectively, at different  $T$ 's. During NGS, holes emitted by barrier traps drift towards the gate contact where they get extracted by the forward-biased Schottky junction. Hole emission increases the density of negatively charged traps in the barrier ( $N_{Bar}^-$ ) thus reducing the concentration of electrons in the 2-DEG;  $R_{ON}$  therefore increases. During PGS, the opposite occurs: holes are injected from the leaky gate contact into the device [9], [18] and get trapped by barrier traps, neutralizing the negative charge and  $R_{ON}$  decreases. Figs. 4(b) and 5(b) show the Arrhenius plots extracted from the measurement and simulation results. The  $\tau$ 's are extracted from the stretched exponential fitting curves as described in [19]. The overall good agreement between measurement and simulation results validates the hole virtual gate model described previously.

Fig. 5 shows that the simulations underestimate the values of  $\tau$  for the PGS case. Because  $\tau$ 's during PGS depend on the amount of injected carriers, as discussed in [11], we attribute the discrepancy to the hole injection model by the gate contact at  $V_{GS} = +6$  V (i.e., non-local tunneling) which tends to overestimate the gate leakage current, hence accelerating hole trapping.

In [11] it was suggested that  $T$ -activation of hole trapping with the same activation energy ( $E_A \approx 0.4$  eV) as hole emission was due to the hole density  $p$  being proportional to  $\exp[-(E_T - E_V)/kT]$ , which occurs for low hole injection

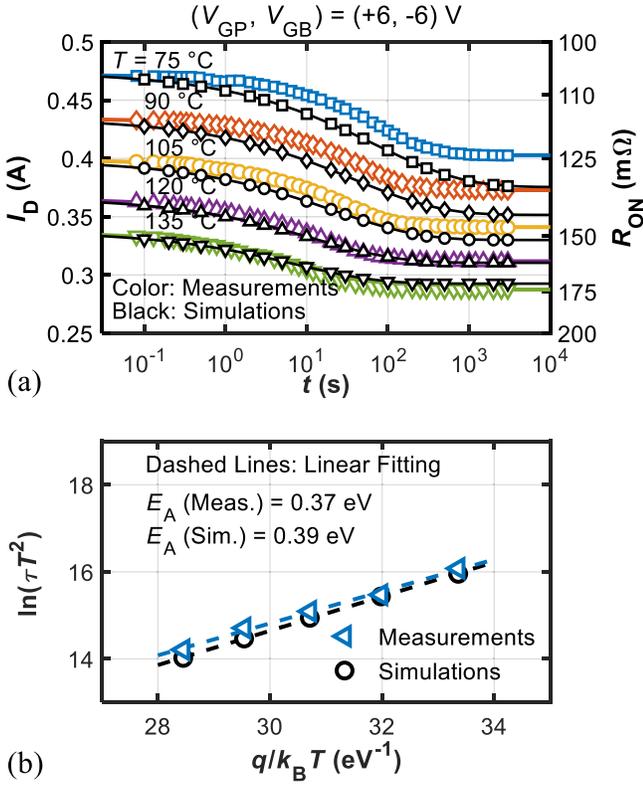


Fig. 4. (a)  $I_D/R_{ON}$  transients taken at different baseplate temperatures,  $T$ , see plot, at  $(V_{GP}, V_{GB}) = (+6, -6)$  V. (b) Arrhenius plots built from the extracted  $\tau$ 's.  $E_A$ 's extracted from the linear fitting of the data points are also indicated.

and relatively high trap concentration in the AlGa $N$  barrier [20]. The simulations support this interpretation, as  $E_A$  extracted in both NGS and PGS is about the same, see Figs. 4(b) and 5(b).

To further elucidate the hole virtual gate effect, we show in Fig. 6 the two-dimensional contour plot of  $N_{Bar}^-$  along the gate-drain access region at  $I_D/R_{ON}$  measurement conditions (i.e.,  $V_{GS} = +6$  V,  $V_{DS} = 50$  mV) after 50 minutes at (a)  $V_{GB} = -6$  V and (b)  $V_{GB} = +6$  V,  $T = 90^\circ\text{C}$ . As explained previously, during NGS  $N_{Bar}^-$  increases by emitting holes that get extracted from the device by the gate contact. As a consequence, the hole virtual gate negatively charges and extends in the gate-drain access region, see Fig. 6(a). Conversely, during PGS holes are injected by the gate contact and get trapped by the barrier traps,  $N_{Bar}^-$  reduces, and the hole virtual gate depletes (of negative charge). In both cases, resulting  $R_{ON}$  depends on the two-dimensional profile of the hole virtual gate. It is worth pointing out that, conversely to the (electron) virtual gate concept proposed in [5], here it is the extraction of holes emitted by traps that determines the formation of the virtual gate itself, which extends along the whole gate-to-drain access region where traps are assumed to be present.

We ruled out buffer trapping as possible cause for the observed dynamic  $R_{ON}$  because gate stress without drain stress is not sufficient to alter significantly the state of buffer traps. Moreover, if C-related traps were to determine the dynamic  $R_{ON}$  then  $E_A \approx 0.9$  eV should have been extracted from the Arrhenius plots [4], which is not the case.

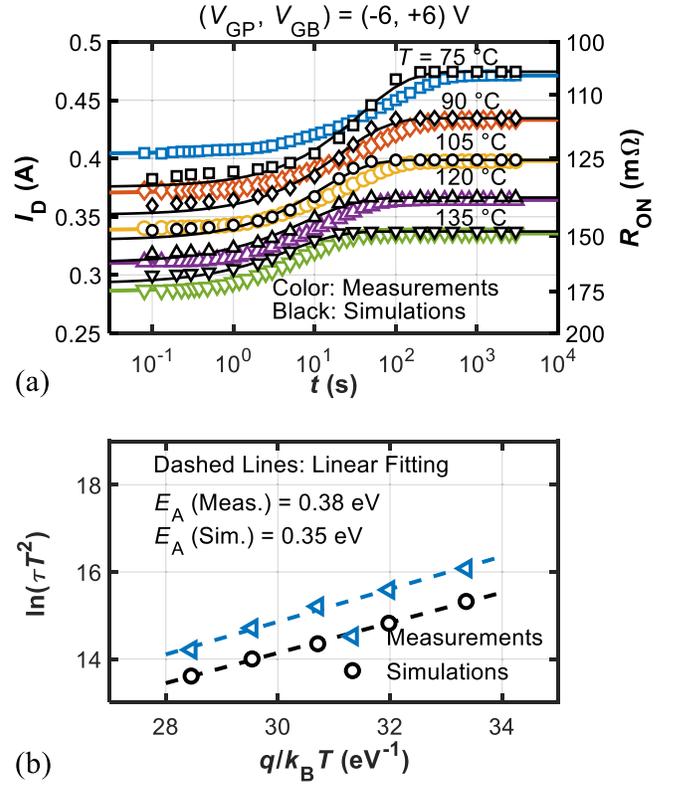


Fig. 5. (a)  $I_D/R_{ON}$  transients taken at different baseplate temperatures,  $T$ , see plot, at  $(V_{GP}, V_{GB}) = (-6, +6)$  V. (b) Arrhenius plots built from the extracted  $\tau$ 's.  $E_A$ 's extracted from the linear fitting of the data points are also indicated.

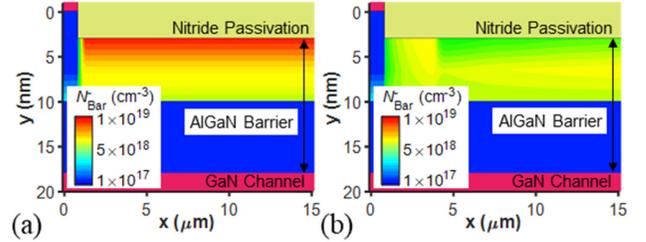


Fig. 6. Contour plot of trapped charge in the barrier ( $N_{Bar}^-$ ) at  $I_D/R_{ON}$  measurement conditions (i.e.,  $V_{GS} = +6$  V,  $V_{DS} = 50$  mV) after 50 minutes at (a)  $V_{GB} = -6$  V and (b)  $V_{GB} = +6$  V,  $T = 90^\circ\text{C}$ . Barrier traps charge (discharge) during  $V_{GB} = -6$  V ( $V_{GB} = +6$  V) due to the extraction (injection) of holes by the gate contact on the p-GaN layer, causing the charging (depletion) of the virtual gate in the gate-drain access region.

#### IV. CONCLUSION

We proposed a hole virtual gate model to explain the dynamic  $R_{ON}$  in p-GaN power HEMTs induced by gate bias stress. The model attributes the observed instabilities to the extraction (injection) of holes from the p-GaN gate and to the consequent emission (capture) of holes in barrier traps within the gate-drain access region. The comparison between experimental results and calibrated simulations validates the model. We attributed the activation energy  $E_A \approx 0.4$  eV, extracted from the  $R_{ON}$  transients during stress, to the thermal ionization energy of traps in the barrier.

#### ACKNOWLEDGMENT

The authors thanks L. Selmi (University of Modena and Reggio Emilia) for the fruitful discussions.

## REFERENCES

- [1] M. Meneghini, C. De Santi, I. Abid, M. Buffolo, M. Cioni, R. A. Khadar, L. Nela, N. Zagni, A. Chini, F. Medjdoub, G. Meneghesso, G. Verzellesi, E. Zanoni, and E. Matioli, "GaN-based power devices: Physics, reliability, and perspectives," *J. Appl. Phys.*, vol. 130, no. 18, p. 227, Nov. 2021, doi: [10.1063/5.0061354](https://doi.org/10.1063/5.0061354).
- [2] S. D. Gupta, V. Joshi, R. R. Chaudhuri, and M. Shrivastava, "Part I: Physical insights into dynamic  $R_{ON}$  behavior and a unique time-dependent critical stress voltage in AlGaIn/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5720–5727, Nov. 2021, doi: [10.1109/TED.2021.3109847](https://doi.org/10.1109/TED.2021.3109847).
- [3] N. Zagni, V. Z. Gao, G. Verzellesi, A. Chini, A. Pantellini, M. Natali, A. Lucibello, L. Latessa, C. Lanzieri, C. De Santi, M. Meneghini, G. Meneghesso, and E. Zanoni, "Mechanisms of step-stress degradation in carbon-doped 0.15- $\mu\text{m}$  AlGaIn/GaN HEMTs for power RF applications," *IEEE Trans. Device Mater. Rel.*, vol. 23, no. 4, pp. 453–460, Dec. 2023, doi: [10.1109/dmr.2023.3305033](https://doi.org/10.1109/dmr.2023.3305033).
- [4] N. Zagni, A. Chini, F. M. Puglisi, M. Meneghini, G. Meneghesso, E. Zanoni, P. Pavan, and G. Verzellesi, "'Hole redistribution' model explaining the thermally activated  $R_{ON}$  stress/recovery transients in carbon-doped AlGaIn/GaN power MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 2, pp. 697–703, Feb. 2021, doi: [10.1109/TED.2020.3045683](https://doi.org/10.1109/TED.2020.3045683).
- [5] F. Roccaforte, G. Greco, P. Fiorenza, and F. Iucolano, "An overview of normally-off GaN-based high electron mobility transistors," *Materials*, vol. 12, no. 10, p. 1599, May 2019, doi: [10.3390/ma12101599](https://doi.org/10.3390/ma12101599).
- [6] A. Stockman, E. Canato, M. Meneghini, G. Meneghesso, P. Moens, and B. Bakeroot, "Threshold voltage instability mechanisms in p-GaN gate AlGaIn/GaN HEMTs," in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2019, pp. 287–290, doi: [10.1109/ISPSD.2019.8757667](https://doi.org/10.1109/ISPSD.2019.8757667).
- [7] L. Efthymiou, K. Murukesan, G. Longobardi, F. Udrea, A. Shibib, and K. Terrill, "Understanding the threshold voltage instability during OFF-state stress in p-GaN HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1253–1256, Aug. 2019, doi: [10.1109/LED.2019.2945776](https://doi.org/10.1109/LED.2019.2945776).
- [8] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, and G. Curatola, "Threshold voltage instability in p-GaN gate AlGaIn/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2454–2460, Jun. 2018, doi: [10.1109/TED.2018.2828702](https://doi.org/10.1109/TED.2018.2828702).
- [9] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic  $R_{ON}$  characterization and circuit design considerations," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017, doi: [10.1109/TPEL.2016.2610460](https://doi.org/10.1109/TPEL.2016.2610460).
- [10] A. Chini, N. Zagni, G. Verzellesi, M. Cioni, G. Giorgino, M. C. Nicotra, M. E. Castagna, and F. Iucolano, "Gate-bias induced  $R_{ON}$  instability in p-GaN power HEMTs," *IEEE Electron Device Lett.*, vol. 44, no. 6, pp. 915–918, Jun. 2023, doi: [10.1109/LED.2023.3265503](https://doi.org/10.1109/LED.2023.3265503).
- [11] N. Zagni, M. Cioni, M. E. Castagna, M. Moschetti, F. Iucolano, G. Verzellesi, and A. Chini, "Symmetrical  $V_{TH}/R_{ON}$  drifts due to negative/positive gate stress in p-GaN power HEMTs," in *Proc. IEEE 9th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Redondo Beach, CA, USA, Nov. 2022, pp. 31–34, doi: [10.1109/WiPDA56483.2022.9955267](https://doi.org/10.1109/WiPDA56483.2022.9955267).
- [12] N. Zagni, A. Chini, G. Verzellesi, M. Cioni, G. Giorgino, M. Concetta, M. E. Castagna, and F. Iucolano, "Unveiling the role of hole barrier traps on ON-resistance instability after gate bias stress in p-GaN power HEMTs," in *Proc. IEEE Int. Integr. Rel. Workshop (IIRW)*, Oct. 2023, pp. 1–5.
- [13] N. Zagni, M. Cioni, A. Chini, F. Iucolano, F. M. Puglisi, P. Pavan, and G. Verzellesi, "Mechanisms underlying the bidirectional  $V_T$  shift after negative-bias temperature instability stress in carbon-doped fully recessed AlGaIn/GaN MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 5, pp. 2564–2567, May 2021, doi: [10.1109/TED.2021.3063664](https://doi.org/10.1109/TED.2021.3063664).
- [14] R. Vetry, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaIn/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001, doi: [10.1109/16.906451](https://doi.org/10.1109/16.906451).
- [15] *Sentaurus SDevice Manual (S-2021.06)*, Synopsys Inc., Sunnyvale, CA, USA, 2021.
- [16] N. Zagni, A. Chini, F. M. Puglisi, P. Pavan, and G. Verzellesi, "On the modeling of the donor/acceptor compensation ratio in carbon-doped GaN to univocally reproduce breakdown voltage and current collapse in lateral GaN power HEMTs," *Micromachines*, vol. 12, no. 6, p. 709, Jun. 2021, doi: [10.3390/mi12060709](https://doi.org/10.3390/mi12060709).
- [17] M. Cioni, N. Zagni, F. Iucolano, M. Moschetti, G. Verzellesi, and A. Chini, "Partial recovery of dynamic  $R_{ON}$  versus OFF-state stress voltage in p-GaN gate AlGaIn/GaN power HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 4862–4868, Oct. 2021, doi: [10.1109/TED.2021.3105075](https://doi.org/10.1109/TED.2021.3105075).
- [18] B. Bakeroot, S. Stoffels, N. Posthuma, D. Wellekens, and S. Decoutere, "Trading off between threshold voltage and subthreshold slope in AlGaIn/GaN HEMTs with a p-GaN gate," in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2019, pp. 419–422, doi: [10.1109/ISPSD.2019.8757629](https://doi.org/10.1109/ISPSD.2019.8757629).
- [19] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Brückner, M. Mikulla, G. Meneghesso, and E. Zanoni, "Deep-level characterization in GaN HEMTs—Part I: Advantages and limitations of drain current transient measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct. 2013, doi: [10.1109/TED.2013.2279021](https://doi.org/10.1109/TED.2013.2279021).
- [20] G. Verzellesi, A. Mazzanti, A. F. Basile, A. Boni, E. Zanoni, and C. Canali, "Experimental and numerical assessment of gate-lag phenomena in AlGaAs-GaAs heterostructure field-effect transistors (FETs)," *IEEE Trans. Electron Devices*, vol. 50, no. 8, pp. 1733–1740, Aug. 2003, doi: [10.1109/TED.2003.815134](https://doi.org/10.1109/TED.2003.815134).