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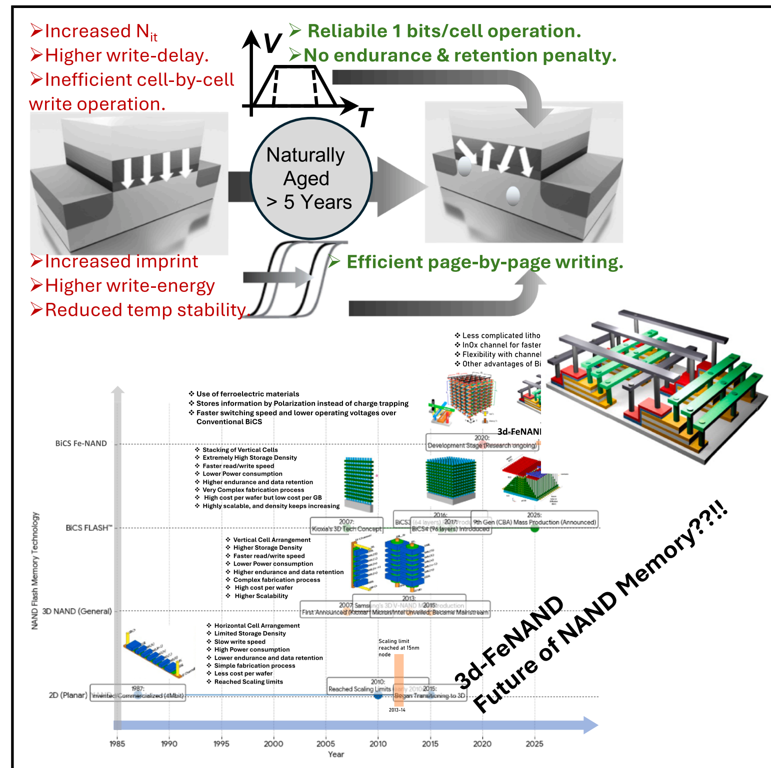
Long-term reliability of naturally aged hafnium oxide ferroelectric transistors for energy-efficient embedded memory

Graphical abstract



Highlights

- Naturally aged (>5 years) FeFETs retain clear switching and >1 V memory windows
- Donor-like interface and oxide traps govern endurance and memory-window loss
- Pulse shaping with slower ramps suppresses trap activation and extends cycling life
- Aged FeFETs show $>10^4$-cycle endurance at 85°C and decade-scale retention at 55°C

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In brief

Senapati et al. report the first long-term reliability study of FeFETs aged naturally for more than 5 years. They show that ferroelectric switching, endurance, and decade-scale retention remain robust, while pulse-engineered waveforms effectively suppress trap activation and enhance stability for embedded and storage-class memory applications.

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Long-term reliability of naturally aged hafnium oxide ferroelectric transistors for energy-efficient embedded memory

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SUMMARY

Ferroelectric field-effect transistors (FeFETs) based on hafnium oxide remain promising for embedded non-volatile memory, yet their long-term stability under realistic storage conditions is not well understood. Here, we examine silicon-doped hafnium oxide FeFETs that have undergone more than 5 years of natural aging in both ambient and cleanroom environments, without any electrical stress. The aged devices show a reduction in the memory window from 1.2 to 0.45 V after 10^4 program/erase cycles, consistent with the buildup of interface and oxide traps. Even so, they retain endurance above 10^4 cycles at 85°C and exhibit extrapolated retention exceeding 10 years at 55°C. Temperature-dependent charge-pumping measurements point to trap-assisted mechanisms as the dominant source of degradation, while waveform engineering with slower rise and fall times suppresses trap activation and stabilizes cycling behavior. These findings show that naturally aged FeFETs can meet key embedded-memory reliability targets and offer a practical route toward long-lived, energy-efficient memory technology.

INTRODUCTION

Hafnium oxide (HfO_2)-based ferroelectric field-effect transistors (FeFETs) have rapidly emerged as frontrunners in the race for next-generation non-volatile memory (NVM).[1–3] Their promise stems from a unique combination of attributes: sub-nanosecond polarization switching,[4] low-voltage operation, and seamless integration into advanced CMOS logic flows. These features collectively render FeFETs attractive for embedded memory,[5] storage-class memory, and in-memory computing,[6–8] offering a compelling alternative to conventional floating-gate flash, which is increasingly constrained by scaling and power inefficiencies. Beyond memory, FeFETs are also being explored as artificial synapses in neuromorphic accelerators,[9–12] where non-volatility, low-energy operation, and endurance are indispensable.[13–15]

Despite these advantages, the practical deployment of FeFET technology is hindered by unresolved questions of long-term reliability.[16,17] A central challenge lies in degradation induced by repeated program/erase (PG/ER) cycling. Cycling generates defect states at the semiconductor/oxide boundary,[18] manifested as interface traps (N_{it}),[19] and within the ferroelectric oxide itself, manifested as bulk oxide traps[20] (N_{ox}). These electrically active defects perturb the local electric field, accelerate depolarization, and ultimately narrow the memory window (MW), thereby reducing both endurance and retention.[21,22] Although a large body of work has examined such degradation in freshly fabricated FeFETs, typically relying on accelerated stress tests to extrapolate device lifetimes,[23] the effect of natural device aging over multi-year timescales has remained unexplored. This knowledge gap is particularly consequential, as commercial deployment requires devices that remain functional not only under immediate cycling but also after extended storage and field operation.

In this work, we present the first comprehensive reliability investigation of silicon-doped hafnium oxide (HSO)-based FeFETs that have undergone more than 5 years of natural aging. These devices, fabricated on 300-mm high-*k* metal-gate (HKMG) wafers using fully CMOS-compatible process flows, provide a unique experimental opportunity to examine the defect physics and endurance behavior of long-aged ferroelectrics. The samples were stored for over 5 years under stable room temperature (RT) conditions in a measurement laboratory, where temperature and humidity were continuously maintained at approximately

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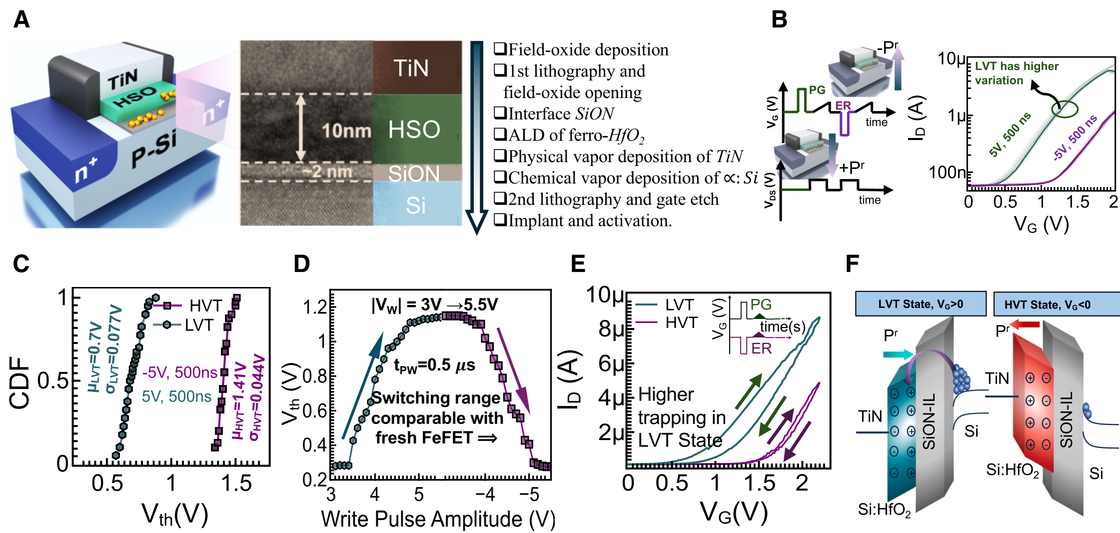


Figure 1. Electrical characteristics and switching behavior of naturally aged FeFET devices|

(A) 3D schematic of the HKMG $Hf_{0.5}Si_{0.5}O_2$-based FeFET with TEM cross-section and fabrication flow on 300-mm wafers.

(B) Left: schematic and pulse sequence illustrating PG/ER cycling and polarization switching under applied V_G and V_D. Right: I_D-V_G characteristics of aged FeFETs after 60 PG/ER cycles, confirming a robust memory window and reproducible switching. Enhanced variation is observed in the low-V_T (LVT) state, consistent with trap-assisted dynamics under favorable E_{app}-E_{FE} alignment.

(C) CDF of V_{th} from 40 FeFETs tested >5 years post-fabrication shows clearly separated LVT and high-V_T (HVT).

(D) The PG/ER response measured after 500-ns write pulses over a ±3→±5.5 V sweep shows switching behavior comparable to fresh FeFETs, confirming preserved ferroelectricity and functional operation. This result highlights the long-term stability of FeFETs and their suitability for embedded non-volatile memory platforms.

(E) Dual-sweep I_D-V_G characteristics post-PG/ER exhibit clear clockwise (CW) hysteresis, with the effect more pronounced in the LVT state due to increased electron trapping under favorable E_{app}-E_{FE} alignment.

(F) Schematic energy-band diagrams for HVT and LVT states, illustrating the alignment of applied field E_{app} and ferroelectric field E_{FE}.

20°C–25°C and 45%–55% relative humidity. Afterward, the devices were transferred internationally for subsequent electrical characterization in 2022. This multi-stage sequence—including controlled ambient preservation, transportation, and remeasurement in a separate laboratory—constitutes a realistic and rigorous aging protocol, closely mirroring the environmental variations typically encountered by commercial semiconductor products during long-term storage and field deployment.

Using variable base-voltage charge-pumping (CP) techniques,[24–26] applied across a wide temperature range,[13] we quantitatively extracted both the interface trap density (N_{it}) and oxide trap density (N_{ox}) before and after cycling, thereby isolating the relative contributions of aging-induced and stress-induced degradation. The analysis reveals that trap-assisted charge exchange governs the long-term degradation of these aged devices and that the progressive narrowing of the MW arises predominantly from the accumulation of donor-like traps near the interfacial region.

Beyond diagnosis, we demonstrate mitigation. A key outcome of this investigation is the identification of pulse-engineering strategies[27] that suppress trap activation. By extending the rise and fall times (t_r/t_f) of PG/ER waveforms while reducing the hold time (t_h), we significantly delay endurance failure and stabilize V_{th} evolution. This approach highlights that waveform design, traditionally viewed only as a means of ensuring functional switching, can in fact be leveraged as a powerful tool to extend reliability. Taken together, our findings advance the understanding of defect dynamics in naturally aged FeFETs and provide practical guidelines for robust operation. The demonstration that devices retain endurance beyond 10^4 cycles at 85°C and project retention lifetimes exceeding a decade at 55°C eintrinsicstablishes their industrial relevance. More broadly, these results confirm that even after extended natural aging, hafnia-based FeFETs remain credible candidates for embedded NVM, E-flash replacement, and unconventional computing platforms, where energy efficiency and long-term stability are paramount.

RESULTS

Electrical characteristics of naturally aged HSO-FeFETs

Figure 1A shows a 3D schematic of the HKMG-based HSO-FeFET along with the principal steps of the 300-mm fabrication process. The device stack features a 2-nm SiON interface and titanium nitride (TiN) electrodes, ensuring compatibility with standard CMOS flows while providing robust ferroelectric switching. The transmission electron microscopy (TEM) cross-section inset verifies uniform layer deposition and clean interfaces, both essential for stable long-term operation. Transfer curves recorded after 60 PG/ER events are presented in Figure 1B. The I_D-V_G characteristics exhibit reproducible, well-separated high-V_T (HVT) and low-V_T (LVT) states, with only minor drift relative to freshly fabricated counterparts. The inset depicts the PG/ER waveform used for stressing.

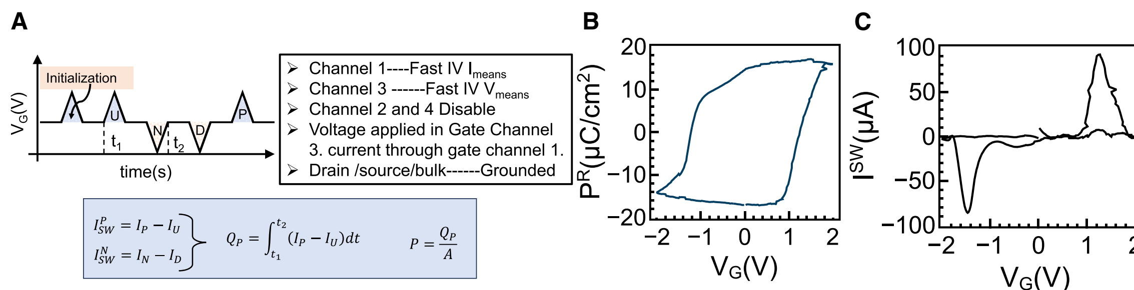


Figure 2. PUND measurements from FeFET's gate stack

(A) Measurement schematic and PUND pulse sequence for polarization extraction from aged FeFET's gate stack.

(B) Ferroelectric *P-V* hysteresis confirming polarization switching behavior of FeFET's gate stack after 5 years of aging.

(C) Corresponding I_{SW}-V_G characteristics showing stable hysteresis.

Uniformity across the device population is captured in Figure 1C, which plots the cumulative distribution of threshold voltages extracted from forty transistors. Despite more than 5 years of natural storage, the distributions remain distinctly separated, yielding an MW of ~0.7 V under ±5 V pulses. The absence of significant stochastic broadening or collapse demonstrates that polarization stability is well preserved at scale with minimal interface degradation. Figure 1D evaluates switching symmetry by mapping the threshold modulation against write-pulse amplitude at a 500-ns duration. The window evolves smoothly and symmetrically across both programming and erasing directions within the 3–5.5 V range, closely matching fresh-device behavior. This observation confirms that the intrinsic ferroelectric polarization of HSO films remains intact after extended ambient aging. This is further corroborated by positive-up-negative-down (PUND) measurements on the gate stack, as shown in Figure 2, which reveal stable ferroelectric hysteresis and switching current characteristics.

The dual-sweep transfer curves in Figure 1E highlight a pronounced clockwise hysteresis, particularly in the low-threshold state. This asymmetry reflects enhanced electron trapping when the applied field aligns constructively with the internal ferroelectric polarization, amplifying the local driving force for charge capture at the interface. The mechanistic picture is summarized in the schematic band diagrams of Figure 1F. Under favorable field alignment, traps are more easily activated, whereas under opposite alignment, the capture rate is suppressed. Collectively, these results demonstrate that even after >5 years of natural aging, HSO-FeFETs retain reproducible switching, a usable programming window, and interpretable trapping dynamics, all of which affirm their suitability for embedded NVM and in-memory computing.

Reliability under temperature and cycling stress

The thermal dependence of aged devices is summarized in Figure 3A. As the temperature increases from 25°C to 150°C, the MW contracts from ~1.12 to ~0.66 V, accompanied by threshold drifts in both states. These drifts are consistent with thermally enhanced trapping and redistribution of carriers. Importantly, the switching transitions remain clear and repeatable, underscoring that the fundamental ferroelectric response is preserved even at elevated temperatures. The gate-leakage characteristics shown in Figure 3B further confirm dielectric integrity: currents remain largely unchanged up to 65°C, with only slight increases thereafter, indicating that MW narrowing originates from defect processes rather than catastrophic leakage.

Cycling stress is examined in Figure 3C. With 5-V PG/ER bipolar pulse cycling repetition up to 10^4 events, the HVT states drift progressively positive, while the low-threshold state remains comparatively stable. This asymmetric evolution indicates bias-dependent donor-like trap generation, which primarily destabilizes the HVT condition and gradually narrows the window. Leakage traces recorded before and after 10^4 cycles (Figure 3D) remain nearly identical, excluding stress-induced breakdown of the dielectric stack. The endurance degradation is thus conclusively linked to trap dynamics rather than structural damage.

Figure 3E maps MW evolution under cycling at different temperatures. While RT cycling yields stable operation, higher temperatures (55°C–85°C) accelerate degradation, reflecting the combined influence of thermal activation and repeated polarization reversal on defect formation. Retention data at 55°C, shown in Figure 3F, demonstrate well-separated threshold states over extrapolated timescales exceeding 10^7 s, equivalent to >10 years of stable data storage. These results establish that aged FeFETs maintain industry-relevant endurance and retention characteristics even after prolonged ambient storage, validating their potential for embedded NVM and E-flash applications.

Trap dynamics revealed by variable-base CP

To investigate the microscopic origin of endurance degradation, variable-base-voltage CP techniques were employed. This configuration enables the probing of trap densities by applying controlled voltage pulses to the gate, allowing for the assessment of charge recombination currents that reveal trap locations and energies within the device stack, as depicted in Figure 4A. The extracted interface N_{it} from I_{CP} data collected at 1 MHz with 20-ns ramps demonstrates enhanced trap activation in the LVT state, attributed to favorable alignment between trapped charges and the ferroelectric polarization field, as shown in Figure 4B. This alignment facilitates charge capture and emission processes, contributing to shifts in threshold voltage and memory window narrowing over time. Figure 4C presents N_{it} as a function of V_B at increasing PG/ER cycle counts, ranging

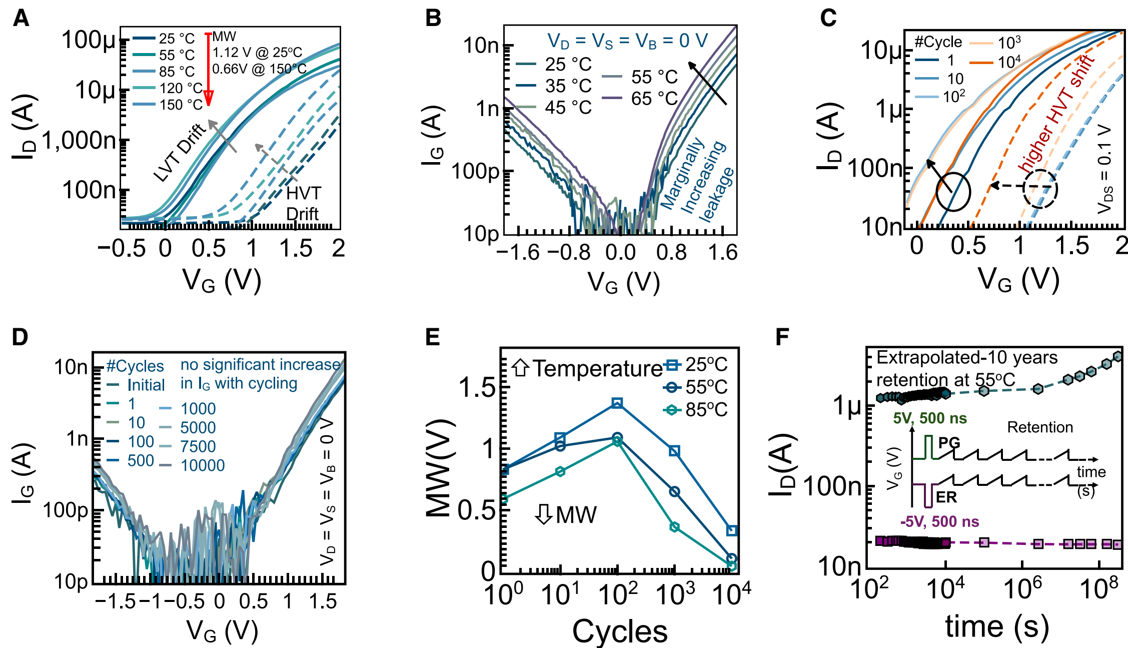


Figure 3. Reliability of naturally aged HKMG-FeFETs

(A) I_D-V_G at 25°C–150°C, showing systematic memory window (MW) reduction from ~1.12 (25°C) to ~0.66 (150°C) V.

(B) I_G-V_G versus temperature, confirming dielectric integrity over the measured range.

(C) I_D-V_G as a function of cycling (1→10^4), highlighting progressive high-V_T (HVT) shift and MW contraction.

(D) Gate leakage I_G before and after cycling (initial →10^4), showing no measurable increase, indicating damage-free PG/ER stress.

(E) Endurance degradation observed at elevated temperatures, where enhanced carrier trapping and defect-assisted charge redistribution accelerate V_T drift and narrow the MW under cycling, compared to RT operation.

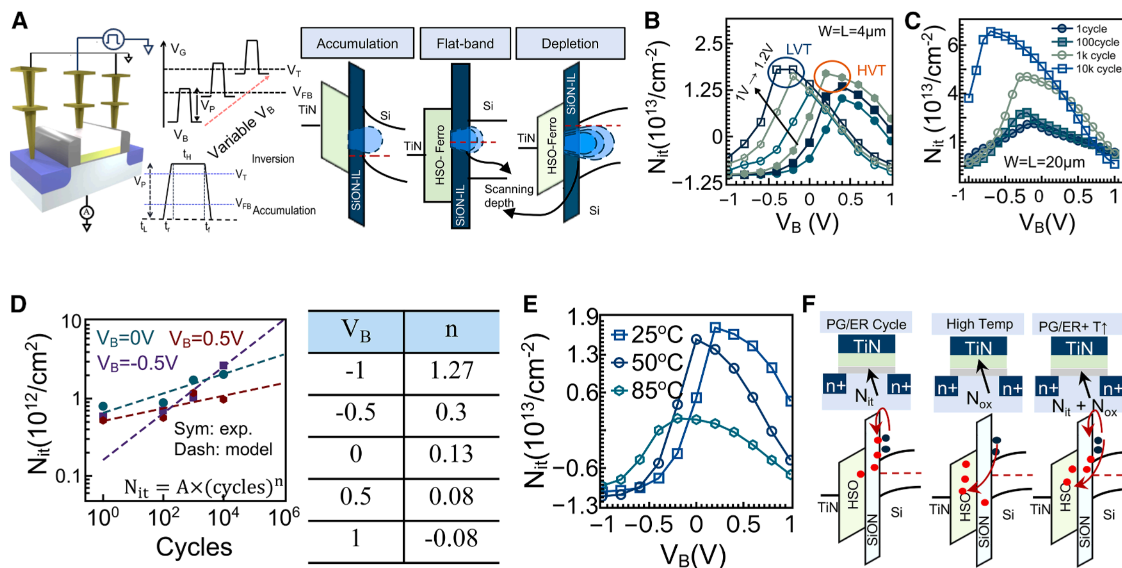
(F) Retention at 55°C shows well-separated low-V_T (LVT) and HVT states, with extrapolated lifetimes >10 years, confirming robust non-volatile data stability of aged FeFETs under moderate thermal stress.

from 1 to 10^4. The plot highlights a strong donor-like trap generation under negative biases, indicating that repeated cycling induces positively charged defects at the interface, which exacerbate depolarization and reduce device stability. Power-law modeling characterizes the evolution of N_{it} across endurance cycling under selected V_B conditions, as illustrated in Figure 4D. The inset extracts the trap-generation exponent η, revealing bias-dependent trap creation dynamics. Higher biases accelerate trap formation, following a sub-linear power-law relationship that underscores the role of electric field strength in defect proliferation. Temperature-dependent N_{it} profiles extracted via CP after wake-up cycling are examined in Figure 4E, across RT, 50°C, and 85°C. The systematic decrease in N_{it} with rising temperature is ascribed to the narrowing of electron/hole emission energy separation, which diminishes recombination currents during CP despite ongoing trap creation. This temperature sensitivity highlights thermal modulation as a factor in trap-assisted degradation. Schematic band diagrams in Figure 4F summarize the dominant mechanisms: (1) donor-like N_{it} formation during repeated PG/ER cycling, driven by field-induced defect generation; (2) thermally assisted N_{ox} activation, where elevated temperatures enhance bulk oxide trap mobility and interaction; and (3) cumulative trap evolution under combined cycling and thermal stress, simulating real-world operational conditions. These findings, derived from the CP techniques, elucidate how interface and oxide traps govern the reduction in memory window and endurance in aged FeFETs, offering pathways for mitigation through optimized pulse waveforms and operational parameters.

The kinetics of trap generation are modeled in Figure 5D, where power-law fitting reveals bias-dependent exponents. Negative base biases yield larger exponents, signaling accelerated donor-trap buildup, whereas positive biases suppress activation or lead to negligible defect formation. Thermal effects are captured in Figure 5E, where trap densities rise significantly with temperature from RT to 85°C, reflecting thermal activation of previously inactive sites. The mechanistic diagrams in Figure 5F consolidate these findings: electrical stress drives donor-like traps at the interface, thermal stress activates bulk oxide defects, and combined stresses amplify both pathways simultaneously. This comprehensive picture highlights the interplay of bias, cycling, and temperature in governing long-term FeFET reliability.

Pulse shaping as a strategy to suppress trap activation

Finally, Figure 5 demonstrates that waveform design provides a practical route to mitigating trap-induced degradation. Endurance data in Figure 5A reveal that slower rise/fall transitions yield substantially reduced MW narrowing compared to abrupt ramps, confirming that temporal shaping of PG/ER pulses



V_B	n
-1	1.27
-0.5	0.3
0	0.13
0.5	0.08
1	-0.08

Figure 4. Trap dynamics revealed by variable base-voltage charge pumping in aged FeFETs

(A) Experimental setup for variable-V_B charge-pumping (CP) measurements, with a Ginestra-inspired band diagram illustrating the depth of trap scanning accessible by CP.

(B) Extracted interface trap density (N_{it}) from I_{CP} data at 1 MHz (20-ns ramps), showing enhanced trap activation in the low-V_T (LVT) state due to favorable alignment between trapped charges and the ferroelectric polarization field (E_{FE}).

(C) N_{it} as a function of V_B at increasing program/erase (PG/ER) cycle counts (1–10^4), highlighting strong donor-like trap generation at negative biases.

(D) Power-law modeling of N_{it} evolution across endurance cycling under selected V_B conditions; inset shows the extracted trap-generation exponent n, evidencing bias-dependent trap creation dynamics.

(E) Temperature-dependent N_{it} profiles extracted by CP after wake cycling, showing a systematic decrease of N_{it} with increasing temperature (RT, 50°C, and 85°C). This reduction is attributed to the narrowing of electron/hole emission energy separation, which suppresses the recombination current during CP despite ongoing trap creation.

(F) Schematic band diagrams summarizing dominant mechanisms: (1) donor-like N_{it} formation during repeated PG/ER cycling, (2) thermally assisted N_{ox} activation, and (3) cumulative trap evolution when cycling and elevated temperature act simultaneously.

directly impacts trap formation. The deconvoluted trap density profiles in Figure 5B further show that fast ramps accelerate donor-like defect creation near the conduction band, while slower ramps strongly suppress activation. The energy-resolved distributions in Figure 5C emphasize this trend: extending t_r/t_f to ~2 μs effectively suppresses mid-gap donor traps (0.2–0.5 eV below E_C), the defects most detrimental to endurance.

In Figure 5D, the schematic illustrates how the temporal shape of the applied waveform governs trap activity during CP and endurance stress. As the channel is driven between accumulation and inversion, recombination occurs predominantly along the rising and falling edges, producing a substrate current directly proportional to the density of active defects. By sweeping the base voltage V_B, the technique selectively probes donor-like traps close to the conduction band edge as well as deeper states distributed across the ferroelectric and interfacial layers (ILs). The sensitivity of CP to t_r/t_f therefore enables not only the quantification of trap density but also an energy-resolved view of how aging and cycling activate different defect populations within the FeFET gate stack.

The physical interpretation is illustrated in Figure 5E. Rapid transients inject carriers efficiently but hinder detrapping, leading to cumulative trap buildup. Conversely, gradual ramps enhance recombination and detrapping, stabilizing the defect population and delaying degradation. These findings demonstrate that pulse shaping is not merely a functional adjustment for switching but a powerful reliability lever. By tailoring ramp profiles, it becomes possible to significantly extend device lifetime and maintain stable operation, even in FeFETs subjected to natural multi-year aging.

Taken together, these results establish a detailed reliability framework for naturally aged HSO-FeFETs. Clean switching characteristics, decade-scale retention, and endurance >10^4 cycles are retained even after prolonged storage, while advanced diagnostics reveal the trap mechanisms that govern eventual degradation. Importantly, pulse-engineering strategies emerge as a CMOS-compatible pathway to suppress defect generation and extend reliability. These insights not only confirm the technological readiness of hafnia-based FeFETs for embedded NVM but also point toward practical design knobs for improving long-term device stability in next-generation computing systems.

DISCUSSION

The results presented here establish that HSO-based FeFETs,[28,29] even after more than 5 years of natural ambient aging, continue to exhibit stable ferroelectric switching,

Table 1. Benchmarking of aged FeFETs against reported literature

Source	Type	Age	Gate stack	Initial MW	Retention loss	T_{ox} (nm)	V_w (V)	Endurance
This work	FeFET	>5 years	MFIS (HSO)	1.2 V	negligible until 10^4 s @ 55°C	9.0	±4.5	>2 × 10^4
IRDS (Hoefflinger[39])	FeFET	fresh	–	>1 V	<10% loss @ 10 years	10	<5	10^7
SK hynix (Yoon et al.,[41] Kuk et al.[42])	flash	fresh	MIFIS	10.5 V	–	19.5	16.6/–12	3 × 10^3
CAS (Kuk et al.[42])	flash	fresh	MIFIS	3.2 V	1.1 V (−66%) after 10 years projected	14	7.5/–4.5	10^4
Samsung (Lim et al.[43])	flash	fresh	MIFIS	5.5 V	1.1 V (−69%) after 1 year projected	27.7	16.5/–12.5	10^6
Samsung (Kuk et al.[42])	FeFET	fresh	MIFIS (IGZO)	5.7 V	–	12	17	–
GF 28 nm (Trentzsch et al.[44])	FeFET	fresh	HKMG	1.5 V	1 h @ 300°C and 7 days @ 250°C	8	±4.2	2 × 10^4
GF 22 nm (Dünkel et al.[45])	FeFET	fresh	FDSOI	1.5 V	similar to 28 nm	–	4.2	2 × 10^4

reproducible MWs, and robust thermal and cycling characteristics. Figure 2 shows stable ferroelectric polarization and a reliable switching current measured from the gate stack of the aged FeFETs via the conventional PUND method.[30] The observation of clear, symmetric polarization reversal across a wide programming range (Figure 1), coupled with retention lifetimes exceeding a decade at 55°C (Figure 3), confirms that ferroelectricity in hafnia-based systems is intrinsically durable. The electrical characteristics of freshly fabricated FeFETs using the same HSO/TiN gate stack and process flow have been documented previously.[31,32] These fresh devices demonstrated an MW of 1–1.4 V and endurance in the range of 10^4–10^5 cycles, consistent with the switching symmetry and polarization levels observed in our naturally aged samples. To further bridge the temporal gap between newly fabricated and long-term aged devices, FeFETs with an intermediate aging period of approximately 2 years were also evaluated, exhibiting similarly robust behavior.[33] These devices exhibited well-preserved transfer characteristics with average MW of ~1.5 V for SiON and ~1 V for SiO_2 interface stacks, along with stable endurance up to 10^4 cycles under a 6-V stress amplitude. The consistent electrical response across fresh, moderately aged, and 5-year-aged samples highlights the structural stability of the HSO ferroelectric layer and confirms that interface quality, rather than bulk ferroelectric degradation, governs long-term device reliability.

The strong agreement between fresh and aged devices confirms that ferroelectric polarization and memory functionality remain remarkably intact after extended ambient storage. Endurance degradation in aged devices is found to be governed not by leakage[34] or structural failure but by trap-assisted dynamics at the interface and within the oxide (Figure 3). The ability to diagnose these processes using variable-base CP and to mitigate them through waveform engineering[13,27] (Figure 5) underscores the importance of coupling physical insight with practical design strategies. The demonstration that simple pulse-shaping techniques can suppress donor-like trap activation and extend device lifetimes bridges the gap between fundamental defect physics and deployable circuit-level reliability. Collectively, these findings advance the case for FeFETs as credible alternatives to flash, meeting both the endurance and retention requirements of embedded and storage-class applications.[35,36]

When placed in the context of prior art, the performance of these aged FeFETs compares favorably with established and emerging NVM platforms. Benchmarking against reports from industry and academia (Table 1) highlights several distinctive strengths. Conventional flash technologies, while mature, require high voltages (>10 V) and exhibit limited cycling capability on the order of 10^3–10^4 cycles,[37] with significant projected retention loss over a decade. In contrast, the aged HSO-FeFETs studied here retain MWs above 1 V under ±4.5 V programming while sustaining endurance beyond 2 × 10^4 cycles and negligible retention loss up to 10^4 s at elevated temperatures. Compared with state-of-the-art FeFETs fabricated on advanced technology nodes (e.g., GlobalFoundries [GF] 22-nm and 28-nm platforms), which achieve endurance in the 10^6–10^7 range[16,38] but with fresh devices, the present results underscore the importance of demonstrating stability after extended storage. The fact that aged FeFETs still approach IRDS 2024 roadmap projections[39] for MW and retention provides confidence in their industrial viability. Moreover, the ability to achieve these metrics with a conventional HKMG process flow[40] strengthens the argument for seamless integration into advanced CMOS logic.[38]

Interestingly, under certain bias conditions, we observe negative values of the extracted N_{it}. This phenomenon should not be interpreted as a physical reduction of interface states but rather as an artifact of the CP technique when additional current components overlap with the recombination signal. These negative N_{it} values in aged FeFETs are diagnostic of competing leakage,[34] detrapping, and noise contributions rather than genuine annihilation of interface states. Recognizing and quantifying these artifacts is essential for a reliable interpretation of CP data, particularly under bias conditions where trap-assisted leakage strongly competes with interface recombination. Taken together, the comprehensive evaluation of electrical characteristics, trap dynamics, and benchmarking against both flash and FeFET baselines highlights a dual message: first, that natural aging does not fundamentally compromise ferroelectric switching, and second, that reliability bottlenecks[30,46,47] can be effectively managed through process-aware and circuit-level strategies. These insights provide a strong foundation for

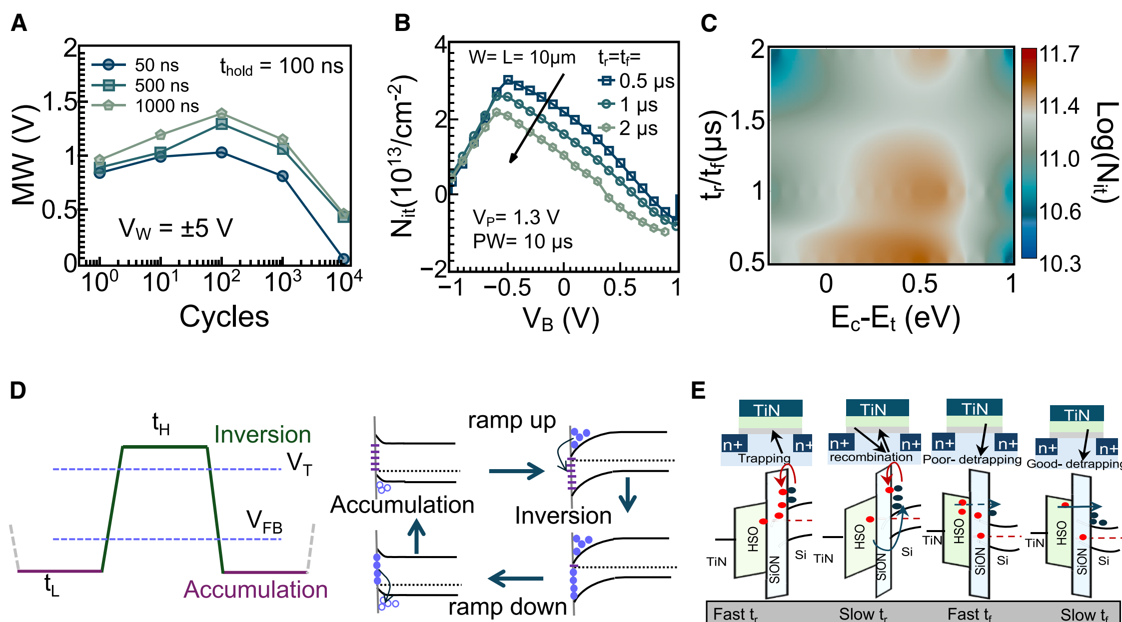


Figure 5. Pulse-shaping strategies to mitigate trap activation in aged FeFETs

(A) Endurance characteristics measured under different rise/fall times (t_r/t_f) at a fixed pulse amplitude (P_A) and hold time (t_h), showing enhanced endurance and reduced degradation with slower ramps.

(B) Deconvoluted N_{it} profiles across cycling, revealing progressive trap activation with increasing program/erase count.

(C) Energy-resolved N_{it} distributions as a function of t_r/t_f and trap depth, demonstrating that longer ramps (~2 μs) effectively suppress mid-gap donor-like traps (0.2–0.5 eV below E_C).

(D) Schematic illustration of the impact of t_r/t_f in CP and endurance experiments in FeFETs. A gate-pulse waveform toggles the channel between accumulation and inversion, while the base voltage is shifted to scan different trap depths. During the rising and falling edges, carriers recombine through interface and near-interfacial oxide states, producing a substrate current proportional to the active trap density. By varying V_B, CP selectively probes donor-like traps near the conduction band and deeper states within the ferroelectric/IL stack, enabling energy-resolved characterization of aging- and cycling-induced defects.

(E) Ginestra-inspired schematic band diagrams under distinct ramp conditions (not to scale), illustrating the physical basis of reduced trap generation with optimized pulse shaping.

positioning FeFETs as a long-term, energy-efficient memory solution spanning embedded NVM, E-flash replacement, and unconventional computing paradigms.[48]

This work provides the first comprehensive reliability assessment of HSO-based FeFETs that have undergone more than 5 years of natural aging. By examining devices fabricated on 300-mm HKMG wafers, we demonstrate that ferroelectric polarization and memory functionality remain remarkably intact after extended ambient storage. Electrical measurements reveal well-preserved switching characteristics, stable MWs, and reproducible device-to-device distributions, underscoring the intrinsic durability of hafnia ferroelectrics. Importantly, endurance degradation in these aged devices is traced not to catastrophic failure of the gate stack but to predictable trap-assisted processes at the interface and within the oxide. This mechanistic clarity provides a pathway to rational reliability engineering. The combination of variable-base CP and temperature-dependent characterization enabled quantitative separation of interface and bulk trap dynamics, revealing donor-like activation under bias stress and enhanced trap generation at elevated temperatures. Crucially, we establish that pulse-shaping strategies—specifically extending ramp times and reducing hold durations—can effectively suppress trap formation and delay endurance failure. This finding reframes waveform design from a purely functional perspective into a reliability lever, offering a practical, CMOS-compatible means of prolonging device lifetime.

From an application standpoint, the aged FeFETs investigated here deliver endurance exceeding 10^4 cycles at 85°C and projected retention lifetimes greater than a decade at 55°C. These metrics compare favorably with both conventional flash and contemporary FeFET implementations, aligning closely with IRDS 2024 roadmap targets for embedded NVM. The demonstration that devices retain functionality after multi-year storage is especially significant, bridging a critical gap between accelerated stress tests and realistic deployment scenarios. Figure 5 presents the schematic and optical image of a FeFET-based NAND string. The schematic in Figure 5A illustrates the page-wise organization of the FeFET NAND string, where each memory cell is connected in series between a source select line (SSL) and a ground select line (GSL). Control select lines (CSLs) and bitlines (BLs) define the read/write access paths, closely mimicking the hierarchy of commercial E-flash arrays but with ferroelectric transistors as storage elements. The accompanying optical micrograph in Figure 5B represents the intended layout scale for large-block integration (16–128 K cells per block), validating the design feasibility for embedded-memory modules.

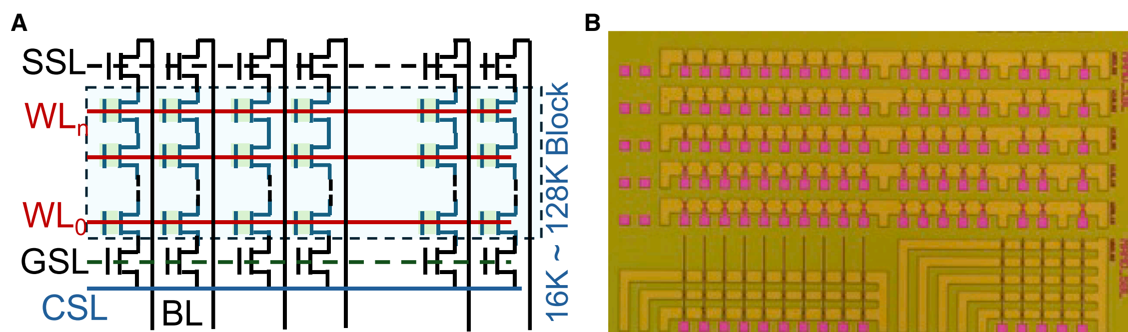


Figure 6. FeFET-based NAND string: Schematic and optical micrograph
The (A) schematic and (B) optical micrograph of an FeFET-based NAND string. Each memory string consists of FeFET devices connected in series between a source select line (SSL) and a ground select line (GSL). The control select line (CSL) and bitline (BL) enable access and read/write operations for individual pages.

Figure 6 illustrates the schematic and optical micrograph of a FeFET-based NAND string, highlighting its potential for large-block integration in embedded-memory modules. The device- and array-level parameters listed in Table 2 are derived from simulations with experimental FeFET data. The calculated results reveal a dramatic improvement in operation speed and energy efficiency compared to both newly fabricated FeFETs and conventional E-flash references. The aged FeFETs in this work demonstrate a superior page-wise PG/ER operation with a simulated write delay of only 0.128 ms and a read delay of 5.24 ms, significantly outperforming E-flash (3.2 ms write and 0.819 ms read). Most notably, the write energy (0.0472 μJ) is nearly three orders of magnitude lower than that of E-flash (160 μJ), highlighting the intrinsic advantage of direct polarization switching over charge-tunneling processes. The inclusion of the aged (≥5 years) FeFET parameters in the simulation underscores their stability and reliability under realistic long-term operation scenarios. Overall, these simulated results confirm that FeFET-based NAND architectures can achieve faster, low-energy page-level access while maintaining excellent endurance, positioning them as strong candidates for next-generation embedded NVM and E-flash replacement technologies.

METHODS

Device fabrication

FeFETs investigated in this study were fabricated on 300-mm bulk silicon wafers using CMOS-compatible, industry-standard process tools. The fabrication details were mentioned in our previous publications.[31,33] Each device features a 2-nm IL of SiON and a 10-nm HSO ferroelectric layer. TEM, as shown in Figure 1, confirms the precise thicknesses of both the interfacial and ferroelectric layers. The SiON interface was formed via rapid thermal annealing (RTA). The HfO_2 thin film was deposited using atomic layer deposition (ALD), a technique based on sequential, self-limiting surface reactions between precursor molecules and an oxidizing agent. In this work, $HfCl_4$ and $SiCl_4$ served as the precursors, with H_2O as the oxidant. The ALD process was conducted at 300°C, with a precursor cycling ratio of 16:1 for $HfCl_4$ to $SiCl_4$. The top electrodes—TiN and amorphous silicon—were deposited via physical vapor deposition (PVD) and chemical vapor deposition (CVD), respectively. Final crystallization and dopant activation were achieved through a single RTA step at 1,050°C for 5 s.[52] A detailed schematic of the fabrication process is provided in Figure 1.

Electrical characterization

Endurance cycling was performed by applying bipolar PG/ER pulses of ±5 V with a duration of 500 ns. I_D-V_G was measured in both states, and the V_{th} was extracted using the constant-current criterion[53] of I_D = 0.1 μA × W/L, with W and L being device width and length. The MW was defined as the difference in V_{th} between PG and ER states.[54,55] The PUND measurement setup used for extracting the polarization response of FeFET's gate stack is shown in Figure 3. For reliability analysis, we tracked the progressive narrowing of the MW and correlated it with trap-assisted degradation.[56,57] The measured drain current was further analyzed to decouple polarization-induced switching currents from trap-mediated leakage. In aged devices, particular attention was paid to the so-called first switch effect, where the initial write event induces significant trap generation at the IL due to unscreened polarization charges. That is a well-structured section detailing the use of CP in characterizing FeFETs, but the equation that relates I_{CP} to t_r and t_f is a simplified approximation and needs to be replaced with the full expression from the Groeseneken model to be accurate and complete. Here, we show the modified section, replacing the simplified equation with the correct, full kinetic expression and slightly refining the surrounding text for academic rigor.

CP analysis

CP was used to quantify the density of the interface traps N_{it} and the near-interfacial border traps N_{ox}.[58] In CP, a periodic gate pulse toggles the channel between accumulation and inversion while the source, drain, and substrate are held at ground or a small reverse bias. During each cycle, recombination of carriers at traps yields a measurable substrate current I_{CP},[59,60] from which the average total active trap density at the interface $\overline{N_{it}}$ (traps/cm^2) is obtained as

$$\overline{N_{it}} = \frac{I_{CP,max}}{qAf}, \quad \text{(Equation 1)}$$

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Table 2. Simulation-based performance benchmarking of FeFET and E-flash memory metrics

Metric	FeFET[31,49,50]	FeFET (this work)	E-flash[51]
Age	new	>5 year	>5 year
PG/ER scheme	cell-wise	by page	by page
Write delay	157.2 ms	0.128 ms	3.2 ms
Read delay	5.24 ms	5.24 ms	0.8192 ms
Write energy	7.078 μJ	0.0472 μJ	160 μJ

where q is the elementary charge, A is the gate area, and f is the pulse frequency.[61] This equation applies when the pulse amplitude is large enough to sweep the entire band gap.

To further resolve the energy distribution of the interface states, the variable-base CP method was applied, where the base voltage V_B was swept between −1 and +1 V. This allowed scanning across the band gap to differentiate N_{it} at the Si/SiON boundary from N_{ox} located deeper in the ferroelectric film. To accurately extract the interface trap density per unit energy D_{it} (traps/cm^2 eV), the current's dependence on the finite pulse transition times (t_r and t_f) must be modeled using the Shockley-Read-Hall (SRH) recombination dynamics.[62] The measured I_{CP} in this regime is related to D_{it} via the active energy window (ΔE) as defined in[63]

$$I_{CP} = qD_{it}fA \cdot \Delta E, \quad \text{(Equation 2)}$$

where the energy window ΔE is given by

$$\Delta E = kT \ln\left(\frac{\frac{|V_{G,high} - V_T|}{|V_{FB} - V_T|}t_r}{\tau_{e,0}}\right) + kT \ln\left(\frac{\frac{|V_{FB} - V_{G,low}|}{|V_{FB} - V_T|}t_f}{\tau_{h,0}}\right), \quad \text{(Equation 3)}$$

where V_T and V_{FB} are the threshold and flat-band voltages, $V_{G,high}$ and $V_{G,low}$ are the pulse levels, k is Boltzmann's constant, T is the absolute temperature, and $\tau_{e,0}$ and $\tau_{h,0}$ are characteristic emission time constants for electrons and holes (which contain the thermal velocity and capture cross-sections).

For polarization-charge quantification,[59] the CP signal was integrated over time:

$$Q = \int I(t)dt, P_r = \frac{Q}{A}, \quad \text{(Equation 4)}$$

which provides the remanent polarization P_r, confirming ferroelectric switching even under aged conditions. This CP-based approach has higher sensitivity than traditional P-V methods, allowing accurate measurement of switching charges in sub-micron devices and at short pulse durations (<50 ns).

The combination of endurance stress, I_D-V_G analysis, and CP measurements enabled us to disentangle the dual roles of cycling-induced and aging-induced defects. Importantly, the methodology also captured the dominant contribution of the "first switch" to interfacial degradation, establishing a direct correlation between switched polarization and trap density.

On the interpretation of negative N_{it} in CP

The N_{it} is extracted from the I_{CP} as in Equation 1, with q as the electronic charge, A as the gate area, and f as the pulse frequency.[13,63,64] In principle, I_{CP} is positive because SRH recombination at interface states[65,66] generates a substrate current during the rising and falling edges of the gate pulse.

In FeFETs, however, apparent negative values of N_{it} can occur under specific biasing conditions.[67,68] This does not imply annihilation of traps but instead reflects competing current components that superimpose on the recombination signal.

(1) Leakage currents. At large negative base voltages (V_B), band-to-band tunneling and gate-induced drain leakage (GIDL) can exceed the recombination current.[34,69] The effective signal becomes

$$I_{CP,eff} = I_{rec} - I_{leak}, \quad \text{(Equation 5)}$$

which yields $N_{it,eff} < 0$ when $I_{leak} > I_{rec}$.

(2) Detrapping currents. Pre-existing trapped charges may be emitted during the falling edge of the pulse,[21] adding a term.

$$I_{CP,eff} = I_{rec} - I_{detrap}. \quad \text{(Equation 6)}$$

This effect is enhanced when the applied field E_{app} aligns with the ferroelectric polarization field E_{FE}, which favors electron emission.

(3) Weak excitation regime. For low pulse amplitudes or slow ramps, I_{rec} is small and comparable to displacement or noise currents[70]:

$$I_{CP,eff} \approx I_{rec} \pm I_{noise}. \quad \text{(Equation 7)}$$

In this limit, statistical fluctuations can again yield apparent negative densities.

Thus, negative N_{it} values in CP analysis are artifacts arising from leakage, detrapping, or noise competition. Their occurrence serves as a diagnostic indicator of parasitic pathways rather than a physical reduction of interface states, and careful biasing is required to avoid misinterpretation.

Retention lifetime extrapolation

Retention projections were estimated using the Arrhenius thermal-acceleration model, an industry-standard approach for predicting data retention from high-temperature stress tests. The degradation rate is assumed to follow an exponential temperature dependence, $\tau(T_{use}) = \tau(T_s) \exp\left[\frac{E_a}{k_B}\left(\frac{1}{T_{use}} - \frac{1}{T_s}\right)\right]$, where E_a is the activation energy. A conservative E_a = 0.7 eV, consistent with charge loss and depolarization in HfO_2-based FeFETs, was used. While more complex multiphysics models may capture additional degradation mechanisms, such as cycling-induced stress or humidity effects, such analysis is beyond the present scope. The Arrhenius method nevertheless provides a reliable first-order estimate of decade-scale retention at 55°C.

RESOURCE AVAILABILITY

Lead contact

Requests for further information and resources should be directed to and will be fulfilled by the lead contact, Sourav De (sourav.de@mx.nthu.edu.tw).

Materials availability

This study did not generate new unique reagents or materials.

Data and code availability

- All data reported in this paper will be shared by the lead contact upon request.
- This paper does not report original code.
- Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

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AUTHOR CONTRIBUTIONS

A.S. and A.D. contributed equally to this work. A.S., A.D., and S.D. prepared the first draft of the manuscript and performed subsequent modifications. A.D. and M.R.S. carried out the experimental investigations. G.K. and S.D. generated and refined the figures and plots. Y.R., R.O., and P.S. contributed to data curation, verification, and critical revision of the draft. B.C., S.M., A. Padovani, and S.D. provided supervision, leadership, and strategic guidance while also contributing to manuscript modifications. S.D. was responsible for funding acquisition.

DECLARATION OF INTERESTS

The authors declare no competing interests.

DECLARATION OF GENERATIVE AI AND AI-ASSISTED TECHNOLOGIES IN THE WRITING PROCESS

We acknowledge using Grammarly and ChatGPT AI to refine the language throughout our manuscript. However, no image, data, or scientific/technical content has been generated using any AI tools. The usage of AI has been strictly limited to language refinement purposes.

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