Analysis of Voltage Distribution and Connections within a High-Frequency Hairpin Winding Model

Marco Pastura, Stefano Nuzzo, Davide Barater, Giovanni Franceschini

***Abstract* – In the last years the adoption of hairpin windings is increasing, especially in the automotive sector, mainly due to their inherently high fill factor and electric loading capability.**

A critical aspect related to the reliability and lifetime of every winding typology is the voltage stress due to the uneven voltage distribution. This phenomenon has already been largely analyzed in conventional stranded conductors, while a few studies are available for hairpin windings. With the spreading of wide bandgap devices, the investigation on voltage distribution becomes an ever-timely topic due to their short rise times. This paper presents an analysis of the uneven voltage distribution triggered within hairpin windings by a low rise time waveform, using a complete high-frequency winding model. The different options to series-connect different paths are investigated, providing simple but essential guidelines to reduce the electrical stress within hairpin windings.

***Index Terms*— Voltage distribution, Insulation stress, Hairpin Conductors, Hairpin connections, Wide-Band-Gap devices, Electric drives**

I. INTRODUCTION

A. Background

Nowadays the importance and diffusion of Variable Speed Drives (VSDs) is well known. With the expansion of electrification, VSDs have reached an enormous variety of applications, from household to industrial, aerospace, automotive or renewable energy generation appliances. VSDs normally require converters with switching semiconductors. In order to increase the overall performance, the research and adoption of Wide Bandgap (WBG) devices is spreading [1]-[4]. In fact, thanks to their fast commutations, higher switching frequencies and lower losses can be achieved. On the other hand, the considerably low rise times of WBG devices tend to increase electrical insulation stress due to voltage wave reflection and uneven voltage distribution within machine windings [4]. Overvoltage due to wave reflection is less prominent where sufficiently short connections between converter and machines are adopted, while the uneven voltage distribution is always present when short rise times occur. This phenomenon has already been largely studied in stranded round conductors [5]-[9], while few data are available for hairpin conductors, which are becoming quite popular, especially for automotive applications.

B. Hairpin Conductors

Hairpin conductors are pre-formed wires which can achieve a high fill factor, thus also a higher slot thermal conductivity [10]-[15]. This aspect allows to increase the electric loading, especially at low frequencies, making them suitable for automotive applications requiring high torque densities. Hairpin conductors are suitable also for large scale productions and allow the realization of identical coils, which is another important requirement to meet in the automotive sector.

Beyond all these advantages, hairpin conductors present also some challenges. They are quite sensitive to AC Joule losses, which are not evenly distributed in the different layers, i.e. they tend to increase from the slot bottom towards the air gap. Hence, transpositions are necessary in order to equalize the impedances of the different winding paths, such that the internal recirculation of currents is avoided [11],[12]. This necessity results in a lower number of degrees of freedom in terms of winding topologies compared to designing windings with round, stranded conductors. Apart from transposition, which is mandatory, some solutions have been studied to decrease the impact of AC losses, such as the adoption of hairpin conductors with variable cross sections inside the slot [13], the increase of the number of layers [12], pushing conductors towards the slot bottom or the adoption of different materials [14].

While extensive attention is given to AC losses in the available literature, little focus is given to the reliability aspects related to hairpin windings and their insulation system. In particular, few data and models are available on hairpin windings' voltage stress.

C. State of the art of hairpin windings voltage distribution

As stated in the previous section, hairpin conductors allow the realization of identical coils.

In fact, the exact location of each conductor is known, thus more reliable results in terms of voltage stress modeling can be achieved and appropriate countermeasures can be taken, such as the choice of a specific insulation or a proper winding layout. Some studies have been done in order to reach a better understanding of these phenomena in hairpin windings [16]-[19]. The general approach is typically based on the finite element (FE) extraction of the impedances, and on the simulation of the voltage waveforms in the equivalent high frequency (HF) circuit of the winding (or a portion of

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it). A particular focus has been given to the influence of the voltage input parameters (amplitude, rise time or *dv/dt*), through some sensitivity analyses [16], [17], and to some possible special connections aimed at reducing the maximum voltage amplitude between adjacent layers [16], [19]. However, more investigations are needed, such as:

1. the influence of winding geometric parameters;
2. the study of the phenomenon in short pitched windings;
3. the study on how to reduce the voltage stress for machines featuring standard and simpler connections, which are more likely to be adopted in a context of large scale and/or lower cost production.

This paper is focused on the third point, whereas the first two aspects will be investigated in future researches.

D. Motivation and Aim

Considering the above, the main aims of this paper are to present a voltage distribution analysis on a complete HF model of a three-phase winding with standard connections, and to investigate the best possible solutions to series connect the different winding paths. The considered machine connections are kept as uniform as possible in order to simplify the realization of the winding, thus no jumps of more than one layer are considered. The main motivation under this assumption is that special connections are not always feasible and they tend to increase the manufacturing complexity, thus some simpler and lower cost alternatives should be also investigated. The main results are then adopted to draw some simple but important guidelines for the realization of hairpin windings with a reduced voltage stress.

II. Model Description

A. Case Study

The considered machine is a dual three-phase PM-assisted synchronous reluctance machine with six conductors per slot and integer slot distributed winding ISDW. Each phase consists of 4 paths whose terminals can be series or parallel connected. The winding main data are summarized in TABLE I. For the sake of the voltage distribution study, only one of the two three-phase windings can be considered and the rotor influence can be neglected.

B. Finite Element Model

A 2D FE model is built for the extraction of all the winding impedances, thus a proper mesh and characterization of all the materials is needed. A picture of it can be observed in Fig.. The adopted software is Simcenter ElecNet for the capacitances determination and Simcenter MagNet for resistances and inductances. The evaluation of the parameters, which is briefly recalled below, is carried out as illustrated in [16]-[19]:

- The capacitances are computed though electrostatic simulations, since they are frequency independent.
- The resistances and inductances can be computed through transient or time harmonic simulations. In this paper, transient simulations are performed to achieve a better accuracy. The saturation is considered low, which should correspond to the worst case scenario in terms of voltage stress. In fact, the consequently higher inductance should trigger voltage oscillations also at lower frequencies.
- The frequency dependent parameters are evaluated at a fixed frequency f_r, which is chosen according to the input waveform rise time t_r [9].

C. Circuital Model

The HF equivalent circuit consists of series and parallel connections of multiple *RLC* impedances. Fig.2 provides an example of the HF model of a 2-layer slot. R_i and L_i are basically the HF resistances and inductances of the conductor belonging to the i^{th} layer. C_{12} is the capacitance between the two considered adjacent layers, while C_{i0} are the conductor to ground capacitances.

The slot walls are considered at the ground potential. The single slot models are identical for a specific machine and should then be connected, according to the number of slots, paths and conductor transposition, in order to realize the HF total impedance of each phase.

D. Winding Connections

Before running the simulations, it is necessary to connect the slot winding models according to the winding diagram. This section illustrates the adopted connections for the

TABLE I. WINDING PARAMETERS

Winding topology	ISDW
Slots	96
Slots per pole per phase	2
Slot Conductors	6
Conductor dimensions [mm]	2.8 x 1.8
Phase Paths	4

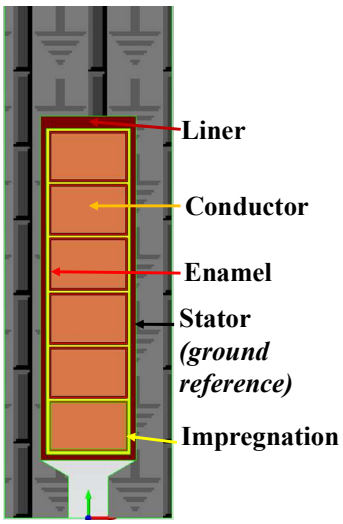

Fig.1. 2D FE model of one slot. The main components are highlighted.

realization of each phase path. Fig. 3 shows the winding diagram of one phase. There are four paths:

- Paths 1 (red) and 2 (green) start form the 1st layer of slots 1 and 2 respectively, while they end in the 6th layer of slots 86 and 85 respectively. They are wounded clockwise.
- Paths 3 (yellow) and 4 (blue) start from the 6th layer of slots 1 and 2 respectively, while they end in the 1st layer of slot 14 and 13 respectively. They are wounded counterclockwise.
- Each path has the same identical connection topology. There are one short and one long connection at each revolution in order to equally fill all the slots per pole per phase. The connections with the dotted lines, which refer to the welding side, are such that the coil pitch is equal the pole pitch. The solid lines are referred to the insertion side and can have different lengths when it is necessary to change slot per pole from even to uneven indexes or vice versa. However, they are kept as uniform as possible. Hence, only jumps of a single layer have been adopted. Each connection is characterized by a change of layer, and for each revolution two layers are filled. The starting slots have been chosen such that the terminals are kept near to each other.

To summarize, all the paths start from slots 1 and 2. The clockwise paths start from the 1st layer, while the counterclockwise paths from the 6th. Depending on how the starting (SP_i) and ending (EP_i) terminals are connected, different phase layouts can be achieved. It has to be considered that the connection topology of each path and the terminal connection must be identical for every phase. This results in the winding diagram of the other phases being equal to that of Fig. 3, with the exception of a different slot index, which can be obtained shifting the actual slot index with the correct phase shift.

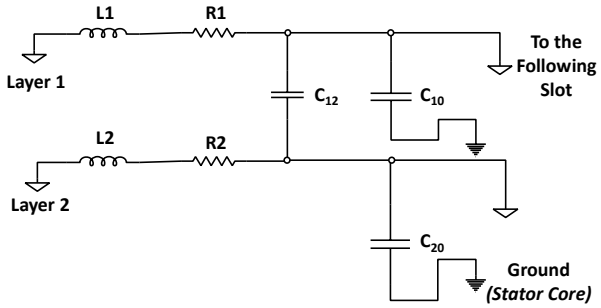

Fig.2. HF slot model of a 2-layer winding.

III. Voltage Distribution Analysis

A. Preliminary considerations

As stated in section I. D. the main aim is to investigate the different series connections which can be obtained from the connection of the paths' terminals. To achieve that, path 1 is kept fixed as the starting one, while the connection order of all the other paths is varied. The simulated transition considers a SV-PWM inverter going from a zero state to an active state, thus the HF total impedance will consist in the series connection of one phase with the parallel of the remaining two (all the phases are modelled). The single phase will be the most stressed, since it will experience a total voltage drop of $\approx 2/3 V_{dc}$ (if no considerable overshoot occurs), where V_{dc} is the DC bus voltage. This analysis will consider the aforementioned transition when the phase shown in Fig. 3 (A1) is the series connected one, as schematized in Fig. 4. The simulations are run with a square wave voltage input of 500V and a rise time of ≈33ns, corresponding to a frequency of ≈10MHz used for the estimation of the HF impedances in the FE-based software.

B. Simulations

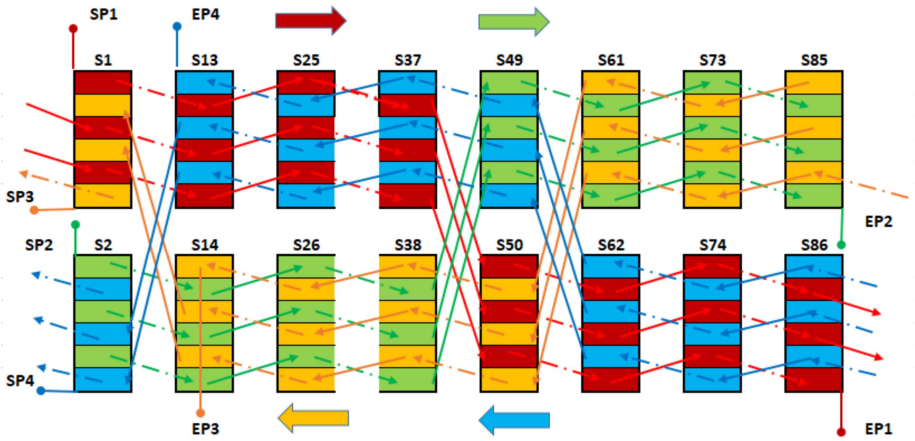

Fig.3. Winding diagram of one phase, including all the paths. The even index slots are on the top, while the others on the bottom. Slots belonging to the same pole are on the same column.

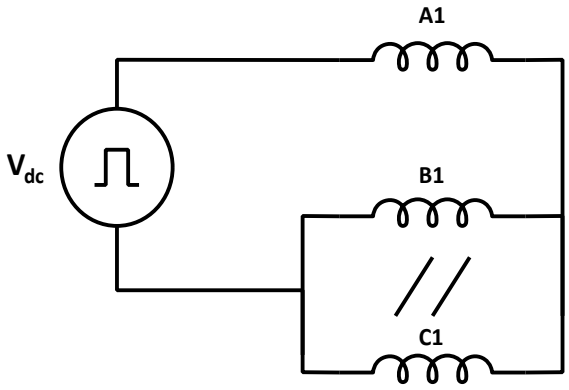

Fig.4. Simulated transition. A1 is the analyzed phase

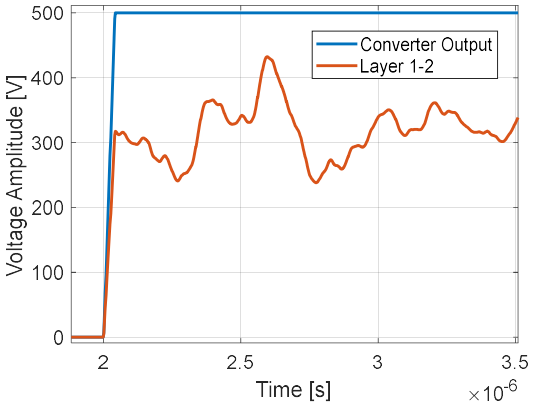

Fig.5. Example of voltage waveform between the first two layers of a slot.

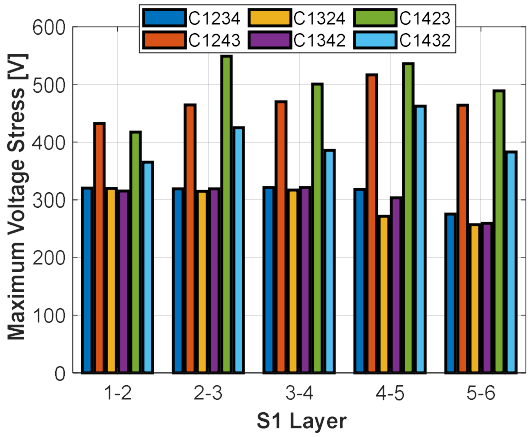

Fig.6. Slot 1 maximum voltage stress as a function of layer.

The most representative slots to analyze are those where the start and end terminals of the four paths are located. These slots are the 1st, 2nd, 13th, 14th, 85th and 86th. Once a simulation is run, it is possible to extrapolate the voltage waveforms between adjacent layers belonging to each slots. Fig. 5 provides an example of the voltage between two layers. The most relevant value during each transition is the peak voltage which corresponds to the maximum voltage stress between the adjacent layers. Therefore, this value is selected for plotting Figures 6-11. This will provide an

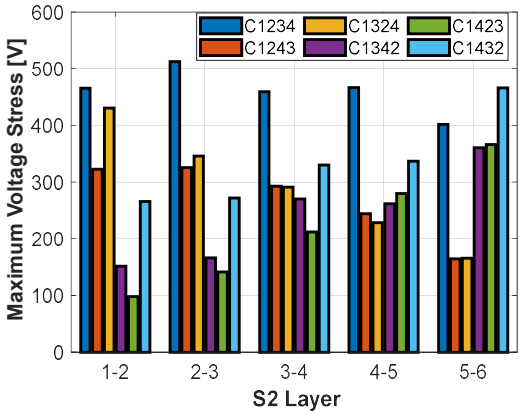

Fig.7. Slot 2 maximum voltage stress as a function of layer.

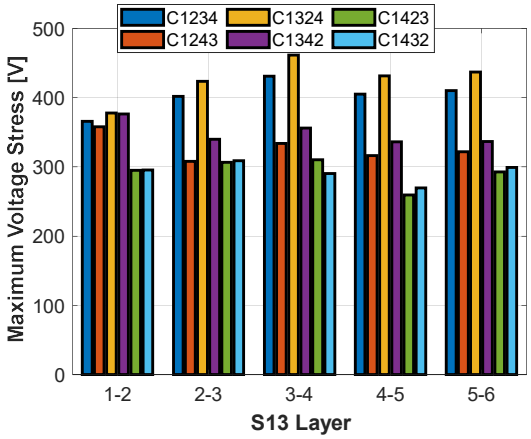

Fig.8. Slot 13 maximum voltage stress as a function of layer.

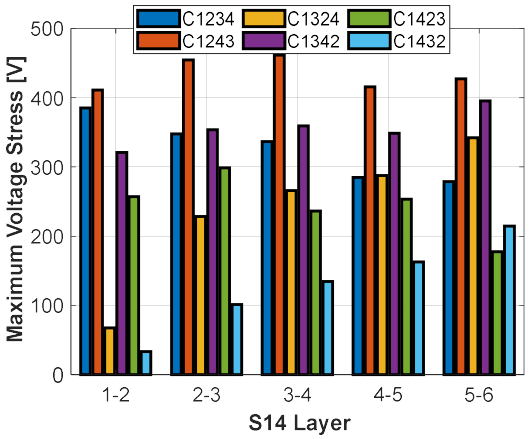

Fig.9. Slot 14 maximum voltage stress as a function of layer.

indication of the best connection paths' configurations C1xxx, where the indexes "1xxx" represent the path series connection order. Each figure from Fig. 6 to Fig. 11 illustrates the layer-to-layer peak voltage, during a switching transient, for each adjacent layers in a representative slot (S_i), and for all the analyzed C_{1xxx} configurations. Fig. 12 shows a summary of the highest values of the maximum voltage stress occurring in each slot for each configuration, regardless of the layer where it occurs. This figure can provide a compact indication of the best configurations. From Fig. 12 it can be observed that there are two optimal

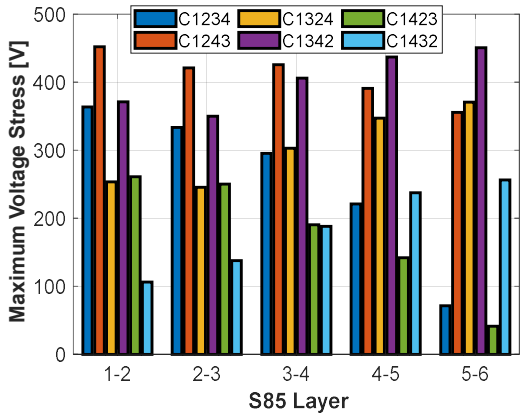

Fig.10. Slot 85 maximum voltage stress as a function of layer.

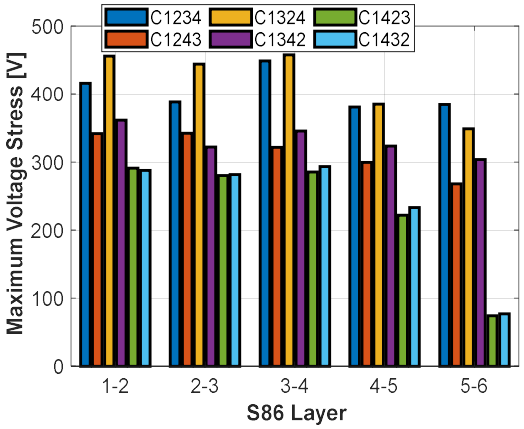

Fig.11. Slot 86 maximum voltage stress as a function of layer.

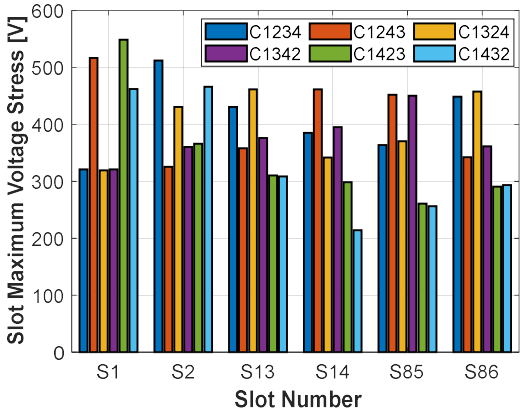

Fig.12. Maximum value of slot peak voltage stress for all the configurations.

configurations, i.e. C1342 (purple) and C1432 (light blue). They both always achieve a slot maximum voltage stress around 450V in two of the considered slots, i.e. S85 for C1342 and S1 for C1432. When the objective was to reduce only the highest value of the peak voltage stress, the path 1-3-4-2 would be the best one, as it can achieve a slightly lower value than the path 1-4-3-2. However, this second configuration can also provide a considerably lower average value of the peak voltage stress (in addition to a comparable maximum value), which is obtained in only two slots. In fact, C1432 has voltage stress values always below 300V for S14, S85 and S86, and a maximum value around 300V for S13, which make it the most interesting choice. On the other hand, C1342 features values always above 300V, for every layer of all of the slots.

A common characteristic of both configurations is that they have path 2 at the end of the series connection. It has to be noticed that the ending path has the same starting layer and wiring direction of the starting path, with which there are no slots in common. The other two paths, wounded in the opposite direction (counterclockwise), occupy the middle positions of the series connection. Therefore, some simple general rules can be derived as follow.

- Starting and ending paths should not share the same slots. In fact, paths which are far in the series connection exhibit a higher voltage difference, but the electrical stress between them cannot occur when there are no common slots.
- When the aim is also to contain the average peak voltage stress, the second path (in the connection order) should be the one which shares the highest number of slots with the starting path. Paths with many slots in common should always be kept as near as possible in the series connection, in order to reduce the voltage difference between them.
- When the winding is an ISDW with the same connection rules illustrated in section II.D, the series connections which satisfy the previous two points belong to one of these two categories: CW-CCW-CCW-CW or CCW-CW-CW-CCW, where CW stands for clockwise and CCW stands for counterclockwise. In order to minimize also the average peak voltage stress, the consecutive paths should start in different slots (this second rule is not satisfied by C1342).

Failing to meet these simple rules could result in voltage stresses, potentially exceeding the DC bus voltage amplitude.

IV. Conclusion

In this work the uneven voltage distribution and the ensuing voltage stress, triggered by a low rise time waveform feeding hairpin windings, was investigated. The winding diagram of the adopted ISDW model was first described, and several ways to series connect the various paths of one machine phase were then illustrated. The winding connections were kept as uniform as possible since it is not always possible to adopt a consistent number of special connections. The voltage stresses between the winding layers were analyzed through the equivalent HF circuital model for all the possible configurations. Some basic rules to reduce both the maximum and the average of the peak voltage stresses between the layers were underlined. The main conclusion relates to a simple guideline consisting of keeping distant the paths with no slots in common, while paths with several slots in common should be kept as near as possible in the series connection.

V. ACKNOWLEDGMENT

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VII. BIOGRAPHIES

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