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Effect of Semiconductor Parasitic Capacitances on Ground Leakage Current in Three-Phase Current Source Inverters

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Abstract: This paper investigates the influence of power semiconductor parasitic components on the ground leakage current in the three-phase Current Source Inverter topology, in the literature called H7 or CSI7. This topology allows reducing converter conduction losses with respect to the classic CSI, but at the same time makes the topology more susceptible to the parasitic capacitances of the semiconductors devices. In the present work, a grid-connected converter for photovoltaic power systems is considered as a case study, to investigate the equivalent circuit for ground leakage current. The same analysis can be extended to applications regarding electric drives, since the HF model of electric machines is characterized by stray capacitance between windings and the stator slots/motor frame. Simulation results proved the correctness of the proposed simplified common-mode circuit and highlighted the need of an additional common-mode inductor filter in case of resonance frequencies of the common-mode circuit close to harmonics of the power converter switching frequency. Experimental results are in agreement with the theoretical analysis.

Keywords: current source inverter; photovoltaic; parasitic capacitance; common mode; ground leakage current

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1. Introduction

The exploitation of photovoltaic energy has been a key topic of industrial and academic research in the past decade. The need for a DC/AC conversion for the grid interface has spurred the researchers to investigate the subject from multiple points of view: energy source, power electronics, controls, etc. Nowadays, plants ranging from hundreds of Watts to MW are installed. In this framework, the research for optimized power electronics for small-scale photovoltaic installation has been particularly active [1].

The most widely adopted topology for the DC/AC converters for photovoltaic system is the voltage source inverter (VSI), due to the good efficiency, low component count and the ease of control. However, the presence of electrolytic capacitors which limit the lifetime, the absence of boost capability and short-circuit resilience, has pushed the investigators to study different topologies, including the impedance source converters and the Current Source Inverters (CSI) [2].

The CSI7 converter was first shown in [3]. The basic structure is made of seven reverse-blocking switches in a three-phase configuration. A preliminary analysis of the power devices parasitic capacitances effects was reported in [4]. Follow-up studies were carried out in [5,6], while [7] proposes a new 5-Level CSI topology.

For variable-speed drive application, the CSI has been adopted [8,9] in a back-to-back configuration, where a current source rectifier regulates the input current of a current source inverter driving an induction machine. For PMSM application, the CSI with front-end and LC filter was presented in [10], and a novel control that allows operating without

front-end was proposed in [11]. It is important to highlight that the new semiconductor technologies [12] and the advanced electrical machine design strategies [13] increased the applicability of the CSI topologies for some specific applications, for example high-speed high-power density machines for the more electric aircraft [14,15]. Other researchers expanded the CSI research for electric drives analyzing the four-leg [16] operations, the zero voltage switching [17], hybrid PWM strategies [18] or the low switching frequency operations [19].

In a space vector modulation paradigm, there are nine possible vectors (six active and three zero vectors [20]). During the active vector, the output current in the selected phases is equal to the dc inductor current, whereas during the zero vector, the inductor current is free-wheeling within the power electronics. With the CSI7 topology, it is possible to generate the zero vector with only the additional device S_7, disconnecting the dc side from the ac one, with great benefits in terms of ground leakage current [21] and conduction power losses. At the same time, this disconnection makes this topology susceptible to semiconductor parasitic capacitances.

Section 2 describes the CSI7 (H7) topology also taking into account the parasitic elements. Sections 3 and 4 report the numerical simulations and the experimental results supporting the theoretical analysis. The conclusion closes the paper.

2. Considerations on Parasitic Components

A thorough description and comparison of CSI and CSI7 topologies about output current distortion and semiconductors power losses for transformerless grid-connected converters can be found in [21].

This work has highlighted that the Alternated Space Vector Modulation (see [5]) and the use of split DC input inductors allows obtaining significantly better performance.

In this work, the effect of the parasitic capacitances of the power transistors and diodes is analyzed in terms of ground leakage current. In particular only the output capacitance C_{oss} of the power transistors and the diode junction capacitance C_j was considered.

Figures 1 and 2 show the schematic of a CSI7 topology with and without the aforementioned parasitic capacitances.

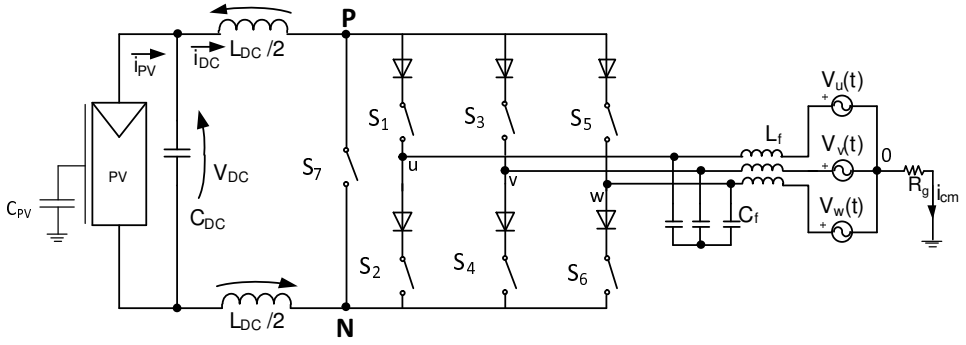

Figure 1. Schematic of CSI7 topology.

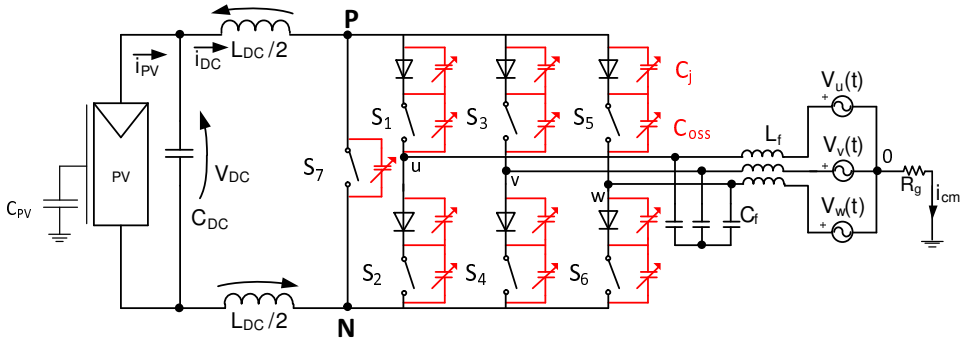

Figure 2. CSI7 topology with parasitic capacitors.

Photovoltaic plants are particularly prone to ground leakage current issues, since the PV modules exhibit a large stray capacitance C_{PV} with respect to grounded metallic structures that are part of the installation. The analysis and the equivalent CM circuit of the converter developed in the present work can be usefully extended to electric drives as well, since the DC source that replaces the PV modules is fitted with C_Y capacitors to ground for EMI suppression and the HF model of electric machines is also characterized by stray capacitance between the machine windings and the stator slots/motor frame, [22,23].

The value of the power semiconductor's parasitic capacitance is not constant, but decreases when the Drain-Source voltage and Diode Reverse Voltage increases. The analysis was carried out considering SiC MOSFETs (C2M0025120D) and Diode (FFSH50120A). Figure 3 shows the parasitic capacitances evolution voltage depending.

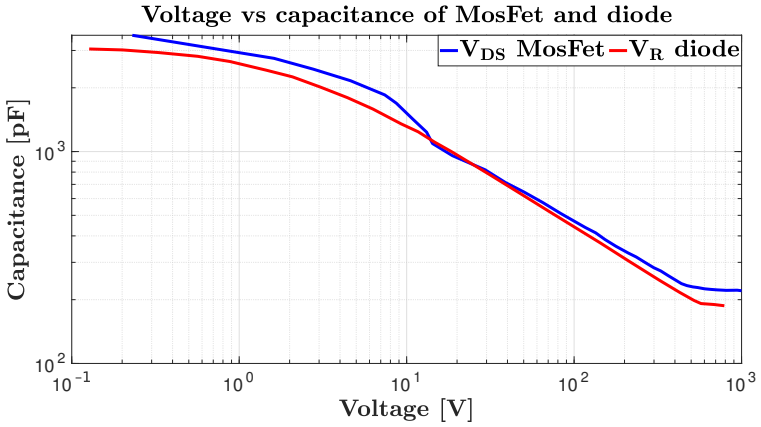

Figure 3. C_{oss} and C_j variations for SiC MOSFETs (C2M0025120D) and Diode (FFSH50120A).

To allow fast simulations, constant values of C_{oss} and C_j could be taken into consideration, namely C_{oss_Fix} and C_{j_Fix}. This assumption allows simplifying the analysis of the ground leakage current and will be validated by means of numerical simulations in Section 3. The choice of the fixed values is not an easy task. In the simulation section the minimum capacitance values were chosen, i.e., the capacitance value when the maximum voltage applied by the grid is present across them.

Since one of the goals of this work is to propose an equivalent common-mode circuit which integrates the semiconductor parasitic capacitances, it is important to focus on the power converter configuration during Zero Vector application. In fact, in this condition there is no connection between the DC link and the grid in the case of ideal switches.

Figure 4 shows the simplified configuration during Zero Vector application (S_7 ON and S_1–S_6 OFF). During the application of any Active vectors the effect of the parasitic capacitances is null in terms of ground leakage current.

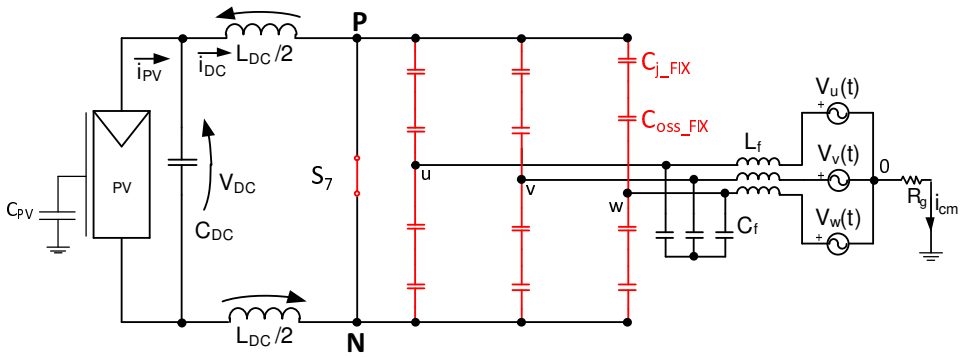

Figure 4. CSI7 topology in the case of Zero Vector applications with power devices parasitic capacitors.

In Current Source Inverter topologies, the common-mode voltage v_{cm} can be calculated using the star point of the three-phase grid voltage as voltage reference [24]:

$$v_{cm} = \frac{V_{P0} + V_{N0}}{2} \quad (1)$$

The variable v_{cmZC} was defined in [25] and represents the v_{cm} voltage in case of zero i_{cm}. The instantaneous value of v_{cmZC} (the same consideration is true for v_{cm}) shows a noticeable difference if the parasitic capacitance is considered.

Figure 5 shows the sequence of Alternated space vector modulation and the evolution of v_{cmZC} during a sampling period T_S: t_a and t_b represent the time intervals of Active Vectors while t_Z represents the time interval of the Zero Vector application as described in [5]. In the same figure, the blue square represents the area of the allowed values for v_{cmZC} during the Zero Vector application, due to the presence of the power devices parasitic capacitances.

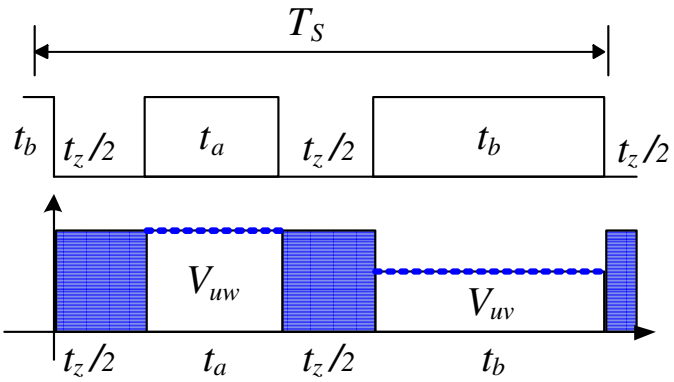

Figure 5. Evolution of v_{cmZC} (lower trace in blue) during a switching period in case of ASVM (active vectors during t_a and t_b, zero vector during t_z). v_{cmZC} evolution with ideal power devices in black trace, and with real power devices in red trace.

During the Zero Vector, i.e., during $t_Z/2$, the v_{cmZC} instantaneous value is not equal to zero (as in case of simulations with ideal switches), but its value depends on the circuit, which is obviously modified by the addition of the capacitance.

An additional equivalent parasitic capacitance can be simply added to the CSI7 common-mode circuit obtained with ideal switches [25].

Figure 6 shows the circuit considering the capacitance $C_{eq\text{-}parasitic}$ of the switches: during the active vectors, the capacitance is shorted by the switches.

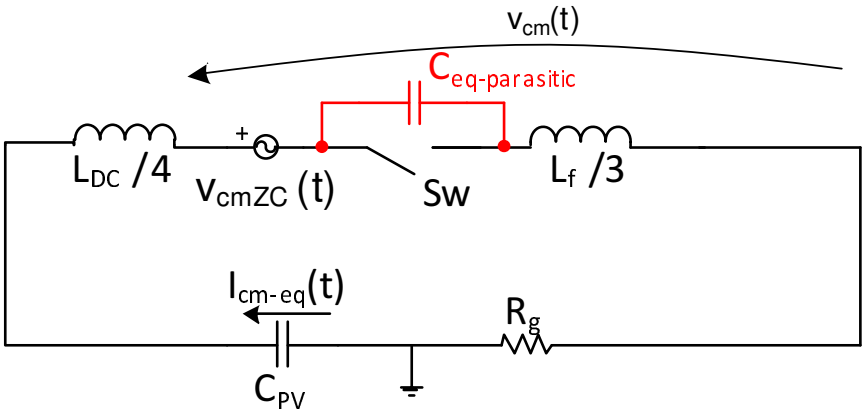

Figure 6. Equivalent common-mode circuit considering parasitic capacitors.

Starting from Figure 4 the value of $C_{eq\text{-}parasitic}$ can be simply computed as the parallel of six capacitors equal to the series of C_{oss} and C_j. The correctness of this last common-mode circuit will be verified in the following section.

Figure 7 shows the equivalent common mode circuit when a Zero Vector is applied, while Figure 8 shows the equivalent circuit in the case of Active Vector application. From these two circuits it is possible highlights the two resonant frequencies present in the equivalent common-mode circuit.

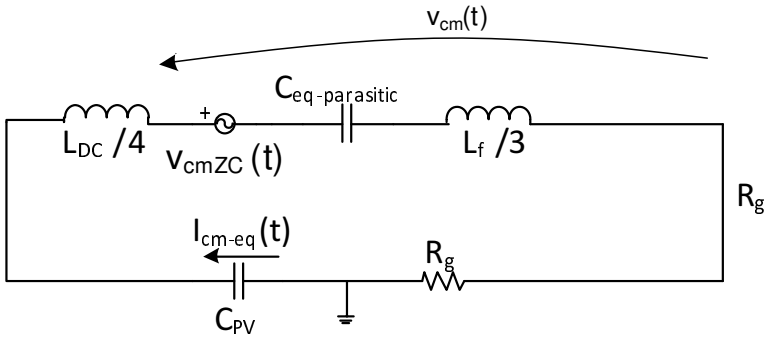

Figure 7. Equivalent common mode circuit in Zero state condition.

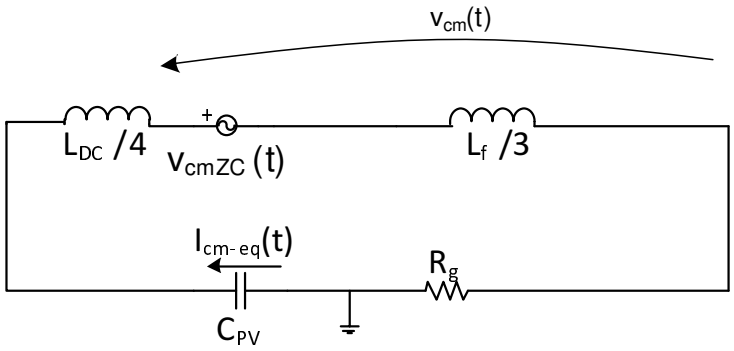

Figure 8. Equivalent common mode circuit in Active state condition.

3. Numerical Simulations

In this section, the behavior of CSI7 with the presence of parasitic capacitances C_{oss} and C_j is analyzed in MATLAB and PLECS environments. Table 1 summarizes the simulation and experimental parameters.

Table 1. Simulation parameters.

Name	Value	Unit	Name	Value	Unit
Input inductance L_{DC}	2	mH	Capacitor filter C_f	1.5	µF
Switching Period T_s	40	µs	PV panels capacitance C_{PV}	150	nF
Overlap time T_{ov}	1	µs	DC bus voltage V_{DC}	120	V
Line-to-line voltage V_{grid}	400	V_{RMS}	Mosfet parasitic capacitance C_{oss_Fix}	224	pF
Inductance filter L_f	1.4	mH	Diode parasitic capacitance C_{j_Fix}	191	pF
Ground resistance R_g	4.7	Ω	Equivalent parasitic capacitance $C_{eq\text{-}parasitic}$	619	pF
Grid frequency f_{grid}	50	Hz	Phase current I_{phase}	0.91	A_{RMS}

3.1. Matching between Variable and Fixed Capacitances

With the aforementioned parameters, the first step is to identify the equivalence between a variable output capacitor in Figure 2 and a fixed equivalent capacitor in Figure 4. The worst condition in terms of energy is represented during the maximum voltage across the capacitors (in this case, the output capacitance is equal to the minimum one).

This is an approximation able to simplify the analysis of the ground leakage current.

Figure 9 shows the waveform of the i_{cm} in case of variable (blue line) and fixed parasitic capacitance (dashed red line) values. It can be noted that this approximation introduces a good match despite some natural differences due to the variable resonance frequency obtained when C_{oss} and C_j are taken into account, however the RMS value with fixed parasitic capacitance is very close as reported in Table 2.

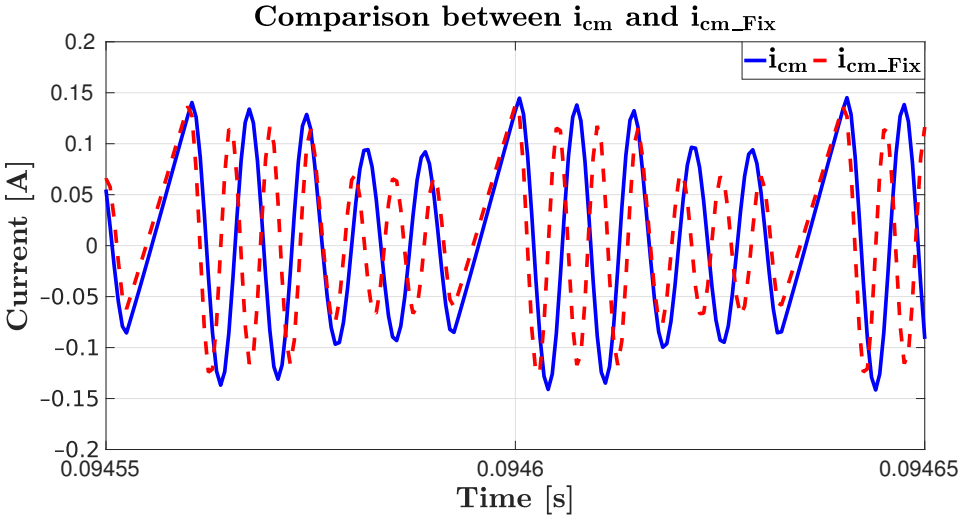

Figure 9. Comparison between i_{cm} (blue line) and i_{cm_Fix} (dashed red line) with C_{oss_Fix} and C_{j_Fix}.

Table 2. RMS values of i_{cm} in case of variable and fixed value of parasitic capacitance.

Case	RMS Current [A]
i_{cm}	0.0650
i_{cm_Fix}	0.0556

This approximation offers a good trade off to compute the RMS value with an easier simulation. For safety reasons, it is important to keep into consideration that the RMS value of the current is most important with respect to the harmonic content.

3.2. Validation of the Equivalent Common-Mode Circuit

With the previous assumptions, the following simulations will take into account fixed values of C_{oss} and C_j (considering the minimum one).

By analyzing Figure 6, it can be noted that for each state a different resonant circuit is obtained, see Figures 7 and 8.

Figure 10 shows the different behavior of the i_{cm_Fix} current (blue line) depending on the output vector of the converter, transitioning between the Zero and the Active Vectors (dotted red line). When an Active Vector is applied, it is worth noticing that i_{cm_Fix} varies, together with the oscillation frequency: this is consistent with the change of the resonance frequency of the common-mode circuit. When an Active Vector is applied, the common-mode equivalent circuit varies, since $C_{eq\text{-}parasitic}$ is short-circuited.

This is also apparent in Figure 11 where the dependency of v_{cmZC} (blue line) on Zero and Active Vectors (dotted red line) is shown. When a Zero Vector is applied, v_{cmZC} value remains constant, in accordance with the expected behavior from theory.

The Bode diagram of the transfer function $i_{cm}(s)/v_{cmZC}(s)$ is reported in Figure 12 for the equivalent common mode circuits in Figures 7 (blue line) and 8 (red line).

The resonance frequencies of the equivalent circuit are located before the switching frequency (in case of Active Vector) and near the 8th harmonic of the switching frequency (in case of Zero Vector).

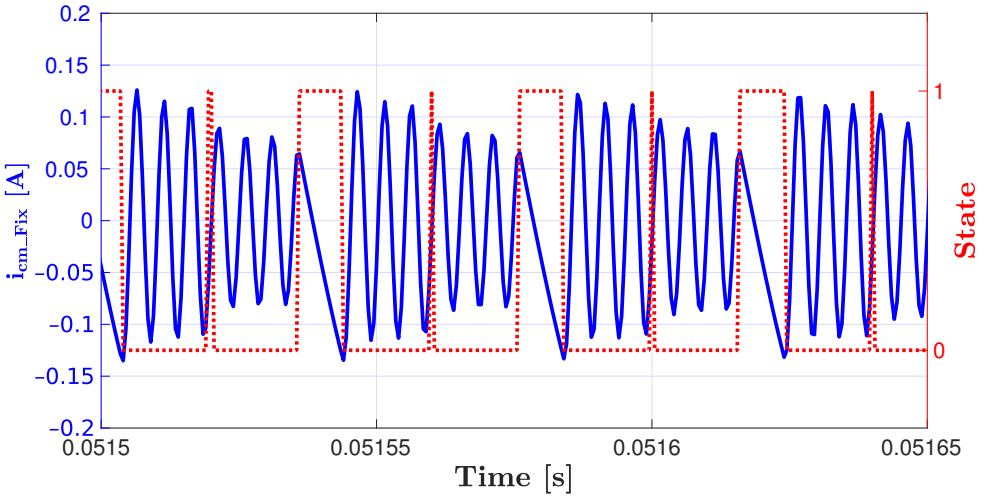

Figure 10. i_{cm_Fix} (blue line) evolution during Zero and Active Vectors. The zero value of the red trace represents the Zero Vector while the value 1 represents the application of any Active Vectors.

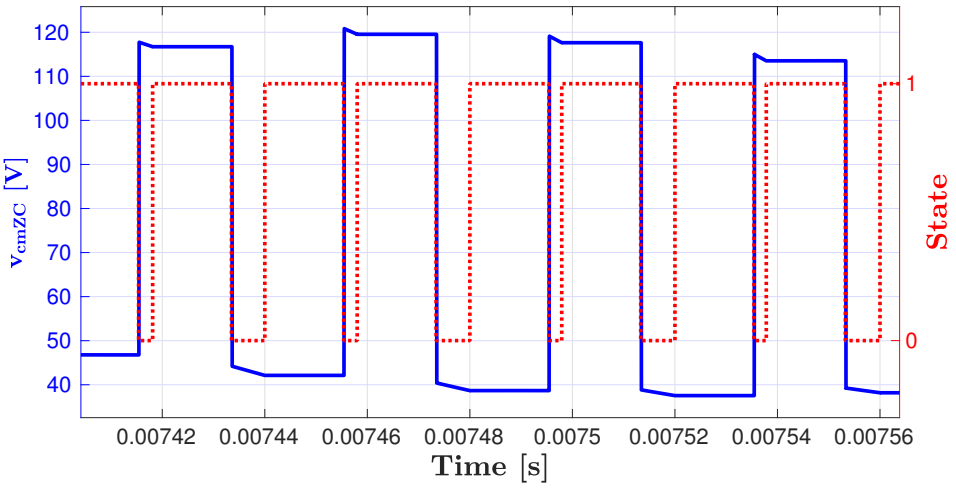

Figure 11. v_{cmZC} evolution in case of Zero Vector (State 0) and any Active Vectors (State 1).

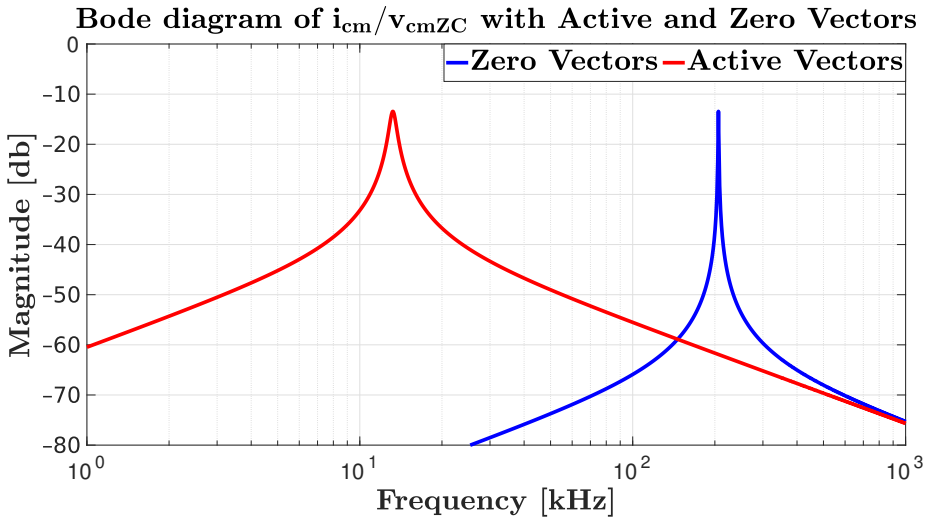

Figure 12. Bode diagram for Zero (blue) and Active (red) Vectors.

This particular situation can have a strong impact on the waveform of i_{cm_Fix}. In fact, in the equivalent circuit the resonance frequency of the Zero Vector matches the 8th harmonic of the switching frequency.

The correctness of the equivalent circuit of Figure 6 using power semiconductors models with constant parasitic capacitances is assessed in Figure 13 that puts in evidence the strong similarity between i_{cm_Fix} (blue line) and i_{cm-eq} (dashed red line).

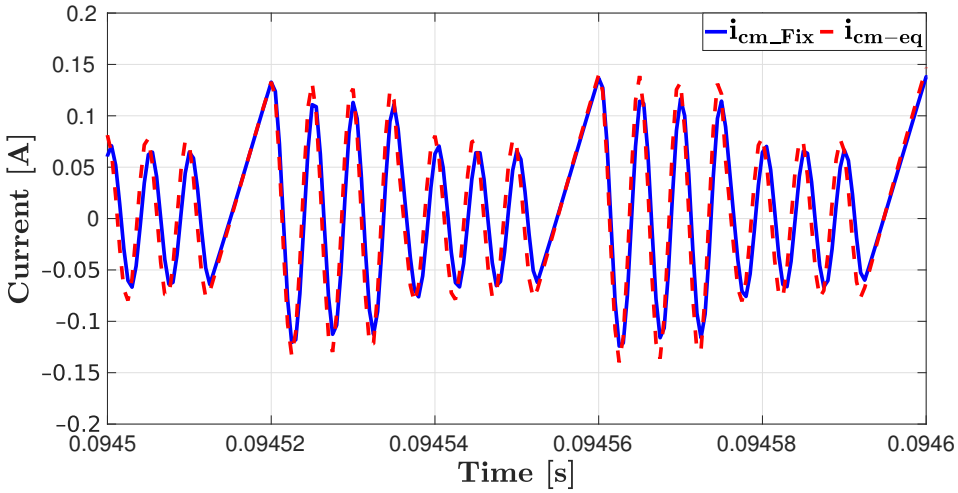

Figure 13. Comparison between i_{cm_Fix} (blue line) and i_{cm-eq} (dashed red line) with fixed capacitances.

In particular, it compares the i_{cm_Fix}, determined considering the entire power converter system shown in Figure 2 with fixed values of C_{oss} and C_j, and i_{cm-eq} calculated according to the equivalent circuit of Figure 6. The waveform of v_{cmZC} is obtained by means of simulation of the whole power converter system considering an open circuit path, instead of C_{PV}.

The simulation reports a good match between i_{cm_Fix} and i_{cm-eq} even in the presence of parasitic capacitances on power semiconductors as already shown in the first step of simulations.

3.3. Critical Aspects of the Resonant Frequency

In the following simulations constant values of C_{series} (defined as the series connection between C_{oss_Fix} and C_{j_Fix} for every single switch) will be considered, namely 220 pF, 440 pF, 660 pF and 880 pF. That bigger values consider other parasitic capacitance introduced by PCB, connections, etc.

The purpose of this simulation is to put in evidence the drawback introduced when the resonance frequency match exactly a harmonic of the switching frequency.

Figures 14 and 15 summarizes the waveforms of v_{cmZC} and their Fast Fourier Transform (FFT) obtained by varying the equivalent parasitic capacitance C_{series}. These figures confirm that v_{cmZC} is not influenced at all by the value of the semiconductor parasitic capacitance. Conversely, the ground leakage current i_{cm} is heavily affected. Figures 16 and 17 report the waveforms and spectra of i_{cm}, while RMS values of the i_{cm} currents are summarized in Table 3. Considering the obtained results, the worst case scenario is related to $C_{series} = 440$ pF. As previously mentioned, the reason lies in the different resonance frequency of the common-mode circuit. In fact, the resonance frequency response that happens during the Zero vector of $i_{cm}(s)/v_{cmZC}(s)$ results equal to 100 kHz, as reported also in Figure 18 Bode diagram. The resulting resonance frequency exactly matches the fourth switching frequency harmonic, thus determining high i_{cm} values. This is yet another example of the importance of the resonance frequency in the response of the equivalent common-mode circuit in practical implementations.

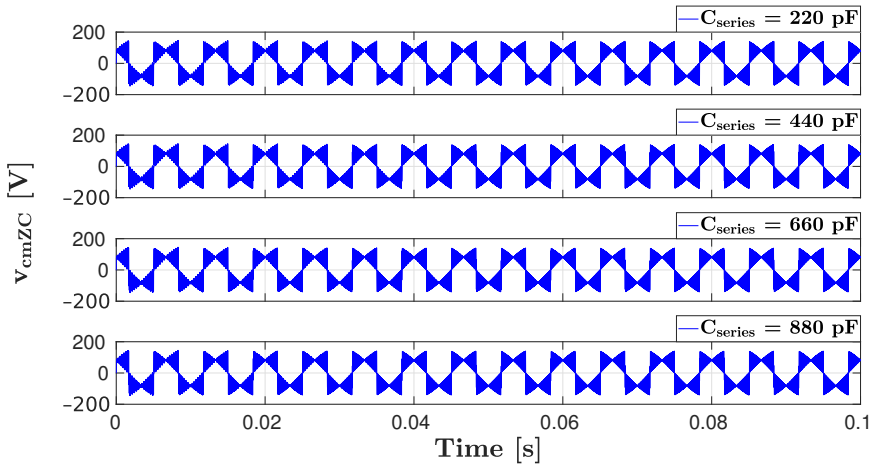

Figure 14. Waveforms of v_{cmZC} with different values of C_{series}.

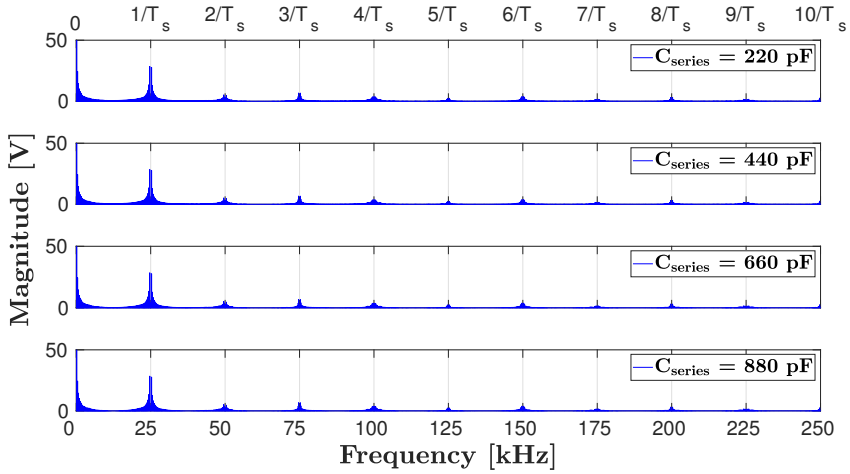

Figure 15. FFT of v_{cmZC} with different values of C_{series}.

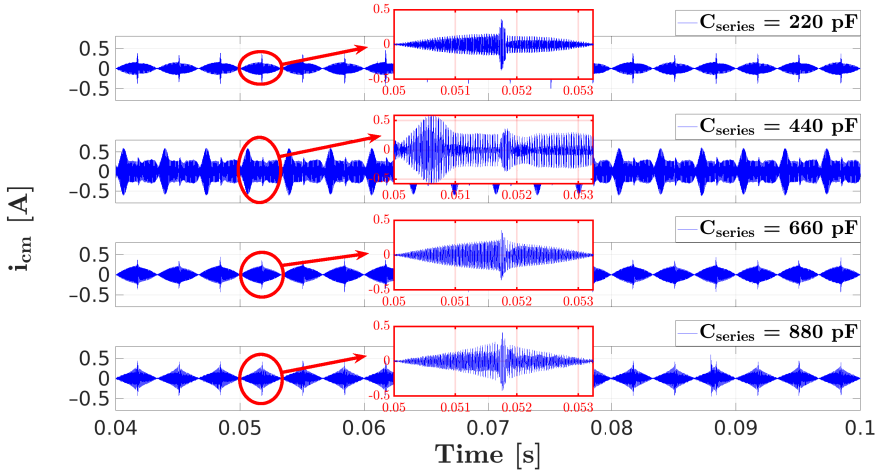

Figure 16. Waveforms of i_{cm} with different values of C_{series}.

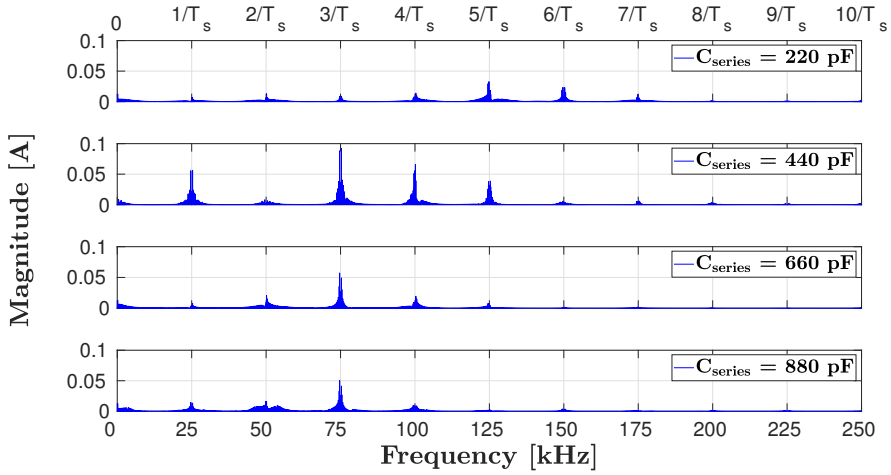

Figure 17. FFT of i_{cm} with different values of C_{series}.

Table 3. RMS values of the i_{cm} currents.

$C_{eq\text{-}parasitic} = 6 \cdot C_{series}$ [pF]	RMS Current [A]
$6 \cdot 220$	0.07119
$6 \cdot 440$	0.18296
$6 \cdot 660$	0.09214
$6 \cdot 880$	0.08938

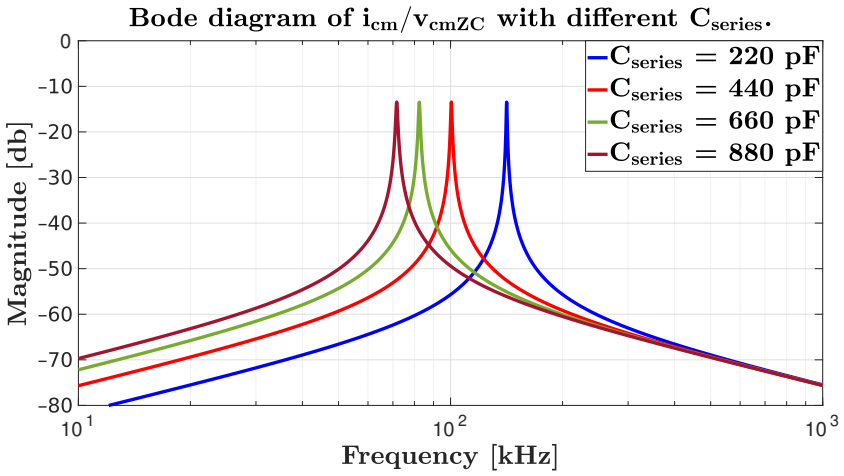

Figure 18. Bode Diagram of $i_{cm}(s)/v_{cmZC}(s)$ during Zero Vector application with different values of C_{series}.

3.4. Mitigation of the Resonance Problem

If the value of C_{series}, during the Zero Vector application, results in a resonance frequency of the common-mode circuit that is close to one of the harmonics of the switching frequency, a small output common mode choke L_{cm} can be added at the converter output to modify the resonance frequency.

The equivalent common-mode circuit shown in Figure 6 is modified into the one shown in Figure 19 by introducing the common mode choke L_{cm} converter output, thus changing the resonance frequency, as shown in Figure 20 in case of $L_{cm} = 3 \times 2\,\text{mH}$.

According to Figure 20 the RMS value of i_{cm} increases with C_{series} because the higher C_{series} is, the lower is the resulting the attenuation of the switching frequency components. Table 4 summarizes the RMS of i_{cm} with the presence of $L_{cm} = 3 \times 2\,\text{mH}$.

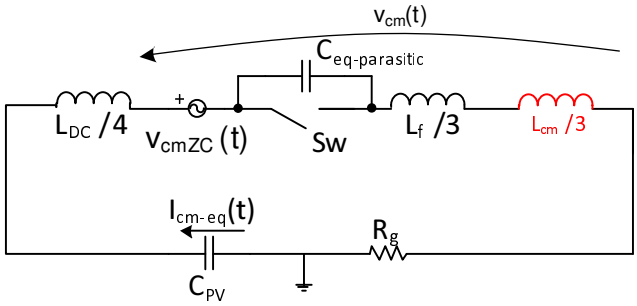

Figure 19. Equivalent common mode circuit with Common mode Filter.

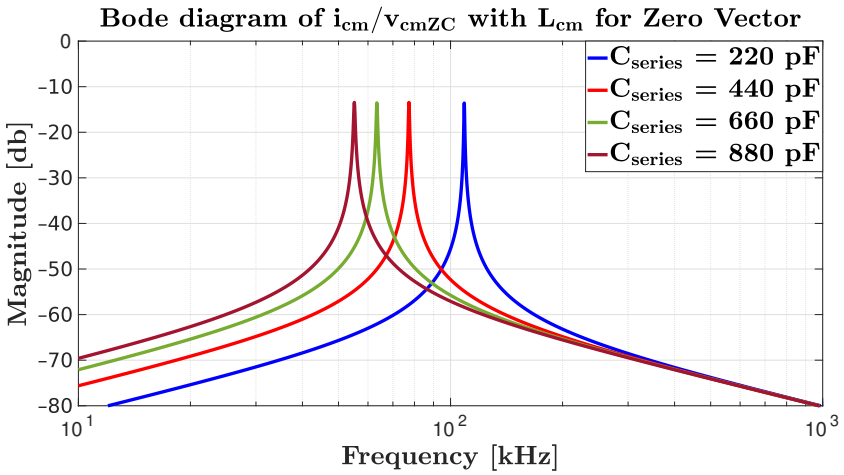

Figure 20. Bode Diagram of $i_{cm}(s)/v_{cmZC}(s)$ with different values of C_{series} and $L_{cm} = 3 \times 2\,\text{mH}$.

Table 4. RMS values of i_{cm} with $L_{cm} = 3 \times 2\,\text{mH}$.

$C_{eq\text{-}parasitic}$ [pF]	RMS Current [A]
$6 \cdot 220$	0.0396
$6 \cdot 440$	0.0715
$6 \cdot 660$	0.0836
$6 \cdot 880$	0.1360

Figure 21 shows the Bode diagram of $i_{cm}(s)/v_{cmZC}(s)$ during Active Vector application with and without $L_{cm} = 3 \times 2\,\text{mH}$, putting in evidence the shift of the resonance frequency with and without the L_{cm}. As shown by Figures 6 and 19 the switch S_W is closed during Active Vectors, so C_{series} does not influence the behavior during an Active Vector application.

By employing an additional L_{cm} the resonance frequency can be further decreased: in this particular example, it drops to 10 kHz, a value that is far lower than the fundamental switching frequency $f_s = 1/T_s = 25\,\text{kHz}$.

As can be seen in Figure 10, the attenuation of i_{cm} is higher during Active Vector time intervals.

The presence of parasitic semiconductor capacitances affected strongly the common-mode current, and to a much lesser extent the efficiency of the converter. Semiconductor power losses computations in case of null parasitic capacitances or with the aforementioned values do not provide significant variations. For that reason, semiconductor power losses results were not shown in this work. The computation of these last ones in case of a different number of PV panels, in standard CSI and CSI7 topology were analyzed in detail in [21].

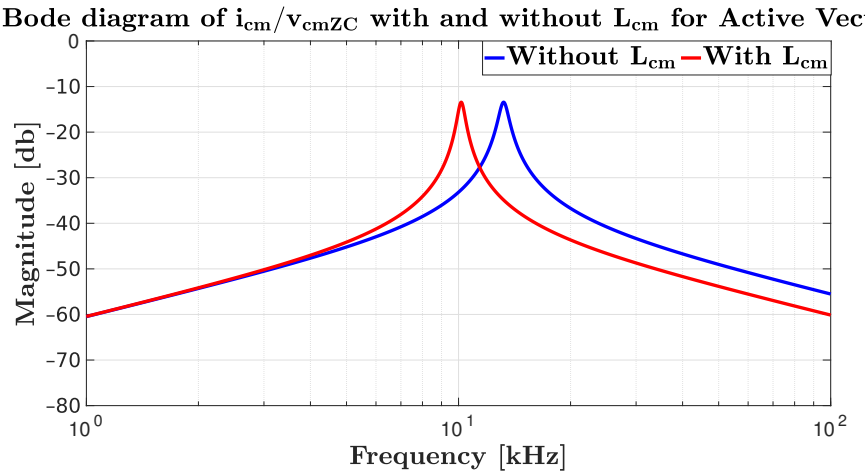

Figure 21. Bode Diagram of $i_{cm}(s)/v_{cmZC}(s)$ with and without $L_{cm} = 3 \times 2\,\text{mH}$ during Active Vectors application.

4. Experimental Results

The test setup, shown in Figure 22, comprising a prototype power converter, was used for experimental validation.

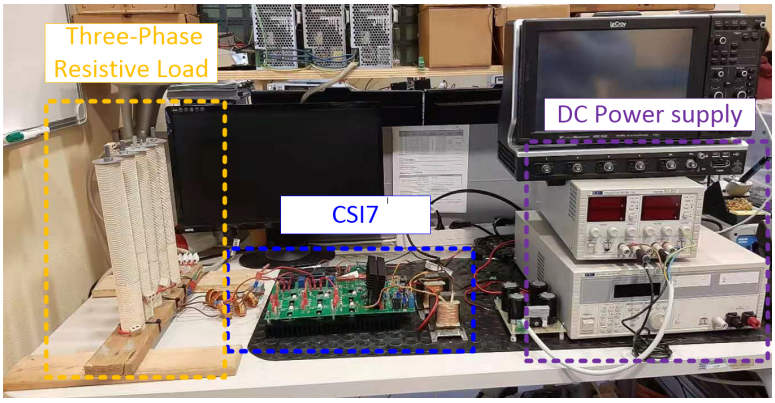

Figure 22. Picture of CSI7 power converter experimental setup.

The experiments are performed in an island operation with the converter connected to a ohmic load ($3 \cdot R_L = 3 \cdot 252\,\Omega$) with the parameters listed in Table 1.

Figure 23 shows the schematic of the experimental test bench, where a Hall effect current sensor was used to measure the current that flows through the series of R_g and C_{PV}.

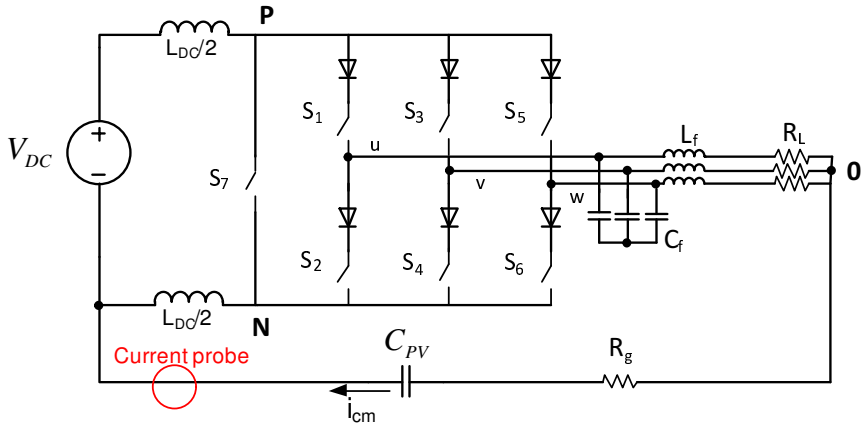

Figure 23. Schematic of the experimental test bench.

A power supply with voltage V_{DC} = 120 V is connected to the DC link and 0.91 A_{RMS} is chosen as current reference to achieve an AC voltage of V_{grid} = 400 V_{RMS} (reported in Figure 24).

It can be noted from Figure 25 that v_{cmZC} changes depend on the Active Vector but are constant during the Zero Vector (keeping its previous value), as expected by the theoretical analysis (Figure 11). More oscillations appear due to the stray inductance of the power converter.

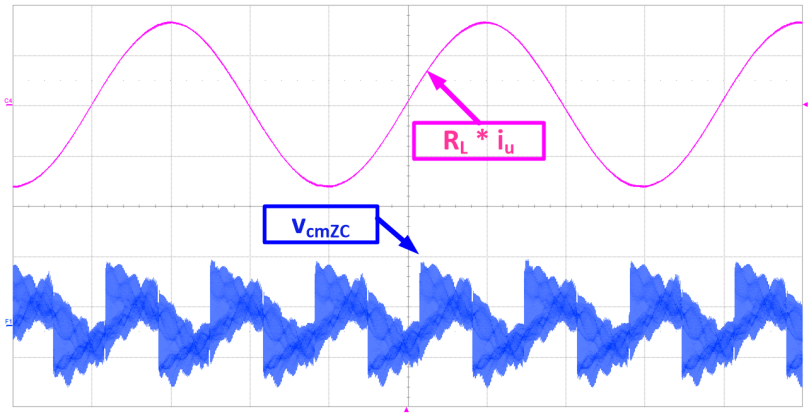

Figure 24. Experimental waveforms. $R_L \cdot i_u(t)$ (upper trace, 200 V/div), V_{cmZC} (lower trace, 100 V/div). The time division is 5 ms/div.

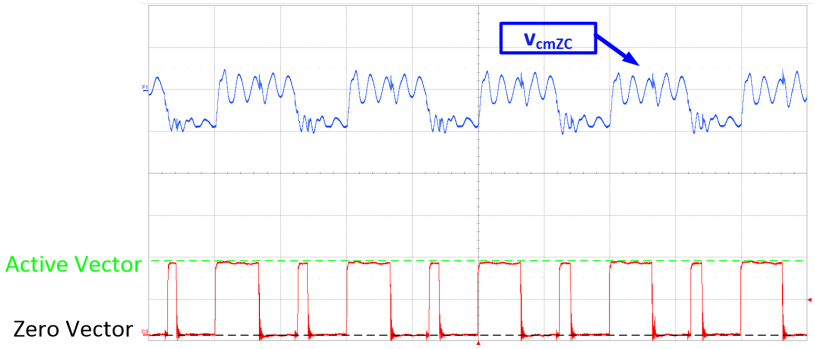

Figure 25. Experimental waveforms. v_{cmZC} (upper trace, 100 V/div) and States (lower trace). The time division is 20 µs/div.

Figures 26 and 27 show the evolution of i_{cm} without and with the connection of a 220 pF capacitor in parallel to every reverse-blocking switch.

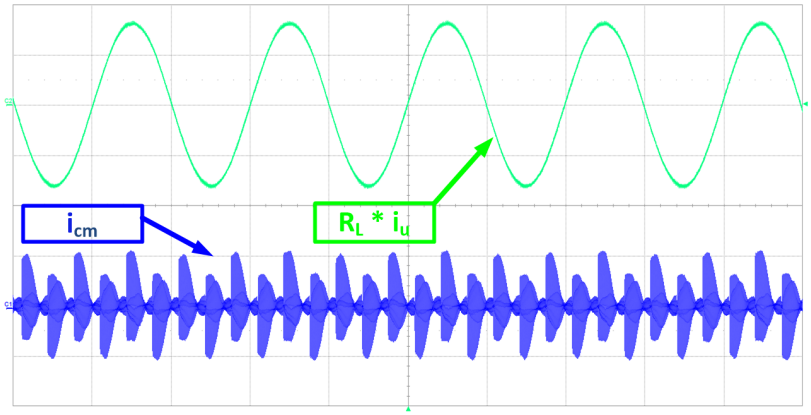

Figure 26. Experimental waveforms. $R_L \cdot i_u(t)$ (upper trace, 200 V/div), i_{cm} (lower trace, 200 mA/div). The time division is 10 ms/div.

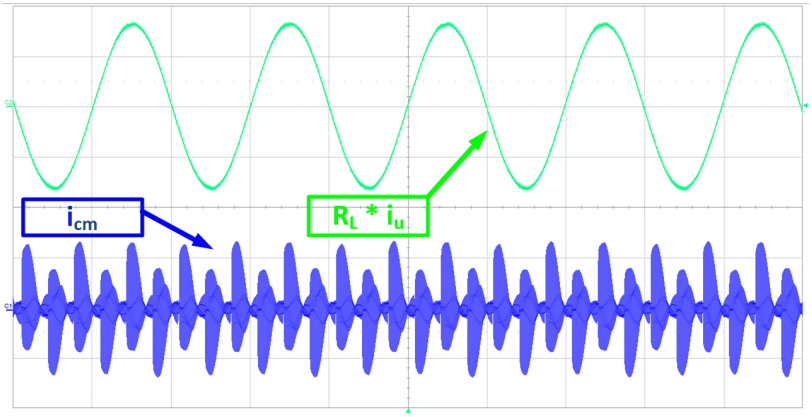

Figure 27. Experimental waveforms. $R_L \cdot i_u(t)$ (upper trace, 200 V/div), i_{cm} (lower trace, 200 mA/div). The time division is 10 ms/div.

In accordance with the theory, i_{cm} changes significantly, confirming the dependence on the parasitic capacitance. Increasing the capacitance leads to an increase of i_{cm} increases from 56.3 mA_{RMS} to 72.6 mA_{RMS}.

5. Conclusions

In this work the effect of the power device parasitic capacitances on ground leakage current was investigated in case of the CSI7 topology. Simulations and experiments show that the effect of device parasitic capacitances have a great impact on the behavior of CSI topologies that ideally present a separation between the DC source and the AC grid during the zero vector application. The same effect can be observed in case of VSI topologies that present an isolation from DC source to AC grid during certain time intervals of the switching period. Simulation results have proven the correctness of the equivalent common-mode circuit in predicting the two resonance frequencies during active and zero vector applications. In a practical implementation, taking into account real power semiconductor devices greatly impacts the ground leakage current. The critical issue is that different parasitic capacitance values of the power transistors can change greatly the resonance frequency values of the common-mode circuit. This work shows that if these resonance frequencies are close to harmonics of the switching frequency of the power converter, the ground leakage current (i.e., the common-mode current) greatly arises. To avoid the matching of these frequencies, thus reducing ground leakage current, an additional common-mode inductor should be added to change resonance frequencies values.

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