(Article begins on next page)

Ferroelectric-like charge trapping thin-film transistors and their evaluation as memories and synaptic devices

Article (Accepted Version)

http://sro.sussex.ac.uk

Ferroelectric-like Charge Trapping Thin-Film Transistors and Their Evaluation As Memories and Synaptic Devices

Alwin Daus*, Pawel Lenarczyk, Luisa Petti, Niko Münzenrieder, Stefan Knobelspies, Giuseppe Cantarella, Christian Vogt, Giovanni A. Salvatore, Mathieu Luisier and Gerhard Tröster

((Optional Dedication))

A. Daus, Dr. L. Petti, Dr. N. Münzenrieder, S. Knobelspies, G. Cantarella, C. Vogt, Dr. G. A. Salvatore, Prof. G. Tröster
Electronics Laboratory, ETH Zürich, Gloriastrasse 35, 8092, Zürich, Switzerland
E-mail: dausa@ife.ee.ethz.ch

P. Lenarczyk, Prof. M. Luisier
Integrated Systems Laboratory, ETH Zürich, Gloriastrasse 35, 8092, Zürich, Switzerland

Dr. N. Münzenrieder
Sensor Technology Research Center, Department of Engineering and Design, University of Sussex, BN1 9QT, Brighton, UK

This work presents a defect charging mechanism in 5 nm thick amorphous Al_2O_3 thin-films fabricated on plastic, which leads to multi-state memory effects, and thus the realization of synaptic thin-film transistors for neuromorphic applications. First, the Al_2O_3 thin-films are characterized in metal-insulator-metal stacks. These devices exhibit ferroelectric-like behavior, which is visible in the small-signal capacitance and the surface charge density. Furthermore, the quantum-mechanical simulation of the current-voltage characteristic leads to a physical model with trap charges close to the anode interface where deep-level traps are identified by fitting the experimentally obtained resonant tunneling peaks. The trap charge lifetime and frequency behavior is evaluated in $InGaZnO_4$ thin-film transistors, where the 5 nm thick amorphous Al_2O_3 layer is employed as the gate dielectric. At an operating voltage as low as ± 2 V, a charge trapping retention up to ~3 h and a discernable ON/OFF read-out with a factor >3 at 2 kHz are achieved. When subjected to a train of gate-source voltage

pulses, the thin-film transistors show charge integration properties which emulate the facilitating and depressing behaviors of biological synapses. These results indicate that thin low-temperature defect-rich metal-oxide dielectrics may be candidates for low-voltage memory applications and neuromorphic circuits on unconventional substrates.

1. Introduction

For many years, ferroelectric thin-films have been of great interest due to their possible application in electronic non-volatile memory devices.[1, 2] However, a successful down-scaling of the layer thickness to achieve low-voltage operations without compromising the electrical performance has still remained an unsolved challenge.[3, 4] In the urge for new materials, electrical polarization measurements have often been misinterpreted and false conclusions about ferroelectricity have been made.[5] In many cases, conventional polarization measurements lead to obscured results which are commonly caused by poor electrical insulating properties of nano-scale ferroelectrics.[6-8] Thus, the accurate determination of remanent polarization has been recently addressed by using specialized measurement protocols that can eliminate leakage components from the measurement and reveal the intrinsic remanent polarization.[9]

Interestingly, even non-ferroelectric materials can exhibit seemingly ferroelectric-like polarization; e.g., from space-charge polarization effects.[10] Recently, significant polarization due to ion movement has been reported for chicken albumen, which then has been implemented in a thin-film transistor (TFT) yielding a biodegradable memory device.[11] This example illustrates that alternative polarization mechanisms can be exploited in emerging memory technologies.

Similarly, metal-semiconductor Schottky contacts with a large number of interface traps have been proposed as material systems capable of mimicking ferroelectric electrical properties.[12]

Previous works on high-k dielectric metal-oxides (such as Al_2O_3, HfO_2, ZrO_2), which typically form Schottky contacts with metals, have reported on their intrinsic defect densities and their charge trapping behavior.[13-15] The migration of these defects has also been employed for resistive switching.[16-19] The chemical composition in abovementioned as well as other metal-oxides (e.g. $SrTiO_x$ or TiO_x) has been systematically altered to lead to oxygen deficiencies, which facilitate their application as resistive switching memories also known as memristors.[20-23] All the above-mentioned metal-oxides have in common that they are especially prone to deep level defects such as oxygen vacancies, which are believed to play a major role in charge trapping effects as well as in resistive switching dynamics.

Memristors have not only been envisioned as an alternative technology for digital memory. Due to their multi-state behavior,[18, 24] they also have been investigated as synaptic devices[25, 26] for neuromorphic systems realized as artificial brain-like circuits employing complementary metal oxide semiconductor (CMOS)-based neurons.[27, 28] These biologically inspired systems provide a large parallel processing capability that could dramatically improve the computational power compared to conventional processors with mainly sequential operations.[29]

In this work, we investigate the defect charging mechanisms in amorphous defect-rich alumina (Al_2O_3). In contrast to resistive switching memories, we do not target the formation of a defect chain throughout the metal-oxide layer which would modulate its resistance. Instead, we induce a capacitive charging effect manifesting itself as a ferroelectric-like behavior. Furthermore, we perform simulations based on quantum-mechanical tunneling and semi-classical hopping transport in an insulator thin-film with trap states. The simulation results reproduce the current-voltage characteristics of the thin film, confirming deep-level trap charges located within a ≤ 0.3 nm proximity to the anode. Finally, the defect charging and discharging is investigated in $InGaZnO_4$ ($IGZO$[30]) TFTs. The analog memory properties and

3

synaptic behavior of the TFTs are evaluated demonstrating their applicability in neuromorphic circuits.

2. Results and Discussion

2.1. Metal-Insulator-Metal stacks with Al_2O_3 thin-films

The schematic layer stack of the metal-insulator-metal (MIM) structure is shown in **Figure 1**a. The bottom electrode and top electrode consist of Ti/Au/Ti and Cu, respectively. The two metal electrodes are separated by a 5 nm thick Al_2O_3 layer deposited by atomic-layer deposition (ALD) at 150 °C. The stoichiometry of the ALD layer measured by Rutherford backscattering spectrometry indicates that the O/Al ratio resembles Al_2O_3. [31] However, we found a large hydrogen concentration of about 7 %, which is a common feature of low-temperature ALD.[32] The high impurity concentration provides a large intrinsic defect density inside the Al_2O_3. The devices are fabricated on a free-standing 50 µm thick polyimide foil. This demonstrates the applicability of the process to low-temperature fabricated electronics on unconventional substrates. Figure 1b displays a high-angle annular dark field (HAADF) transmission electron microscope (TEM) image of the cross-section. We performed a line scan with electron dispersive x-ray spectroscopy (EDX) and mapped the corresponding element detection as a function of depth (right side of Figure 1b). The material analysis shows a SiN_x adhesion layer on the bottom and a Pt top layer serving as a conductive surface for the preparation of the cross-section TEM-lamella by focused-ion beam (FIB) milling. The oxygen peak extends into the Ti region indicating a Ti surface oxidation, which resulted from the oxygen plasma cleaning of the bottom electrode prior to the ALD. The Cu peaks at the locations of Pt and Au are artefacts from the Cu TEM grid used for mounting.[33] In **Figure 2**, the electrical characterization results of the MIM structure are presented. The small-signal

capacitance of 5 nm thick Al_2O_3 shows a butterfly shape that is typical for ferroelectric materials,[34, 35] whereas thicker Al_2O_3 layers have a nearly constant capacitance without any hysteresis (see Figure 2a). Additionally, the effective dielectric constant of the 5 nm thick Al_2O_3 MIM capacitor is reduced to a value of 5.9 compared to a bulk value of ~7.4 due to an increasing impact of electrode interface effects.[36] Figure 2b displays the current density-voltage characteristics of the MIM structures with different Al_2O_3 thicknesses. The inset visualizes the triangular sweep function. The forward current density through the 5 nm thick Al_2O_3 thin-film has a significantly greater magnitude compared to the thicker layers. Additionally, a trap-assisted resonant tunneling peak[37, 38] is observed for the voltage back sweep. As previously mentioned, the measurement of the polarization (or surface charge density) is non-trivial for thin-films with large electrical leakage components. As expected, the polarization hysteresis measurement, acquired in a conventional triangular voltage sweep, exhibits a cigar-shape which is typical for lossy-dielectrics[5, 9] (see **Figure S1**). We investigated the trap-charging and leakage behavior of 5 nm thick Al_2O_3 by applying several consecutive unipolar triangular voltage sweeps (see **Figure S2**). We can conclude from these investigations that a significant component of the forward current density in 5 nm thick Al_2O_3 is caused by trap-charging and that the leakage current density through the device accounts for around half of the measured current density. Hence, the leakage is significant enough to disturb conventional polarization measurements. Thus, we generated a customized voltage sweep (Figure 2c, inset), which let us eliminate the leakage components from our measurement and extract the charging and discharging current densities of a single voltage sweep. The measurement consists of two consecutive sweeps for both the charge trapping and charge de-trapping mechanisms, where the blue part corresponds to the cumulative current density and the red part contains all components except the initial trap charging. Hence, the difference of these measurements (blue minus red) approximates the current density that corresponds to trap charging or discharging of a single voltage sweep. Between the charging

measurement (V = [+1.08 V +2 V]) and the discharging measurement (V < +1.08 V), the trapped charges need to be erased once which is done in the sweep interval between 50 s and 110 s (Figure 2c, inset). This is necessary, because two consecutive positive voltage sweeps result in higher charge trapping compared to a single sweep (see negative current peaks in Figure S2). The single pre-charging event prior to the de-trapping measurement is then performed in the sweep interval between 110 s and 140 s. For the current component marked in green, we were unable to construct the difference because the voltage back sweep de-trapping already starts in the range of interest (see Figure 2c). We assume for the further analysis that for the forward sweep between V = [0 V +1.04 V] the leakage components can be neglected. The integral of the current difference (blue – red and green) over time gives the surface charge density within the material (see Figure 2d). We obtain a surface charge density of ~60μC/cm^2 and a curve that is similar to ferroelectrics.[34, 35] The surface charge density acquired in a conventional rectangular voltage sweep (**Figure S3**) resembles a similar shape with greater magnitude. The main contribution of the leakage becomes visible at voltages ≥1.5 V in the negative voltage sweep direction. The remanent polarization protocol measured with an LC 2 ferroelectric tester (Radiant technologies) at a sweep time of 1 s, which has recently been verified with a leaky ferroelectric,[9] also leads to a significant surface charge density ~1.3μC/cm^2 for the 5 nm thick Al_2O_3 (see Figure 2d, inset). The significantly smaller surface charge density from the ferroelectric tester with an 80-fold faster sweep compared to our customized approach indicates a strong low-frequency dependence of the trapped charges.

2.2. Simulation of trap charge locations and energy levels in Al_2O_3

For further insight, we performed quantum-mechanical simulations combining methods presented in previous works.[39-41] These simulations enable us to find possible trap locations, energy levels, and charge states. **Figure 3**a represents the band diagram of the material system including the trap states that we associate with the observed device behavior. The work

function of Ti (4.33 eV)[42] and Cu (4.65 eV),[42] the Al_2O_3 conduction band offset (2.35 eV for Ti and 2.67 eV for Cu)[43, 44] and electron effective mass (0.28)[45] are all taken from literature. The Al_2O_3 bulk dielectric constant of 7.4 has been determined with the method presented by Groner et al.[36] All other parameters are used as fitting variables. The trap-capture cross-section was fitted to $4 \cdot 10^{-11}$ cm^2. The large energy distribution (≥ 0.40 eV) of the defects is a consequence of the broad negative peak in the current density. It agrees with the findings from other work on amorphous Al_2O_3.[15] The centers of the trap energy levels are situated at 2.33 eV, 3.25 eV, and 3.7 eV below the conduction band edge of Al_2O_3 and correspond to deep level mid-gap defect states e.g., oxygen vacancies[46] or aluminum dangling bonds.[47] The simulation predicts traps in immediate vicinity of the Cu anode (≤ 0.3 nm distance) with trap area densities of $1.1 \cdot 10^{12}$ cm^{-2} at 2.33 eV, $3 \cdot 10^{13}$ cm^{-2} at 3.25 eV, and $5 \cdot 10^{13}$ cm^{-2} at 3.7 eV. Assuming a homogeneous depth distribution of traps at the Cu side (within 0.2 nm) and taking into account the maximum number of charged (unoccupied) traps (see **Figure S4**a), we estimate a maximum volumetric charge density of ~$9 \cdot 10^{18}$ cm^{-3} on the Cu side which is comparable with other work.[15] The significant amount of these interface charges leads to a non-linear potential distribution Ψ close to the Al_2O_3/Cu interface (see Figure S4b). This change in the electrostatic environment has a positive dielectric polarization shift on the Cu side as a consequence (see Figure S4c), while the Ti side still shows the conventional dielectric polarization. In Figure 3b, the simulated and measured current density-voltage characteristics for 5 nm thick Al_2O_3 are compared. The black dashed line refers to the expected tunneling current density without any traps. The inset shows the separate transmission current densities from the respective trap levels. By combining the three trap levels mentioned above, the experimental and simulated current densities (red solid line) agree very well. Summarizing, the model confirms the presence of trap charges inside the Al_2O_3 thin film. The absence of the negative resonant tunneling peak for the forward voltage sweep suggests that the trap environment within the Al_2O_3 is altered when a positive voltage

is applied. Possible mechanisms for that could be trap ionization at the anode due to impact ionization[48, 49] or multi-phonon ionization[50] from local heating[51] as we discussed in our previous work.[31]

2.3. InGaZnO$_4$ thin-film transistors with 5 nm thick Al$_2$O$_3$ gate dielectrics

In the following, the charge trapping behavior of 5 nm thick Al$_2$O$_3$ is further evaluated within an IGZO TFT. A comparison of TFTs with different gate dielectric thicknesses can be found elsewhere.[31] **Figure 4**a presents the drain current I$_D$ and gate current I$_G$ as a function of the gate-source voltage V$_{GS}$. The device cross-section is schematized in the inset. The TFT shows counter-clockwise hysteresis in I$_D$, which confirms positive charges within the Al$_2$O$_3$ gate dielectric. Its V$_{GS}$ back sweep subthreshold swing is reduced below 60 mV/decade from charge de-trapping[52] thereby demonstrating its low-power capability. These features also indicate a ferroelectric-like charge trapping behavior in the TFTs as both the counter-clockwise I$_D$ hysteresis and the sub-60 mV/decade subthreshold swing can be found in field-effect transistors with ferroelectric gate insulators.[53] The I$_G$ has a similar behavior compared to the transmission current density in the MIM structure (see Figure 2b). The I$_D$ and I$_G$ as a function of V$_{GS}$ for ten different TFTs showing comparable behaviors can be reviewed in **Figure S5**. The I$_D$ hysteresis is evaluated by determining the threshold voltage shift ΔV$_{Th}$ which rises for larger maximum gate-source voltages V$_{GS, max}$ (see Figure 4b). This indicates an increased charge trapping for larger V$_{GS, max}$. The lifetime of the trap charges can be evaluated in TFT retention measurements, where first a write (Wr) or erase (Er) pulse is applied and subsequently the I$_D$ is read-out at V$_{GS}$ = 0 V. The result is presented in Figure 4c, where an increased retention for longer Wr/Er pulses can be observed. The maximum retention is found to be in the order of ~3 h for a Wr/Er pulse of 30 s. Subsequently, the frequency behavior of the charge trapping is investigated. The TFTs are subjected to an AC modulation of V$_{GS}$ at a constant drain-source voltage V$_{DS}$ = 100 mV and I$_D$ is measured with a

current amplifier (see **Figure S6**). The V_{GS} AC modulation is rectangular and follows a sequence of Wr at +2 V, read-high (RH) at 0 V, Er at -2 V and read-low (RL) at 0 V. **Figure 5**a and Figure 5b display two examples of the modulated I_D at 1 Hz and 1 kHz Wr/Er-frequency, respectively. The frequency dispersion of I_D (Figure 5c) shows that the Wr-current is significantly larger than the RH-current, whereas the Er-current as well as the RL-current are several orders of magnitude smaller (similarly as in Figure 4). The inset reveals that the RH current is still a factor of ~3 larger than the RL current at a frequency of 2 kHz. Lastly, this configuration is tested in 3000 cycles at a frequency of 10 Hz, demonstrating a stable ratio RH/RL >80 (see Figure 5d).

Comparing the memory properties of our defect-rich Al_2O_3 TFTs to other low-temperature processed and low-voltage memory transistors, we find the following: the programming voltage of this TFT with ±2 V is less than half compared to previous reports.[54-56] However, the device retention of a few hours still needs improvement and is an issue that has also been reported for very thin dielectric layers in floating gate memory devices.[54] We believe that in the Cu/Al_2O_3 system the energy level of the deep-level defects as well as the Fermi energy of the Cu gate electrode are the physical measures defining the retention properties of the trap charges. The careful design of a system where the defect-rich gate dielectric contains positive and stabilized charge states with respect to the gate Fermi level is expected to improve the retention in future devices. With the help of our simulation framework, we find that the largest trapping and detrapping modulation of the relative trap occupancy happens when the center of the trap level is equal to the Fermi energy of the gate metal (see **Figure S7**). In this configuration, a significant portion of the charged traps remains stable at 0 V applied over the dielectric. Furthermore, we find that the trap charges are significantly more stable when situated further away from the interface between the gate dielectric and metal. However, it should be noted that trap states in greater distance from the interface take longer to be

occupied/unoccupied which impairs the frequency performance of the device.[15] Thus, a trade-off between the amount of trap charges, which is enhanced for a greater depth, and the trapping/detrapping frequency has to be found. The varieties of possible metal-oxide materials with large oxygen vacancy concentrations provide many opportunities to investigate the trapping/detrapping mechanisms at different energy positions for the positive trap charges.[13, 14]

From the analysis of the charge/detrapping behavior of the MIM structures and TFTs, we find that these devices are suitable to emulate biological synapses. The main requirement for such an application is the integration of subsequent stimuli where the device output depends on the present stimulus as well as on the past ones.[28] Our results on several consecutive positive voltage sweeps for the MIM structures highlight this behavior, as the negative detrapping current density peak becomes significantly larger the more positive voltage sweeps are applied prior to detrapping (see Figure S2). Additionally, the transient response of the TFT I_D on positive V_{GS} suggests that the electrostatic effect of the trap charges on the TFT channel is an integral of V_{GS} over time (Figures 5a, 5b and 5c). Thus, we investigated the synaptic functionality of the TFT in more details. This is typically done by monitoring the device response on a train of voltage pulses.[57, 58] Similarly to previous work,[57] we show in **Figure 6** the behavior of a facilitating a) and depressing b) synapse. These results are enabled by the short-term memory properties of our devices. The long-term memory is limited to the retention in Figure 4c, which is comparable to prior work in the order of hours.[57, 58] Another important property of a synaptic device is the dependence of the output signal on the time interval between pulses. Consequently, we investigated this behavior for a pulse width of 0.5 s separated by periods of 0.25 s to 10 s (see Figure 6c). The device displays facilitating and depressing characteristics for short and long time intervals, respectively, which as well resembles the behavior of biological synapses.[57] In **Figure S8**, the facilitating behavior of the

synaptic TFT is reported for a V_{GS} excitation with a 50 % duty cycle at larger frequencies up to 500 Hz.

The implementation of synaptic functionality in these three-terminal devices provides an architectural advantage compared to the two-terminal memristors where the signal transmission and learning function typically cannot be carried out simultaneously.[58] In three-terminal components (i.e., TFTs), the signal transmission is performed via the TFT channel and the learning function (modulation of the synaptic weight) is carried out independently via the gate. Other realized synaptic transistors mainly rely on the movement of ionic species in electrolytes and ion gels.[59-61] These approaches suffer from challenges in reliability and environmental dependence *e.g.*, humidity.[58] The movement of oxygen vacancies in relatively thick Ta_2O_{5-x} dielectrics (120 – 350 nm) has led to similar TFT behavior and operation conditions as in our approach.[58] In comparison, our ultra-thin (5 nm) Al_2O_3 dielectric based TFTs show even lower synaptic operating voltage (1.5 V) and broader frequency range (up to 500 Hz).

3. Conclusion

We observed butterfly shaped small-signal capacitance-voltage characteristics and ferroelectric-polarization-like surface charge density hysteresis in 5 nm thick defect-rich Al_2O_3. Quantum-mechanical simulations confirmed the existence of charged deep-level defects in proximity to the Cu anode. The charge trapping retention and speed were investigated in IGZO TFTs where the Al_2O_3 layer was employed as a gate dielectric. Furthermore, we demonstrated that these TFTs can be utilized as synapses in neuromorphic circuits. These findings promise low-voltage operation of ±2 V and 1.5 V for the memory and the synaptic device, respectively. In future, defect-engineered metal-oxide dielectrics based TFTs could provide many opportunities for emerging memory as well as neuromorphic applications.

4. Experimental Section

Device fabrication: The devices were fabricated on free-standing polyimide foil with a thickness of 50 μm. The substrates underwent an initial cleaning in 2-propanol and acetone by sonication in an ultrasonic bath for 5 min. Subsequently, the substrates were baked in an air oven at 200 °C for 24 hours. Then, the foils were encapsulated in 50 nm thick SiN_x passivation layers which were deposited on both sides by plasma-enhanced chemical vapor deposition at 150 °C. The bottom (or source/drain) electrodes were realized by a Ti/Au/Ti (5/30/5 nm) layer which was electron-beam evaporated and structured by optical lithography and lift-off. Then, a UV-ozone cleaning for 1 min was performed. A 15 nm thick IGZO semiconductor was deposited by RF magnetron sputtering at room temperature using an $InGaZnO_4$ target. The layer was structured by photolithography and wet chemical etching. IGZO islands were formed for the thin-film transistors. In other locations, the semiconductor was completely removed to allow for the realization of the metal-insulator-metal capacitors. The Al_2O_3 layers with different thicknesses were deposited by thermal atomic-layer deposition at 150 °C. Contact holes were defined by optical lithography and wet chemically etched. Finally, a 20 nm thick Cu layer, serving as top (or gate) electrodes, was electron-beam evaporated (substrate rotating at an angle of 30°). The layer was structured thereafter by optical lithography and wet chemical etching.

Electrical characterization: The electrical measurements were performed on a probe station at ambient conditions. The small-signal capacitance was measured on a ModLab MTS MAT-1MHz test system with an AC modulation amplitude of 100 mV and a modulation frequency of 10 Hz. The DC sweep rate for Al_2O_3 with thicknesses of 5 nm, 10 nm and 20 nm was 40 mV/s, 80 mV/s, 160 mV/s, respectively. The direct measurement of polarization hysteresis

and remanent polarization was performed on a ferroelectric tester LC II from Radiant Technologies.

The current-voltage characteristics of the metal-insulator-metal stacks as well as the thin-film-transistors were measured on a semiconductor device analyzer B1500A (Agilent technologies). The frequency dependent analysis of the thin-film transistors according to the schematic in Figure S6 was done with an Agilent waveform generator (33522A) connected to the gate. The constant drain-source voltage was applied with a Keysight precision source/measure unit (B2902A). At the source, a current amplifier (Stanford Research Systems, Model SR570) was connected which converted the current to a voltage for the display on the oscilloscope (Agilent Technologies, MSO-X 3014A). This was also the configuration for the frequency dependent measurements on the synaptic response (Figure S8). The synaptic responses of the TFTs at a pulse frequency of 2 Hz (Figure 6) were acquired with the Keysight precision source/measure unit (B2902A).

Simulation: Based on the quantum-mechanical tunneling and semi-classical hopping mechanisms, the electron transport characteristics in a thin dielectric film were calculated. For that purpose, we invoked the current conservation law at each localized trap site i. The time evolution of the site occupation probability f_i contained: 1) the rate for an electron to hop into this trap site from the other trap sites j; 2) the rate to escape to other trap sites from this trap site; 3) the net tunneling rate between the trap site i and the cathode c; 4) the net tunneling rate to the anode a. Therefore the phenomenon can be described as:

$$\frac{df_i}{dt} = (1 - f_i) \sum_j \nu_{i,j} f_j - f_i \sum_j (1 - f_j) \nu_{j,i} + J_{i,c} + J_{i,a} \qquad (1).$$

As for the hopping rates between localized trap sites i and j we used the standard Miller-Abrahams formula[39]:

$$v_{i,j} = v_0 \exp(-2\alpha r_{i,j} - E_{i,j}/kT) \tag{2},$$

where v_0 is the attempt to escape frequency, α^{-1} is the localization length, $r_{i,j}$ is the distance and $E_{i,j}$ is the energy difference of the two trap sites.

The tunneling rates were calculated within a formalism based on the Landauer-Buttiker formula for the current while employing the detailed balance at thermal equilibrium for the capture-emission from localized trap sites[40], which resulted in the following expressions for the net particle currents (unit: s^{-1}) between the trap site i and the cathode c or the anode a:

$$J_{i,c/a} = \int \sigma_{i,c/a}(E) \cdot (1 - \frac{f_i}{f_{c/a}(E)}) dE \tag{3}$$

In Equation (3), $f_{c/a}(E)$ is the Fermi-Dirac distribution function in the cathode/anode and σ is the trap site capture rate (unit: $s^{-1}\ eV^{-1}$) which we calculated as:

$$\sigma_{c/a,i}(E) = \frac{m^* kT}{\pi \hbar^3} \cdot \sigma_0 \cdot D_i(E) \cdot P_{i,c/a}(E) \cdot F_{c/a}(E) \tag{4},$$

where m^* is the electron tunneling mass in the dielectric, T is the temperature, k denotes the Boltzmann constant, $\hbar$ denotes the reduced Planck constant, σ_0 is the trap capture cross-section (unit: cm^2), $D_i(E)$ is the site energy distribution function (unit: $e\ V^{-1}$), $P_{i,c/a}(E)$ is the tunneling probability from the cathode/anode to the trap site i, and $F_{c/a}(E)$ resulted from the integration of the cathode/anode Fermi-Dirac distribution over transverse wave vectors.

In the simulations, the trap site energy distribution was assumed to be Gaussian centered at the site discrete energy level E_i. The tunneling probability was computed within the WKB approximation[41]. The total current density (unit: $A\ cm^{-2}$) flowing through the dielectric was obtained from the elementary contributions as:

$$J_{tot} = J_{c,a} + \bar{e} N_t \sum_i (J_{i,a} - J_{i,c}) \tag{5},$$

where $J_{c,a}$ is the one-step tunneling current between the cathode and the anode (unit: $A\ cm^{-2}$), $\bar{e}$ denotes elementary charge and N_t is the areal density of traps (unit: cm^{-2}).

14

The self-consistent coupling to Poisson's equation through the surface charge density $N_i = \bar{e}N_t f_i$ provided the band bending that influences both transport mechanisms. Finally, the polarization was calculated using the standard formula:

$$P = \frac{1}{\epsilon_0(\epsilon_r - 1)}F \tag{6},$$

where F is the electric field, ε_0 is the vacuum permittivity and ε_r is the relative permittivity of the material.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.
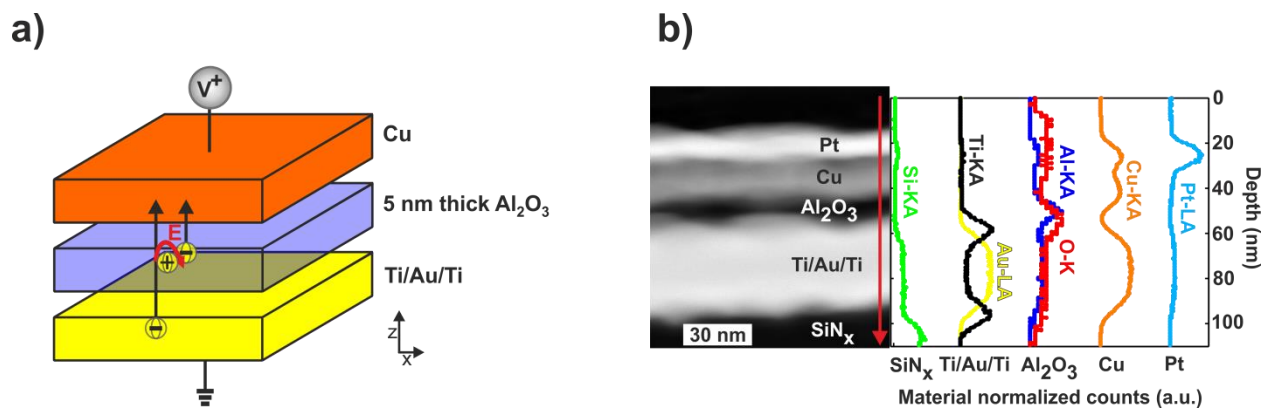
References

[1]   S. Y. Wu, *IEEE Trans. Electron Devices* **1974**, *21*, 499.

[2]   J. F. Scott, P. De Araujo, A. Carlos, *Science* **1989**, *246*, 1400.

[3]   T. P. Ma, J. P. Han, *IEEE Electron Device Lett.* **2002**, *23*, 386.

[4]   H. Kohlstedt, Y. Mustafa, A. Gerber, A. Petraru, M. Fitsilis, R. Meyer, U. Böttger, R. Waser, *Microelectron. Eng.* **2005**, *80*, 296.

[5]   J. F. Scott, *J. Phys. Condens. Matter* **2007**, *20*, 021001.

[6]   J. Kim, S. A. Yang, Y. C. Choi, J. K. Han, K. O. Jeong, Y. J. Yun, D. J. Kim, S. M.

Yang, D. Yoon, H. Cheong, K. S. Chang, *Nano Lett.* **2008**, *8*, 1813.

[7]   H. Kliem, R. Tadros-Morgane, *J. Phys. D: Appl. Phys.* **2005**, *38*, 1860.

[8]   T. Tybell, C. H. Ahn, J. M. Triscone, *Appl. Phys. Lett.* 1999, *75*, 856.

[9]   U. Chowdhury, S. Goswami, D. Bhattacharya, A. Midya, P. Mandal, *Appl. Phys. Lett.*

2016, *109*, 092902.

[10]   H. Kliem, B. Martin, *J. Phys. Condens. Matter* **2008**, *20*, 321001.

[11]   S.-J. Kim, D.-B. Jeon, J.-H. Park, M.-K. Ryu, J.-H. Yang, C.-S. Hwang, G.-H. Kim,

S.-M. Yoon, *ACS Appl. Mater. Interfaces* **2015**, *7*, 4869.

[12]   L. Pintilie, M. Alexe, *Appl. Phys. Lett.* **2005**, *87*, 112903.

[13]   J. Robertson, R. M. Wallace, *Mater. Sci. Eng. R* **2015**, *88*, 1.

[14]   J. Robertson, *Solid-State Electron.* **2005**, 49, 283.

[15]   R. Degraeve, M. Cho, B. Govoreanu, B. Kaczer, M. B. Zahid, J. Van Houdt, M.

Jurczak, G. Groeseneken, In *Trap Spectroscopy by Charge Injection and Sensing (TSCIS): A*

Quantitative Electrical Technique for Studying Defects in Dielectric Stacks; IEEE Int.

Electron Dev. Meet.: San Francisco, 2008; pp. 1-4.

[16]   S. Yu, H. Y. Chen, B. Gao, J. Kang, H. S. P. Wong, *ACS Nano* **2013**, *7*, 2320.

[17]   G. Bersuker, D. C. Gilmer, D. Veksler, P. Kirsch, L. Vandelli, A. Padovani, L. Larcher,

K. McKenna, A. Shluger, V. Iglesias, M. Porti, *J. Appl. Phys* **2011**, *110*, 124518.

[18]   S. Balatti, S. Larentis, D. C. Gilmer, D. Ielmini, *Adv. Mater.* **2013**, *25*, 1474.

[19]   C. Y. Lin, C. Y. Wu, C. Y. Wu, C. Hu, T. Y. Tseng, *J. Electrochem. Soc.* **2007**, *154*,

G189.

[20]   J. Shang, G. Liu, H. Yang, X. Zhu, X. Chen, H. Tan, B. Hu, L. Pan, W. Xue, R. W. Li,

Adv. Funct. Mat. **2014**, *24*, 2171.

[21]   J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart, R. S. Williams, *Nat.*

Nanotechnol. **2008**, *3*, 429.

[22]   F. Messerschmitt, M. Kubicek, J. L. Rupp, *Adv. Funct. Mat.* **2015**, *25*, 5117.

[23]   R. Waser, R. Dittmann, G. Staikov, K. Szot, *Adv. Mater.* **2009**, *21*, 2632.

[24]   K. Nagashima, T. Yanagida, K. Oka, M. Taniguchi, T. Kawai, J. S. Kim, B. H. Park, *Nano Lett.* **2010**, *10*, 1359.

[25]   Z. Q. Wang, H. Y. Xu, X. H. Li, H. Yu, Y. C. Liu, X. J. Zhu, *Adv. Funct. Mat.* **2012**, 22, 2759.

[26]   S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, W. Lu, *Nano Lett.* **2010**, *10*, 1297.

[27]   K. H. Kim, S. Gaba, D. Wheeler, J. M. Cruz-Albrecht, T. Hussain, N. Srinivasa, W. Lu, *Nano Lett.* **2011**, 12, 389.

[28]   A. Thomas, *J. Phys. D: Appl. Phys.* **2013**, *46*, 093001.

[29]   D. Monroe, *Commun. ACM* **2014**, *57*, 13.

[30]   K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* **2004**, 432, 488.

[31]   A. Daus, C. Vogt, N. Münzenrieder, L. Petti, S. Knobelspies, G. Cantarella, M. Luisier, G. A. Salvatore, G. Tröster, *J. Appl. Phys.* **2016**, *120*, 244501.

[32]   M. D. Groner, F. H. Fabreguette, J. W. Elam, S. M. George, *Chem. Mater.* **2004**, *16*, 639.

[33]   J. Hu, M. Li, Q. Gao, C. Niou, W. T. K. Chien, In *Energy Dispersive Spectrum (EDS) Study of Copper Grid Effect on Semiconductor Failure Analysis*; Int. Symp. Test. Fail. Anal.: Austin, 2006; pp. 297-299.

[34]   R. Moazzami, C. Hu, W. H. Shepherd, *IEEE Trans. Electron Devices* **1992**, *39*, 2044.

[35]   K. H. Lee, G. Lee, K. Lee, M. S. Oh, S. Im, S. M. Yoon, *Adv. Mater.* **2009**, *21*, 4287.

[36]   M. D. Groner, J. W. Elam, F. H. Fabreguette, S. M. George, *Thin Solid Films* **2002**, *413*, 186.

[37]   R. I.Yamada, J. Yugami, M. Ohkura, In *Charging and Intrinsic-Leakage Current Peaks in Thin Silicon-Dioxide Films*; IEEE Symp. on VLSI Technol.: Kyoto, 1997; pp. 147-148.

[38]   A. I. Chou, K. Lai, K. Kumar, P. Chowdhury, J. C. Lee, *Appl. Phys. Lett.* **1997**, *70*, 3407.

[39]   M. Z. Szymański, B. Łuszczyńska, D. Djurado, *IEEE J. Sel. Topics Quantum Electron.* **2013**, *19*, 1.

[40]   D. Ielmini, A. S. Spinelli, M. A. Rigamonti, A. L. Lacaita, *IEEE Trans. Electron Devices* **2000**, *47*, 1258.

[41]   Á. Szabó, M. Luisier, *IEEE Trans. Electron Devices* **2013**, 60, 2353.

[42]   D. E. Eastman, *Phys. Rev. B* **1970**, *2*, 1.

[43]   Y. N. Novikov, V. A. Gritsenko, K. A. Nasyrov, *JETP Lett.* **2009**, *89*, 506.

[44]   J. J. Brady, V. P. Jacobsmeyer, *Phys. Rev.* **1936**, *49*, 670.

[45]   Y. T. Hou, M. F. Li, H. Y. Yu, D. L. Kwong, *IEEE Electron Device Lett.* **2003**, *24*, 96.

[46]   D. Liu, S. J. Clark, J. Robertson, *Appl. Phys. Lett.* **2010**, *96*, 032905.

[47]   M. Choi, A. Janotti, C. G. Van De Walle, *J. Appl. Phys.* **2013**, *113*, 044501.

[48]   Y. B. Park, D. K. Schroder, *IEEE Trans. Electron Devices* **1998**, *45*, 1361.

[49]   J. Maserjian, N. Zamani, *J. Vac. Sci. Technol.* **1982**, *20*, 743.

[50]   C. Bonnelle, *Phys. Rev. B* **2010**, *81*, 054307.

[51]   E. Yalon, I. Riess, D. Ritter, *IEEE Trans. Electron Devices* **2014**, *61*, 1137.

[52]   A. Daus, C. Vogt, N. Münzenrieder, L. Petti, S. Knobelspies, G. Cantarella, M. Luisier, G. A. Salvatore, G. Tröster, *IEEE Trans. Electron Devices* **2017**, *64*, 2789.

[53]   S. Dasgupta, A. Rajashekhar, K. Majumdar, N. Agrawal, A. Razavieh, S. Trolier-Mckinstry, S. Datta, *IEEE J. Explor. Solid-State Computat. Devices Circuits* **2015**, *1*, 43.

[54]   T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, T. Someya, *Science* **2009**, *326*, 1516.

[55]   S. T. Han, Y. Zhou, C. Wang, L. He, W. Zhang, V. A. L. Roy, *Adv. Mater.* **2013**, *25*, 872.

[56]   M. Kaltenbrunner, P. Stadler, R. Schwödiauer, A. W. Hassel, N. S. Sariciftci, S. Bauer, *Adv. Mater.* **2011**, *23*, 4892.

[57]   F. Alibart, S. Pleutin, D. Guérin, C. Novembre, S. Lenfant, K. Lmimouni, C. Gamrat, D. Vuillaume, *Adv. Funct. Mat*. **2010**, *20*, 330.

[58]   P. Balakrishna Pillai, M. M. De Souza, *ACS Appl. Mater. Interfaces* **2017**, 9, 1609.

[59]   W. Xu, S. Y. Min, H. Hwang, T. W. Lee, *Sci. Adv.* **2016**, *2*, e1501326.

[60]   L. Q. Zhu, C. J. Wan, L. Q. Guo, Y. Shi, Q. Wan, *Nat. Commun.* **2014**, *5*, 3158.

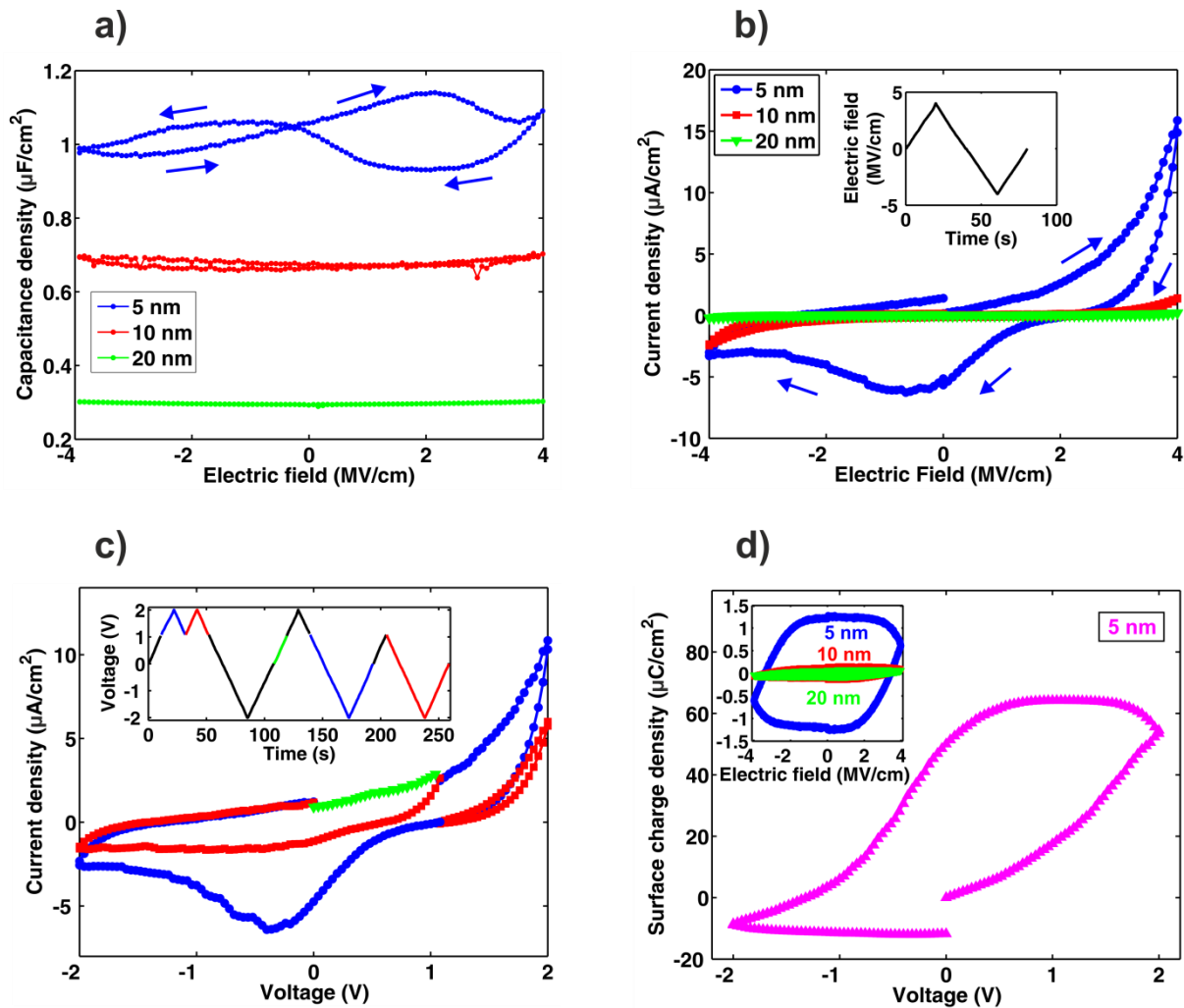[61]   J. Zhou, C. Wan, L. Zhu, Y. Shi, Q. Wan, *IEEE Electron Device Lett.* **2013**, *34*, 1433.

Figure 1. Device cross-section. a) Schematic device stack indicating tunneling and charge generation within the 5 nm thick Al_2O_3 layer. b) HAADF-TEM image of the fabricated layer stack with an EDX line scan (red arrow) through the cross section.

Figure 2. Electrical characterization of the Ti/Au/Ti-Al$_2$O$_3$-Cu stack. a) Small-signal capacitance measurement for different Al$_2$O$_3$ thicknesses at a frequency of 10 Hz. b) Current density-voltage measurement for different Al$_2$O$_3$ thicknesses (inset: conventional triangular voltage sweep). c) Customized current density-voltage measurement of 5 nm thick Al$_2$O$_3$ .The trap charging and discharging components of the current density are extracted by calculating the difference between the blue and the red current densities. The inset shows the customized voltage sweep. d) Surface charge density extracted from the customized current density-voltage measurement, where the computed trap charging/discharging current is integrated over the sweep time. The inset shows the surface charge density acquired with a build-in protocol of an LC 2 ferroelectric tester at a sweep time of 1 s.
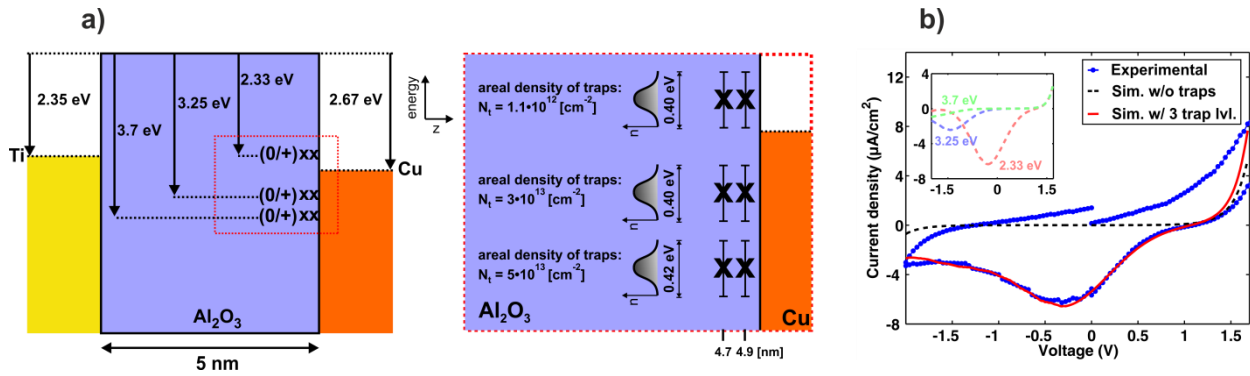
Figure 3. Investigation of the device physics by quantum-mechanical simulations: a) Assumed band configuration and simulation parameters including three trap levels close to the Cu anode. b) Comparison of fitted and experimental current density. The inset separately displays the current density components for each trap level.
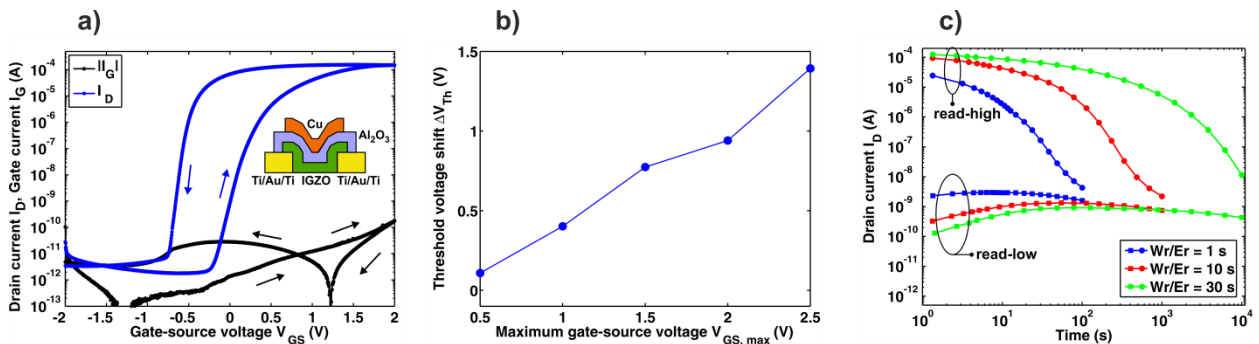

Figure 4. InGaZnO$_4$ (IGZO) thin-film transistor with 5 nm thick Al$_2$O$_3$ gate dielectric at a drain source-voltage V$_{DS}$ = 100 mV. a) Drain current I$_D$ and gate current I$_G$ as a function of gate-source voltage V$_{GS}$. The counter-clockwise hysteresis of I$_D$ indicates positive trap charges. b) Threshold voltage shift ΔV$_{Th}$ for different maximum gate-source voltages V$_{GS, max}$. c) I$_D$ retention measurement for different write (Wr) and erase (Er) times. The read-out is performed at V$_{GS}$ = 0 V and a V$_{DS}$ = 100 mV.
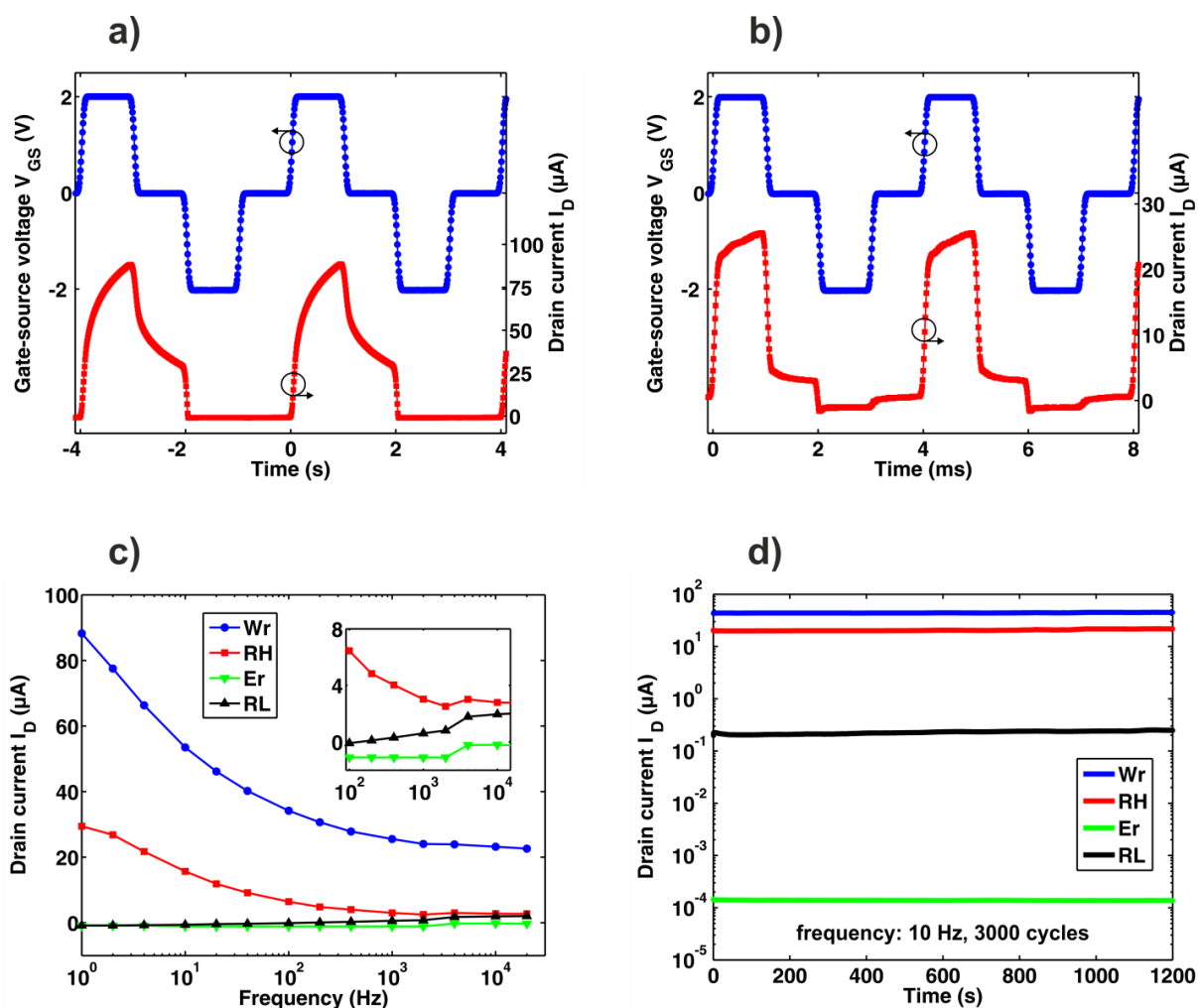
Figure 5. AC characterization of an InGaZnO$_4$ (IGZO) thin-film transistor (TFT) with a 5 nm thick Al$_2$O$_3$ gate dielectric at a drain source-voltage V$_{DS}$ = 100 mV. a) Drain current I$_D$ response at a write (Wr)/ erase (Er) modulation of 1 Hz. b) I$_D$ response at a Wr/Er modulation of 1 kHz. c) Frequency dispersion of I$_D$ for Wr, read-high (RH), Er and read-low (RL). The inset provides a magnification of the RH and RL region above 100 Hz. d) Cycling stability of Wr, Er, RH and RL.
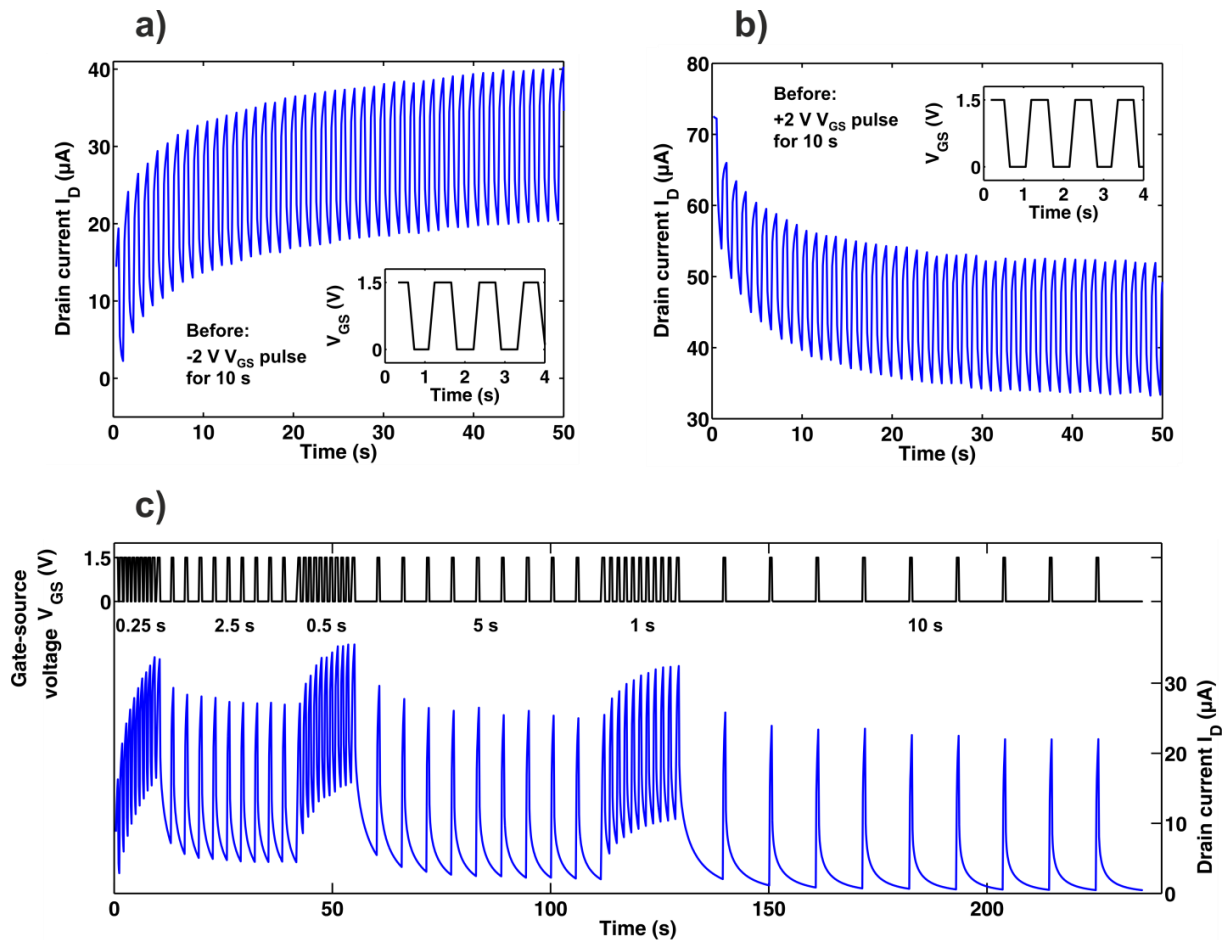
Figure 6. Synaptic response of an InGaZnO$_4$ (IGZO) thin-film transistor (TFT) with 5 nm thick Al$_2$O$_3$ gate dielectric at a drain source-voltage V$_{DS}$ = 100 mV. The drain current I$_D$ and the gate-source voltage V$_{GS}$ represent the synaptic signal transmission and the modulation of the synaptic weight, respectively. a) Facilitating synaptic behavior after a negative V$_{GS}$ pulse showing increasing synaptic signal. The inset displays the corresponding V$_{GS}$ excitation. b) Depressing synaptic behavior after a positive V$_{GS}$ pulse showing decreasing synaptic signal. The inset displays the corresponding V$_{GS}$ excitation. c) Dependence on the duty cycle of the pulsed excitation. The denoted time indicates the time period where the gate-source voltage V$_{GS}$ = 0 V, which follows after each positive V$_{GS}$ pulse (1.5 V, 0.5 s).