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Wafer-Scale Synthesis of Graphene on Sapphire: Toward Fab-Compatible Graphene

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The adoption of graphene in electronics, optoelectronics, and photonics is hindered by the difficulty in obtaining high-quality material on technologically relevant substrates, over wafer-scale sizes, and with metal contamination levels compatible with industrial requirements. To date, the direct growth of graphene on insulating substrates has proved to be challenging, usually requiring metal-catalysts or yielding defective graphene. In this work, a metal-free approach implemented in commercially available reactors to obtain high-quality monolayer graphene on c-plane sapphire substrates via chemical vapor deposition is demonstrated. Low energy electron diffraction, low energy electron microscopy, and scanning tunneling microscopy measurements identify the Al-rich reconstruction $\left(\sqrt{31}\times\sqrt{31}\right)R\pm 9°$ of sapphire to be crucial for obtaining epitaxial graphene. Raman spectroscopy and electrical transport measurements reveal high-quality graphene with mobilities consistently above 2000 $cm^2\ V^{-1}\ s^{-1}$. The process is scaled up to 4 and 6 in. wafers sizes and metal contamination levels are retrieved to be within the limits for back-end-of-line integration. The growth process introduced here establishes a method for the synthesis of wafer-scale graphene films on a technologically viable basis.

The route for the implementation of graphene in the electronic/optoelectronic-technology market relies on the existence of a synthesis method that yields graphene films over wafer-scale, with good crystallinity and with contamination levels compatible with large-scale back-end-of-line (BEOL) integration. At present, chemical vapor deposition (CVD) on catalytic copper (Cu) substrates is widely recognized as the most promising route to obtain scalable monolayer graphene for electronic and optoelectronic applications.[1–4] However, significant hurdles are limiting the actual integration of CVD graphene grown on Cu for most applications. In the first instance, the unavoidable transfer process over wafer-scale is rather cumbersome and introduces contamination, unintentional doping, and mechanical stress,[5–7] which adversely impact the physical integrity and electrical performance[8] of the graphene layer. The significant challenge involved in carrying out this seemingly straightforward task is reflected by the vast literature on large-scale transfer processes. Second, metallic contamination levels in transferred CVD graphene grown on Cu are typically well-above the specifications requested for BEOL integration.[6] Clearly, as

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graphene moves closer toward applications, contamination will become an increasingly serious roadblock, unless addressed.

A way to overcome the above hurdles would be to directly synthesize graphene onto the target substrate, such as epitaxial graphene on silicon carbide (SiC).[9,10] There, high growth temperatures provide a sufficient amount of energy to sublimate silicon from the substrate, while the remaining carbon rearranges on the surface in the form of graphene. However, the very high cost of the substrate and of the process itself, together with its marginal and niche application range in consumer electronics make it something of a cul-de-sac as a route for commercialization.

The successful synthesis of monolayer high-quality graphene on sapphire would instead be readily implemented into what is already a very mature device-processing technology as well as into the vast market pushing it. Indeed, sapphire has recently become ubiquitous as a substrate for light-emitting diodes,[11–13] and is being adopted in microelectronics with relevance in high frequency and data communication.[13] Also, synthesis of graphene on sapphire would provide an alternative route to obtain metal-free graphene that could be transferred onto final target substrates, something that to date has not been achieved at wafer scale for epitaxial graphene on SiC due to the very strong epitaxial interaction with the growth substrate. To date, several works have reported attempts to synthesize graphene directly onto insulating substrates, mostly silicon and sapphire.[7,14–23] Most of them use metal catalysts sacrificially deposited on the substrate[7,16,20–22] or in the vapor phase[18] to aid the growth, which does not resolve the metallic contamination issue. Only few works have reported the metal-free synthesis of graphene on sapphire, obtaining high-quality graphene over small areas at growth temperatures higher than 1500 °C.[14,15] Scaling up high-quality metal-free graphene on sapphire has proved to be challenging, with best reported mobilities for 2 in. graphene wafers of about 370 $cm^2\ V^{-1}\ s^{-1}$.[17] Also, no work has identified to date the sapphire surface reconstruction upon graphene growth, a crucial aspect in identifying and clarifying favorable growth mechanisms. Ultimately, to date, no work has identified a clear path to obtain wafer-scale metal-free graphene on sapphire with mobilities comparable to those obtained for graphene grown on Cu. Here, we demonstrate and scale up to 4 and 6 in. wafers a CVD metal-free approach for growing graphene directly on sapphire substrates that yields films with mobilities above 2000 $cm^2\ V^{-1}\ s^{-1}$ and contamination levels compatible with BEOL integration. We show that wafer-scale graphene films grown on sapphire can be transferred with a metal-free approach while maintaining the original (as-grown) carrier mobilities. Furthermore, we perform an in-depth investigation of the graphene/sapphire interface via low-energy electron diffraction (LEED) and scanning tunneling microscopy (STM), which allows us to identify the path for high-quality epitaxial growth.

Two different approaches for graphene synthesis were adopted and compared as shown in the schematic diagram reported in **Figure 1**a. In one case, graphene was grown directly

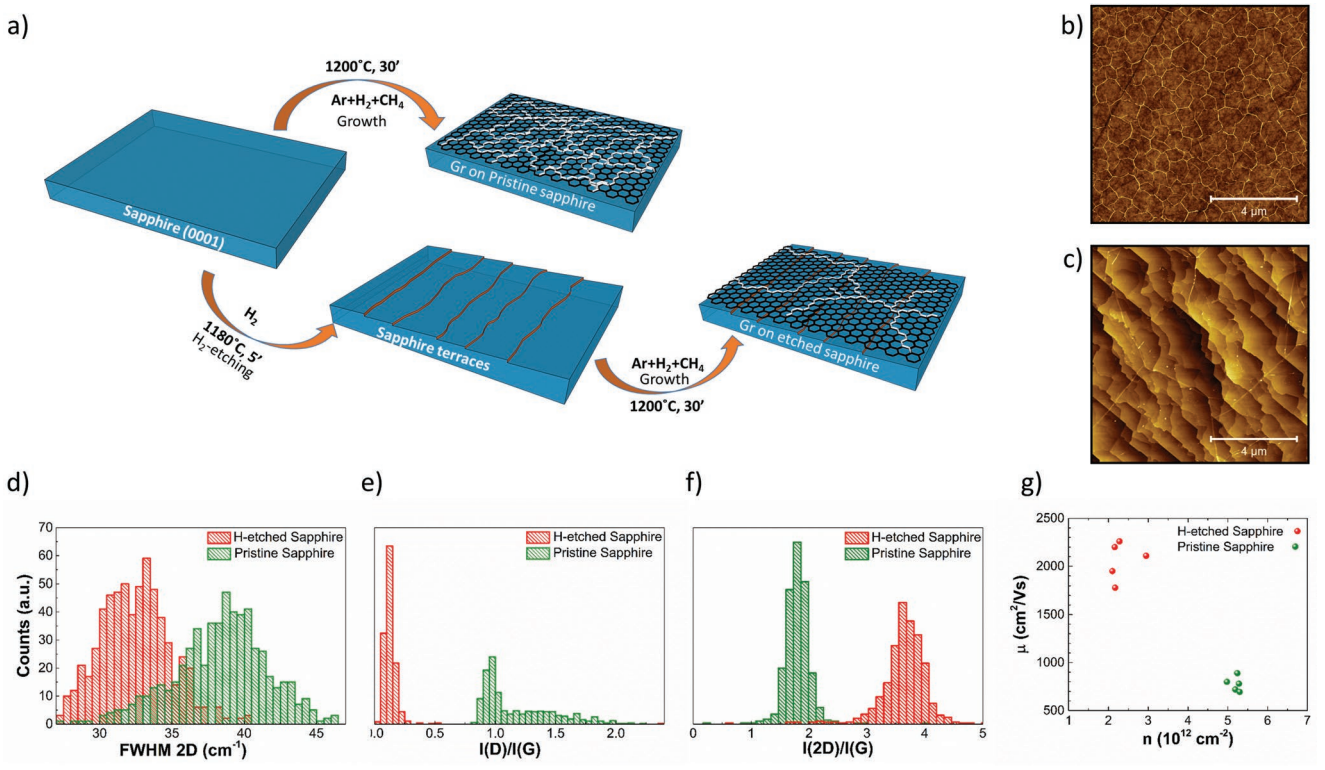

Figure 1. a) Schematic sketch depicting the processing steps for the two different approaches for obtaining graphene: growth on pristine and H_2-etched sapphire. b,c) Representative 10 × 10 μm AFM micrographs of graphene grown on b) pristine and c) H_2-etched sapphire, respectively. d–f) Representative histograms obtained from 25 × 25 μm^2 Raman maps of graphene on pristine and H_2-etched sapphire showing the d) FWHM of the 2D peak, e) the D/G intensity ratio, and f) the 2D/G intensity ratio. g) Mobility versus carrier density plot for graphene Hall bars fabricated on pristine and H_2-etched sapphire.

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on sapphire without preparing the surface (pristine), while in the other one the sapphire surface was hydrogen-etched (H_2-etched) before graphene deposition. In both cases, c-plane Al_2O_3 (0001) dies were introduced in a high temperature cold-wall research reactor (AIXTRON BM Pro HT) and graphene was grown at 1200 °C, 25 mbar, in a mixture of 20:2:0.1 Ar:H_2:CH_4 for 30 min. In the H_2-etched approach, an additional step was performed prior to graphene growth, where the sapphire samples were etched in the same reactor at 1180 °C, 750 mbar, in H_2 atmosphere for 5 min. More detailed information about the growth and etching processes can be found in the Experimental Section. Raman spectroscopy, atomic force microscopy (AFM), and electrical measurements were performed to investigate the quality of the graphene grown with the two different approaches (Figure 1b–g). The topographical difference between the graphene grown on pristine and H_2-etched sapphire is remarkable, as visible in the AFM micrographs reported in Figure 1b,c, respectively. The graphene film grown on pristine sapphire shows a high density of ridges (see panel (b)), similar to those measured on graphene on SiC (000-1).[24] Such ridges form as a consequence of the different thermal expansion coefficients of graphene and sapphire, as also observed in other works,[14,15,17] and have a height of around 1–4 nm (Figure S1a, Supporting Information). In addition, scratches originating from the substrate polishing process are also visible, even after graphene growth. In contrast, the graphene grown on H_2-etched sapphire exhibits a significantly reduced density of ridges. Also, well-defined atomic steps with heights that are integer multiples of the single unit cell height (i.e., 1.3 nm) become visible (panel (c) and Figure S1b, Supporting Information). Hence, similarly to SiC,[25] optimized H_2-etching reveals atomic terraces on sapphire. Histograms obtained from representative Raman maps acquired over areas of 25 × 25 μm^2 are reported in panels (d)–(g) and consistently indicate a significant improvement of the crystalline quality of graphene on H_2-etched sapphire (see also Figure S2, Supporting Information). Each Raman histogram is fitted with a Gaussian curve to extract the distribution maximum and the half-width-at-half-maximum, the latter employed as uncertainty. Figure 1d shows that the full-width-at-half-maximum (FWHM) of the 2D mode of graphene decreases from 38.44 (±3.17) to 32.32 (±2.22) cm^{-1} for graphene grown on pristine and H_2-etched sapphire, respectively, indicating an improvement in graphene crystalline quality and less strain fluctuation across the samples.[26] Notably, the average 2D FWHM measured on H_2-etched sapphire is the lowest reported to date for as-grown graphene on sapphire. In pristine samples, the D/G intensity ratio, indicative of the defect concentration in graphene, presents a bimodal distribution with the main peak at 0.94 and a broader peak at 1.4, suggesting the presence of highly defective areas across the sample. Upon H_2-etching of the substrate, the D/G distribution peaks at a much-reduced value of 0.13 (±0.04) (Figure 1e), indicating a low defect density. The 2D/G intensity ratio distributions peak at 1.80 (±0.17) and 3.67 (±0.27) for graphene on pristine and H_2-etched sapphire, respectively (**Figure 2**f). These values indicate a lower charge carrier concentration for graphene on the H_2-etched sapphire sample, which we estimate[27] being in the lower 10^{12} cm^{-2} range, compared to graphene grown on pristine sapphire, which is estimated to be around 5 × 10^{12} cm^{-2}. These estimates are confirmed by Hall effect measurements at room temperature. The highest carrier mobility measured for graphene on H_2-etched sapphire is 2260 cm^2 V^{-1} s^{-1}, with a hole density of 2.3 × 10^{12} cm^{-2}. For graphene on pristine sapphire, the highest mobility is 890 cm^2 V^{-1} s^{-1}, with a hole density of 5.24 × 10^{12} cm^{-2}. In general, we observe that mobilities on H_2-etched substrates are at least a factor of 2.5 higher than on nontreated substrates grown in nominally identical conditions (see Supporting Information for further details). It is therefore clear that H_2-etching of sapphire is crucial to obtain high-quality graphene while growing at temperatures comparable to those conventionally used for metal-CVD processes.

In order to determine the structural properties at the graphene/sapphire interface and gain a better understanding of the growth mechanisms—something that to date has remained elusive—we performed LEED and STM measurements. First, LEED was carried out on pristine and etched sapphire surfaces. For pristine sapphire surfaces, as expected, no LEED pattern could be retrieved, due to the insulating nature of the sample. On the other hand, surprisingly, LEED on etched sapphire was measurable down to 60 eV and revealed a clear ($\sqrt{31}$ × $\sqrt{31}$)R9° reconstruction (see Figure S4a, Supporting Information). The Al-rich nature of this reconstruction accounts for the direct visualization of the LEED pattern. Although there

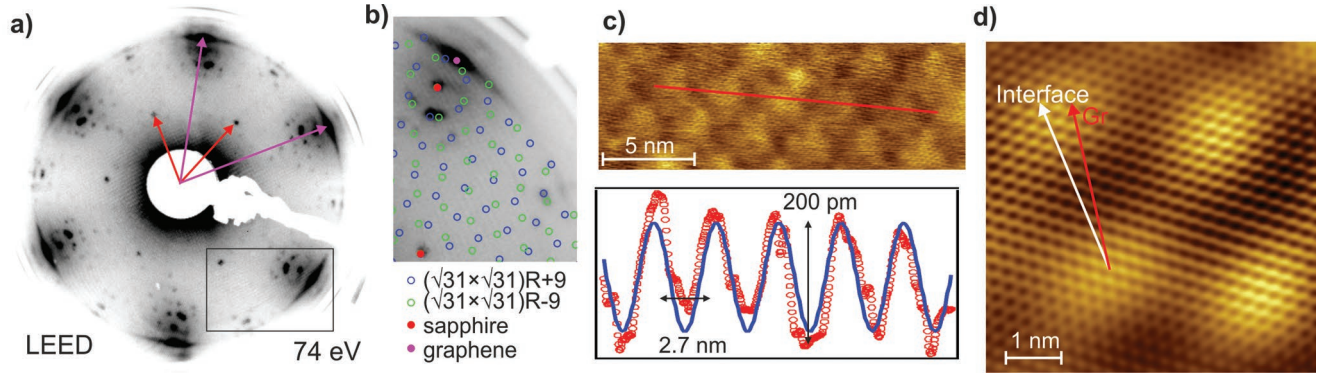

Figure 2. a) LEED pattern of graphene grown on H_2-etched sapphire, measured at 74 eV. b) Zoom of the inset in panel (a), showing the sapphire reconstruction superimposed with the theoretical diffraction spots. c) STM image and a line profile (along the red solid line) of a portion of graphene over the ($\sqrt{31}$ × $\sqrt{31}$)R±9°. d) FFT-filtered STM image from a portion of (c).

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is a rather long history of controversy and debates concerning its actual atomic structure,[28–32] Lauritsen et al. bring a compelling argument in favor of an Al (111) layer on top of the Al-terminated c-plane of the substrate.[29] To date, this reconstruction has been observed only upon annealing in ultra-high vacuum (UHV) of Al_2O_3 (0001) at temperatures well-above 1200 °C,[28–31] resulting in a loss of surface oxygen. Our recipe can induce the $(\sqrt{31} \times \sqrt{31})$R9° reconstruction at lower temperatures and higher pressures than those reported in literature[28–31] as a result of the H_2-etching process, i.e., oxygen reduction is facilitated by hydrogen. Figure 2a reports the LEED pattern recorded after graphene synthesis on etched sapphire and, as visible in Figure 2b, all measured spot positions are perfectly explained by the expected presence of two rotational domains of the $(\sqrt{31} \times \sqrt{31})$R9° reconstruction (i.e., $(\sqrt{31} \times \sqrt{31})$R±9°). In Figure 2c, we show an atomically-resolved STM image of graphene over the $(\sqrt{31} \times \sqrt{31})$R±9° reconstruction. The complex pattern of the underlying reconstructed sapphire layer is recognizable as a periodic arrangement of irregularly rhombi-shaped domains. In the bottom inset of the panel, we show the line profile (red solid line on the image) indicating the spacing between the maxima to be (27 ± 1) Å, compatible with the nominal length of the reconstruction of 26.5 Å. A 2D-FFT (fast Fourier transform) filtered portion of the image in panel (c) is shown in panel (d) together with the directions of the graphene (red) and the reconstruction (white) primitive vectors. The mutual orientation between the two is 21°, corroborating the fact that graphene preferentially aligns along the R30 direction with respect to the Al_2O_3 (0001) (1 × 1), as also visible from the LEED pattern in panel (a). The structural model of the Al-rich reconstruction on sapphire is complicated by the fact that the lattice spacing between the Al atoms is not constant within the unit cell, but depends on the mutual arrangement of the Al atoms with respect to the substrate registry.[29] Although the current resolution of the STM measurements does not allow us to draw a conclusion on the atomic arrangement between the graphene and the Al atoms at the interface, we observe that the graphene lattice conforms well to the periodic corrugation imposed by the $(\sqrt{31} \times \sqrt{31})$R±9°. Thus, graphene growth on sapphire is apparently catalyzed by the highly reactive Al-rich surface of the reconstructed surface. During growth, the Al sites are strong Lewis acids that dissociate the methane molecules, thus catalyzing graphene growth.

To assess the size of the single-crystalline graphene domains, the sample was measured with low-energy electron microscopy (LEEM), which is a technique highly sensitive to the crystalline orientation.[33] In the LEEM micrograph shown in Figure S5 in the Supporting Information, three color contrasts (white, light gray, and dark gray) are visible. When performing LEED with micro-spot illumination (μLEED) on the white and light gray regions, only the $(\sqrt{31} \times \sqrt{31})$R9° pattern is recognizable, together with the R30 graphene reflections, thus indicating the same crystallographic phase (see Figure S6, Supporting Information). On the dark gray phase instead, multiple rotational domains are found, and no $(\sqrt{31} \times \sqrt{31})$R9° pattern is observed. From the dark-field analysis reported in the Supporting Information (see Figures S5 and S6, Supporting Information), we estimate the single-crystal grain size of graphene to have an average lateral size of more than 450 nm, with several grains extending more than a micrometer across, a value larger than what has been reported in the literature so far.[15,17] Hence, on the one hand, graphene grows with a high degree of crystallinity on the fully reconstructed sapphire surface and, on the other hand, the graphene single-crystal domain size is essentially limited by the grain size of the reconstructed domains on the Al_2O_3 (0001) surface. Therefore, the route for obtaining high-quality graphene on sapphire relies on the fine control of the Al-rich reconstructed sapphire surface.

To demonstrate the industrial viability of this method, the process is transferred onto a production-scale reactor (AIXTRON CCS 2D) and graphene growth on sapphire is demonstrated in 5 × 4 and 1 × 6 in. configuration. **Figure 3** shows

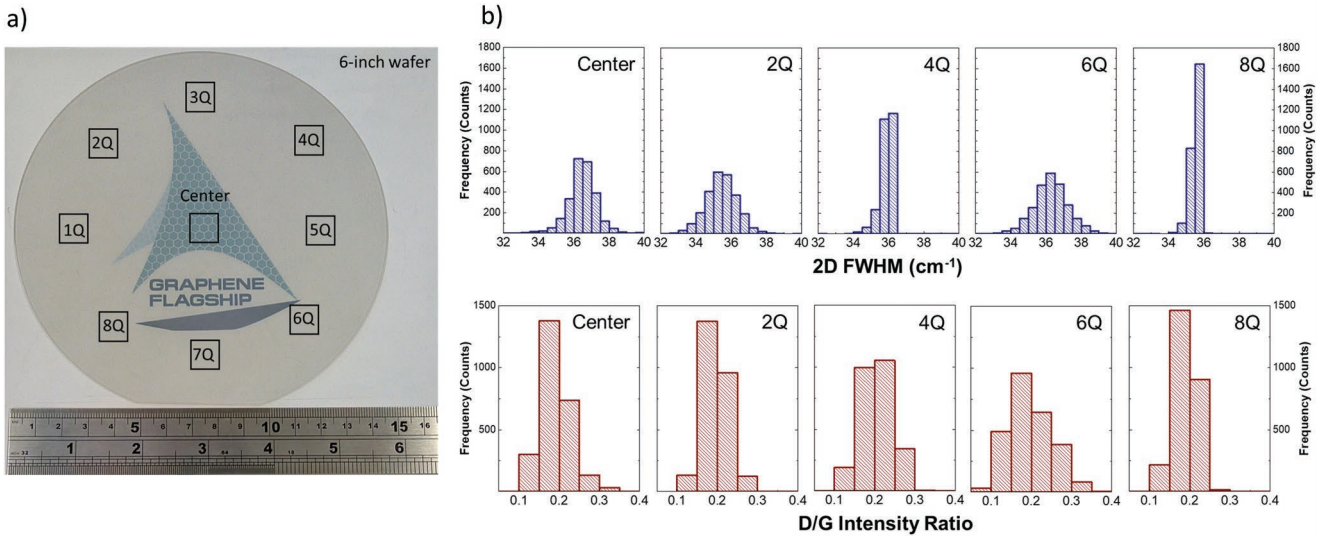

Figure 3. Characterization of graphene grown on 6 in. sapphire wafer. a) Optical image of the grown wafer, with squares indicating the approximate locations where Raman measurements were performed. The wafer looks highly transparent, with the "Graphene Flagship" logo behind remaining clearly visible. b) Raman analysis of graphene grown on a 6 in. sapphire wafer, measured at five different places.

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the results of the Raman analysis of graphene grown on a 6 in. sapphire wafer. The analysis is carried out on nine areas of 2×2 mm^2, as indicated by the squares superposed to the optical picture of the as-grown wafer in Figure 3a. Figure 3b shows the histograms of the FWHM of the graphene 2D Raman peak and of the ratio of the intensities of the D and G peaks for five selected areas (center and even-numbered quadrants). These Raman histograms are employed to benchmark the graphene crystalline quality on the different areas of the wafer, in terms of concentration of defects and strain-doping fluctuation. The comparison of the different histograms of the 2D FWHM demonstrates a high degree of homogeneity of the graphene film throughout the wafer. The average value of the 2D FWHM is 36 cm^{-1} for all the areas (slightly larger than what reported in Figure 1d, due to the upscaling process). Remarkably, the D/G peak intensity ratio average ranges from 0.15 ± 0.06 to 0.2 ± 0.12, demonstrating that even the defect concentration shows little variation across the wafer. The 2D/G peak intensity ratio average varies between 3.45 ± 0.30 and 3.83 ± 0.35 (see the Supporting Information), confirming that the synthesized material is monolayer. The complete histograms and the precise values of the 2D FWHM, D/G, and the 2D/G peak intensity ratios for the 6 and 4 in. wafers are reported in the Supporting Information. In all cases, the wafers processed at the same time showed the same quality and homogeneity, and the process repeatability was outstanding. In all the samples analyzed, the $(\sqrt{31} \times \sqrt{31})$R±9° reconstruction could be observed with LEED.

To measure the conductivity of the graphene on sapphire wafers, we performed terahertz time-domain spectroscopy (THz-TDS) measurements[34] (see the Experimental Section for additional information). **Figure 4**a shows the sheet conductivity map of an entire 4 in. wafer, and the average sheet conductivity value, retrieved by fitting the histogram in Figure 4b, is 0.91 ± 0.04 mS. To broaden the applicative range, graphene grown on sapphire wafers was successfully transferred to target substrates (in this case 90 nm SiO_2/Si) using the poly-vinyl acetate (PVA) lamination approach.[35] Figure 4c shows a 4 in. graphene film transferred onto SiO_2/Si, continuous over 97% of the area. Field effect transistors (FETs) were fabricated from graphene transferred on SiO_2/Si dies and measured in a back-gate geometry (Figure 4e). Figure 4d shows a typical measured device, consisting in a series of stripes of graphene with lateral size of 3.7 µm and lengths variable between 33 and 42 µm, contacted with 10/60 nm of Cr/Au contacts. A typical conductivity versus gate voltage curve is reported in Figure 4f: the neutrality point is around −5 V, indicating low doping of graphene ($n \approx 3 \times 10^{11}$ cm^{-2}). Mobility values are obtained from the slope of the linear fit of the conductivity versus gate voltage,[36] according to the formula; $\mu = \pm \frac{\sigma t}{\varepsilon \varepsilon_0 (V_g - V_D)}$ where t and ε are the thickness and the dielectric constant of SiO_2, respectively.

For the representative device shown in Figure 4d, we obtain $\mu_h = 2300$ cm^2 V^{-1} s^{-1} for holes and $\mu_e = 2000$ cm^2 V^{-1} s^{-1} for electrons, respectively (see also Figures S14–S16, Supporting Information). These values are comparable with what has

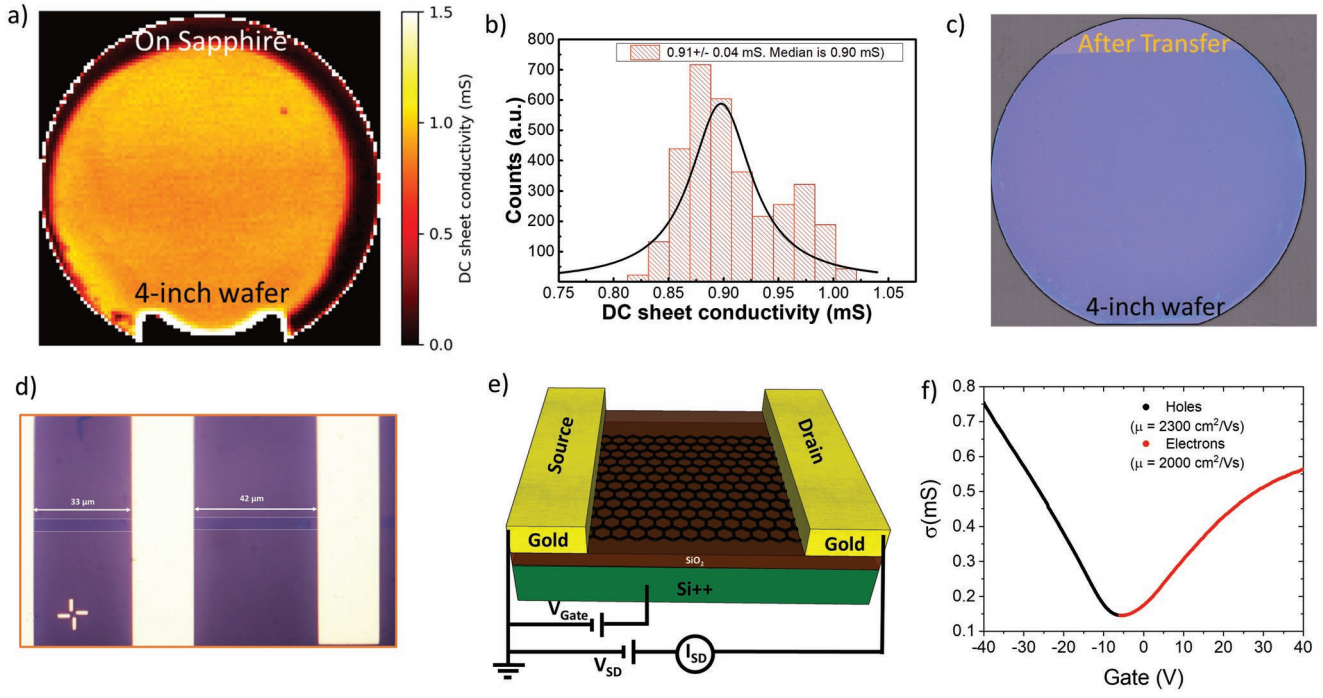

Figure 4. a) THz-TDS mapping of the sheet conductivity across the 4 in. wafer. b) Histogram of THz-TDS sheet conductivity measured of graphene on sapphire. c) Optical image of graphene transferred onto a 90 nm SiO_2/Si substrate by the PVA lamination method. d) Optical view of the fabricated devices for electrical characterization of graphene grown on sapphire and transferred to SiO_2/Si. The yellow stripes are the metal contacts and the darker horizontal areas are the two graphene stripes defined by EBL and RIE processing (marked up by white lines). e) Schematic diagram showing the FET device and the electrical setup. A highly doped silicon substrate, covered with 285 nm of dielectric oxide, is used as a backgate for the FET characterization. f) Two-probe conductivity σ as a function of the applied backgate voltage for electrons and holes (in red and black, respectively).

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been reported for CVD polycrystalline graphene grown on Cu foil and transferred onto SiO_2/Si.[37] However, in contrast to CVD graphene on Cu, these samples already fully satisfy the specifications for BEOL integration as confirmed by total reflection X-ray fluorescence (TXRF) measurements (see the Supporting Information), (even if manually handled under noncontrolled laboratory conditions). We are confident that even front-end-of-line requirements could be met with more stringent wafer preparation and handling under fab conditions, since there is no metal used for the growth or transfer processes in our method.

In conclusion, this work identifies a clear approach for obtaining graphene directly on the c-plane of Al_2O_3 (0001) substrates in commercially available CVD reactors. We show that no external catalyst needs to be added in the growth process to obtain high-quality graphene, if the sapphire surface is properly prepared. Indeed, sapphire preparation via H_2-etching is crucial to obtain an Al-rich ($\sqrt{31}$ x $\sqrt{31}$)R± 9° reconstructed surface, which catalyzes graphene growth at temperatures comparable to those conventionally used for metal-CVD processes (i.e., 1200 °C). We show for the first time that high-quality graphene can be grown on 4 and 6 in. sapphire wafers with quality and properties comparable to those obtained for graphene on Cu foil. The results show a high degree of uniformity and consistency, which is crucial for any industrial process. While we here demonstrate up to 6 in. wafer growth, there is no indication that commercially available 12 in. sapphire substrates should not produce similar results. The clear advantage of this approach is the compatibility with fab contamination specifications, as shown by TXRF measurements, and the straightforward use of readily available sapphire wafer substrates (in contrast to metal foils, or thin films on wafer, or SiC). Furthermore, we demonstrate that large wafer areas of graphene can be transferred to any target substrate with a polymeric lamination approach, and that the obtained carrier mobilities are about 2000 $cm^2\ V^{-1}\ s^{-1}$. LEEM measurements indicate that the synthesized graphene is polycrystalline, with a preferential orientation of 30° with respect to the Al_2O_3 (0001) substrate and with grain sizes approaching one micrometer. Having observed to what extent graphene is affected by the ordering and composition of the interface, we suggest that a fine control over the homogeneity and domain size of the reconstructed sapphire surface should enhance the quality as well as the domain size of the grown graphene even further, thereby increasing its electrical mobility. This work demonstrates a viable route for the production of metal-free wafer-scale high-quality graphene directly onto insulating substrates, with a significant potential impact on a wide number of microelectronic, optoelectronic, and photonic applications.

Experimental Section

Growth of Graphene on Sapphire: c-axis, HEMCOR single crystal, double side polished sapphire (0001) substrates supplied by Alfa Aesar (Germany) were used. Before growth, sapphire substrates were cleaned with acetone, isopropanol, and deionized (DI) water in an ultra-sonicator bath, immersed in piranha solution (1:3, H_2O_2:H_2SO_4) for 15 min, and finally washed in DI water and N_2-blow-dried. The H_2-etching was performed in the growth reactor at 1180 °C for 5 min in an atmosphere of H_2.[38] Samples were then extracted and characterized. Graphene growth for both H_2-etched and pristine sapphire was performed as follows: i) the substrate was annealed at 1200 °C for 10 min in an atmosphere of 1000 sccm of Ar at 25 mbar; ii) growth was performed by introducing 100 sccm H_2 and 5 sccm of CH_4 while flowing 1000 sccm of Ar for 30 min at 25 mbar; iii) cooling was carried out under Ar flux.

Transfer of Graphene Grown on Sapphire: See the Supplementary Video (Supporting Information).

Characterization: Raman measurements were performed with a Renishaw Invia system with a 532 nm laser, a spot size of ≈1 µm, and at 5 mW of laser power. AFM was carried out with an AFM+ (Bruker Dimension Icon) operated in tapping mode in air and the Gwyddion software package was used to analyze the micrographs. LEED measurements were performed at room temperature with a SPECS GmbH LEED optics. STM and scanning tunneling spectroscopy measurements were carried out in an Omicron LT-STM at a base pressure of 10^{-10} mbar. LEEM measurements were done using an Elmitec LEEM III microscope with energy filter operated at an electron energy of 15 keV and a base pressure of 10^{-10} mbar. In µLEED, the incident electron beam was limited to an area of about 250 nm in diameter.

The electrical transport measurements on the transferred graphene were performed in a home-made probing station on an optical table to minimize vibrations. The gate and drain voltages were provided by a couple of Keithley 2450, used also to measure the source-drain current and the eventual presence of leak current between the gate and the drain. The device was contacted using tungsten tips of 25 µm radius, aligned using 3 MPI MP-40 micropositioner. FETs were defined by electron beam lithography (EBL) and reactive ion etching (RIE) techniques. All the electrical characterizations were performed in air at room temperature, in a 2-probe configuration applying a DC bias between source and drain of 10 mV. Before measuring, the samples were annealed in UHV at 230 °C for 2 h.

THz-TDS of as-grown graphene on sapphire was conducted in transmission mode using a commercial Picometrix T-Ray 4000 system with a THz spot size of ≈350 µm at 1 THz.[39] Samples were raster scanned with 1 mm step size in the focal plane between the THz transmitter and receiver. Examples of THz time-domain waveforms are shown in Figure S10a in the Supporting Information. The waveforms contained transients from internal reflections within the sapphire substrate. Here, the data from the directly transmitted transients were used to extract the sheet conductivity ($\sigma_s\ (\omega) = \sigma_1 + i\sigma_2$) of graphene as[39–41]

$$\sigma_s(\omega) = \left(\frac{n_{sap}+1}{Z_0}\right) \times \left(\frac{1}{T_{film}(\omega)} - 1\right) \quad (1)$$

where Z_0 is the vacuum impedance, T_{meas} is the ratio of the Fourier transforms of the THz waveforms transmitted through graphene-covered sapphire and bare sapphire (Figure S10b, Supporting Information), and n_{sap} is the refractive index of sapphire (Figure S10c, Supporting Information) calculated from THz waveforms from bare sapphire relative to air.[42]

Examples of sheet conductivity spectra from as-grown graphene on sapphire are shown in Figure S10d in the Supporting Information. The sheet conductivity spectra did not follow the classical Drude-model as previously observed[40,41,43] as a reduction was noticed in the sheet conductivity at low frequencies—this indicated that the carriers in graphene did not scatter isotropically but experienced some degree of carrier localization.[39,41,44] In such cases, the sheet conductivity was better described by the first term of the phenomenological Drude–Smith model[39,41,45]

$$\sigma_s(\omega) = \frac{W_D}{(1 - i\omega\tau)}\left(1 + \frac{c}{(1 - i\omega\tau)}\right) \quad (2)$$

where W_D is the Drude weight related to the DC sheet conductivity as $\sigma_{DC} = W_D\ (1 + c)$, and c is a parameter that can take values from −1 to 0 and describes the degree of carrier localization/backscattering.[39,41] If $c = 0$, the carrier momentum is totally randomized (classical Drude model), while carriers are completely backscattered in the case $c = -1$.[44] Fits to the Drude–Smith model and the extracted parameters for σ_{DC},

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τ, and c are shown together with the sheet conductivity spectra in Figure S10d in the Supporting Information.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

graphene on insulator, interface, metal free, sapphire, wafer scale

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