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# Time-domain Analysis of Chalcogenide Threshold Switching: from ns to ps scale

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## 2 ABSTRACT

3 A space- and time-dependent theoretical model based on a trap-assisted, charge-transport  
4 framework for the amorphous phase of a chalcogenide material is used here to interpret  
5 available experimental results for the electric current of nanoscale devices in the ns–ps time  
6 domain. A numerical solution of the constitutive equations of the model for a time-dependent  
7 bias has been carried out for GST-225 devices. The “intrinsic” rise time of the device current  
8 after the application of a suitable external bias is controlled by the microscopic relaxation of the  
9 mobile-carrier population to the steady-state value. Furthermore, the analysis is extended to  
10 include the effect of the external circuit on the electrical switching. A quantitative estimate of the  
11 current delay time due to unavoidable parasitic effects is made for the optimised electrical set  
12 up configurations recently used by experimental groups.

13 **Keywords:** Chalcogenides, GST, Ovonic threshold switching, Phase change memories, Charge transport, Amorphous materials

## 1 INTRODUCTION

14 Chalcogenide-based Phase Change Memories (PCM) have been studied for many years as a possible  
15 replacement for Flash memories, and in the late 2000’s eventually hit the market as storage elements for  
16 cell phones (Servalli, 2009). Furthermore, being two-terminal devices, they were easily integrated in 3D  
17 cross-point memory arrays (Optane, 2017a,b; Choe, 2017), paving the way for storage-class memories  
18 thanks to their fast access time and moderate cost per bit.

19 After a suitable tailoring of the chalcogenide-alloy composition, to match the specs dictated by a specific  
20 use, embedded PCM have the potential to become key enablers of technological breakthroughs in a  
21 number of industrial applications; among these, automotive applications (Arnaud et al., 2018). In recent  
22 years, PCM devices were also profitably employed in “non von Neumann” neuromorphic computing  
23 architectures, exhibiting a better performing collocation of memory and processing (Markram et al., 2011;  
24 Le Gallo et al., 2018; Sebastian et al., 2020; Sarwat et al., 2021).

25 Whatever application for PCM devices is envisaged, their working principle relies on the fast and  
26 reversible structural change of a chalcogenide alloy that switches between the amorphous (*reset*) and  
27 crystalline (*set*) states, upon the application of an electric pulse (Lai, 2003; Raoux and Wuttig, 2009;

28 Kolobov and Tominaga, 2012; Redaelli, 2019). The bottleneck of a fast electrical switching is inherent in  
29 the crystallization process, starting from the high-resistance amorphous phase (Anbarasu et al., 2012). In  
30 many cases, a voltage pulse of suitable intensity, and width of a few ns is required to surpass, first, an  
31 Ovonic Threshold Switching (OTS) event, namely an off-to-on threshold switching in the amorphous state,  
32 precursor of the amorphous-to-crystalline phase change. A useful parameter that has been introduced to  
33 quantify the transition speed is the so-called delay time  $t_d$ , defined as the time interval between the instant  
34 at which the applied voltage exceeds the threshold value and the instant at which a steep rise in the  
35 device current begins (Wimmer and Salinga, 2014; Shukla et al., 2016). Despite efforts to decrease  $t_d$   
36 with different strategies, so far it has been difficult to obtain values below 1 ns (Wimmer and Salinga,  
37 2014). Thus, achieving sub ns threshold-switching times for nanoscale devices is a goal of both scientific  
38 and technological relevance (Wimmer and Salinga, 2014; Saxena et al., 2021).

39 The exploitation of the electrical threshold switching property of many chalcogenide-based devices,  
40 for designing phase-change memory devices with access speed comparable to the SRAM, pushed  
41 experimentalists to design extremely performing and accurate measuring setups (Shukla et al., 2017). The  
42 latter must be able to respond to very fast external electric pulses, in order to precisely record the onset of  
43 the threshold switching and the change of the current value from the low value of the amorphous off state  
44 to the high value of the amorphous on state. A major attempt to provide new experimental insights into  
45 the threshold-switching mechanism by means of a precise knowledge of the exact shape of the voltage  
46 applied to the chalcogenide cell has been carried out by Salinga and coworkers (Wimmer and Salinga,  
47 2014). According to the Authors, in the reported experiments on GST-225 devices, due to the careful  
48 impedance matching of the contact board the applied voltage pulses reach the memory cell without any  
49 significant distortion. Measurements were performed where the applied voltage signal, aimed at producing  
50 the threshold voltage, ramps up linearly from zero to a maximum value; the leading edge of the voltage  
51 ranges from few ns to 104 ns. The value at which threshold switching appears depends upon the steepness  
52 of the ramp; in particular, short rise times of the latter lead to high switching voltages, whereas the  
53 application of slow ramps produces a decrease in the switching voltage. Thus, the pulse shape strongly  
54 influences the switching voltage, so that the concept of a unique voltage at which the resistance of the cell  
55 falls becomes questionable (Wimmer and Salinga, 2014; Shukla et al., 2016).

56 This concept is pushed even further in a recent paper by Saxena and coworkers (Saxena et al., 2021),  
57 where it is shown that delay times in the ps scale can be obtained in GST-225 cells by means of an  
58 appropriate design of both the experimental apparatus and the external voltage applied to the cell. In  
59 particular, the Authors measured delay times shorter than 50 ps for a voltage equal to twice the threshold  
60 voltage measured in static conditions for the same material, proving that PCM memory devices can  
61 reach SRAM-like speeds. Besides the technological implications of the above-mentioned performances,  
62 experimental measurements of Ovonic threshold switching in the time domain provide new interpretation  
63 challenges to test the existing theories about the switching mechanism; such theories have been  
64 formulated mainly by Academia over the last five decades in parallel with the technological developments.  
65 While, in the low-resistance state, the standard description of conduction in semiconductors applies,  
66 the electric properties of the high-resistance state are explained as a hot-carrier effect (Ielmini, 2008;  
67 Cappelli et al., 2013; Buscemi et al., 2014a; Brunetti et al., 2020), or a combination of electro-thermal  
68 effects (Bogoslovskij and Tsendin, 2011; Le Gallo et al., 2016). Experiments where the parasitic effects  
69 have been reduced as much as possible confirm the relevance of hot-carrier phenomena on OTS, even  
70 though the high thermal efficiency and the fast thermal dynamics in nanoscale devices suggest that the  
71 heat flow dynamics can indeed play a role (Le Gallo et al., 2016).

72 As for the OTS effect in the amorphous phase, structural analyses and Molecular-Dynamics simulations  
73 of amorphous chalcogenides confirm the existence of a number of trap states located around mid gap,  
74 that play a fundamental role on the onset of the electrical switch (Kolobov and Tominaga, 2012; Redaelli,  
75 2019). At low fields (below threshold) the majority of carriers are trapped and the conduction is very low;  
76 when the field is strong enough to heat the carriers, the population of the high-energy, high-mobility states  
77 is enhanced. This, in turn, increases the energy gain of the trapped carriers at the expense of the field,  
78 further enriching the population of the trap states close to the conduction-band edge (and, possibly, also  
79 band states (Brunetti et al., 2020)): in this way a positive feedback is established which, eventually, makes  
80 the current to increase by several orders of magnitude.

81 In this paper we apply a space- and time-dependent theoretical model based on a trap-assisted charge  
82 transport in the amorphous phase of a chalcogenide material (Piccinini et al., 2016; Jacoboni et al., 2017),  
83 to interpret the available experimental results in the ns–ps time domain for the electric current of nanoscale  
84 devices, based on the GST-225 chalcogenide, in a variety of bias conditions. A numerical solution of the  
85 constitutive equations of the model for a time-dependent bias makes it possible to test to what extent  
86 the threshold voltage depends upon the microscopic characteristic times that regulate the field-to-carrier  
87 energy transfer; this transfer is in fact responsible for the carrier heating which, in turn, produces the  
88 threshold switching. Furthermore, the analysis is extended to include the effect of the external circuit on  
89 the electrical switching, with reference to the optimised electrical set up configurations recently used by  
90 experimental groups (Saxena et al., 2021).

91 Sect. 2 summarizes the main features of the theoretical approach; the set of equations which constitute  
92 the model for the OTS device, and the numerical algorithm implemented for solving them, are described  
93 in Sects. 2.1–2.3, while Sect. 2.4 illustrates how we modeled the OTS device coupling with an external  
94 circuit that represents the measuring equipment. Dynamic and static models for the OTS device have been  
95 tested in view of their possible implementation into a device simulation framework. Section 3 contains  
96 our results and their critical analysis: first, parasitic effects are neglected; the ideal cases of a voltage  
97 step (Sect. 3.1) and of voltage trapezoidal profiles, similar to those reported in (Saxena et al., 2021), are  
98 considered with the purpose of evaluating the delay time of the OTS device (Sect. 3.2); then, the more  
99 realistic condition of a voltage trapezoidal profile applied to a device in presence of parasitic effects is  
100 studied (Sect. 3.3). Finally, Sect. 4 summarises the main achievements of the analysis, and provides some  
101 comments about possible developments of the present approach.

## 2 THEORETICAL APPROACH

102 The analysis aims at interpreting the experimental current-voltage curves obtained by applying time-  
103 dependent voltages with a time scale ranging from the nanoseconds to the picoseconds. Based on a  
104 thorough study of the Ovonic threshold switching by the Authors of the present paper and others (Ielmini,  
105 2008; Piccinini et al., 2016; Jacoboni et al., 2017), the theoretical approach assumes that, when the  
106 chalcogenide material is in the amorphous phase, carrier heating due to energy transfer from the external  
107 field dominates over thermal effects in determining the OTS. Accordingly, the heat equation for the lattice  
108 is not included in the model. Carriers, here assumed to be electrons, can occupy two trap levels with  
109 energy values  $E_T = 0$  and  $E_B = \Delta$ , with density of states  $g_T$  and  $g_B$ , respectively. Carriers in level  $E_T$  are  
110 trapped, i.e., have zero mobility and, therefore, do not contribute to the current; carriers in level  $E_B$  mimic  
111 conduction electrons, even though they have a unique well-defined energy, and contribute to the current  
112 with a constant mobility  $\mu$ . The use of a single energy level for the mobile states is in fact a simplification

113 of the model; however, a sensible description of the physics is anyway achieved (Piccinini et al., 2016).  
 114 The introduction of a dispersion relation of the mobile states improves the quantitative description of the  
 115 electric switching at and above threshold, without altering the key features of the present implementation  
 116 (Brunetti et al., 2020).

117 The device dynamics is assumed to be one-dimensional: the cross section of the sample is supposed large  
 118 enough to neglect the effects of the lateral boundaries. Thus, the physical quantities of interest along the  
 119 device are functions only of the longitudinal coordinate  $x$  and of time  $t$ ; they are the electric field  $F$ , the  
 120 total concentration of carriers  $n$ , the concentration of mobile carriers  $n_B$ , the concentration of carriers in  
 121 the trap states  $n_T$ , and the particle current density  $j$ . The above quantities are not all independent from  
 122 each other; in fact,

$$j = n_B \mu F - D_B \frac{\partial n_B}{\partial x}, \quad n = n_T + n_B, \quad (1)$$

123 where  $D_B$  is the diffusion coefficient of the mobile electrons, assumed here to be given by the equilibrium  
 124 Einstein relation  $D_B = \mu k T_0 / q$ , with  $q$  the carrier charge,  $T_0$  the room temperature, and  $k$  the  
 125 Boltzmann constant. At equilibrium, the device is assumed to be spatially uniform, with an electron  
 126 density  $n_0$  neutralized by an equal density of opposite fixed charges. Furthermore, assuming Maxwellian  
 127 distributions, the densities of carriers in the traps and in the mobile states are given by

$$n_{T0} = C_0 g_T \exp\left[-\frac{E_T}{k T_0}\right] = C_0 g_T, \quad n_{B0} = C_0 g_B \exp\left[-\frac{E_B}{k T_0}\right] = C_0 g_B \exp\left[-\frac{\Delta}{k T_0}\right]. \quad (2)$$

128 The normalization constant  $C_0$  is obtained from the total electron density  $n_0$ , leading to:

$$n_{T0} = \frac{n_0}{1 + (g_B/g_T) \exp[-\Delta/(k T_0)]}, \quad n_{B0} = \frac{n_0}{1 + (g_T/g_B) \exp[\Delta/(k T_0)]}. \quad (3)$$

129 In presence of an electric field  $F(x, t)$ , electrons gain energy; furthermore, the excitation energy to reach  
 130 the upper level is reduced by the field according to the Poole model (Poole, 1916), to become

$$\Delta'(x, t) = \Delta - \gamma |F(x, t)|, \quad (4)$$

131 with  $\gamma$  a suitable constant.<sup>1</sup> Out of equilibrium we assume that an electron temperature  $T_e(x, t)$  is defined,  
 132 such that the electron populations, in analogy with (3), read

$$\tilde{n}_T(x, t) = \frac{n(x, t)}{1 + (g_B/g_T) \exp[-\Delta'/(k T_e)]}, \quad \tilde{n}_B(x, t) = \frac{n(x, t)}{1 + (g_T/g_B) \exp[\Delta'/(k T_e)]}, \quad (5)$$

133 It is worth noting that a variation of the electric field  $F(x, t)$  is instantaneously accompanied by a variation  
 134 of the activation energy  $\Delta'$ , while the carriers require some time to adjust their occupations to the new  
 135 situation. Thus, the above quantities  $\tilde{n}_B(x, t)$  and  $\tilde{n}_T(x, t)$  are to be considered “tendential” values  
 136 (Jacoboni et al., 2017).

## 137 2.1 Equations

138 The model is based on a set of four differential equations, each encoding a basic physical principle.

<sup>1</sup> Elsewhere the Poole-Frenkel model, viz,  $\Delta' = \Delta - \gamma' \sqrt{|F|}$  (Jacoboni et al., 2017) is used in the description of electron transport in chalcogenides. The Poole model adopted here is usually appropriate for large concentrations of traps (Ielmini and Zhang, 2007). The theoretical development presented in this paper can include either approach.

139 i. Particle continuity: only charges in the mobile states can move, so that the rate of change of electron  
140 density at a given position  $x$  reads:

$$\frac{\partial n}{\partial t} = -\frac{\partial j}{\partial x}, \quad (6)$$

141 ii. Local particle redistribution: as indicated in (6), particles that cross the device at the position  $x$  come  
142 from mobile states. The rate of change of the concentration  $n_B$  accounts for redistribution between  
143 trap and mobile states, and reads

$$\frac{\partial n_B}{\partial t} = \frac{\partial n}{\partial t} - \frac{n_B - \tilde{n}_B}{\tau_n}, \quad (7)$$

144 where  $\tau_n$  is the mobile-carrier relaxation time, taken as a model parameter, and  $\tilde{n}_B$  is given by (5).

145 iii. Energy continuity: the energy density  $\epsilon^t$  at  $(x, t)$  is given by  $n_B \Delta$  since  $E_T = 0$ . Its variation accounts  
146 for the power density pumped by the field, the space variation of the energy flux  $j \Delta$ , and the energy  
147 relaxed to the phonon bath which, in this case, is described by a temperature-relaxation time  $\tau_T$   
148 Buscemi et al. (2014b):

$$\frac{\partial \epsilon^t}{\partial t} = q j F - \Delta \frac{\partial j}{\partial x} - n \frac{k T_e - k T_0}{\tau_T}. \quad (8)$$

149 On the other hand, differentiating the total energy  $\epsilon^t(x, t) = n_B \Delta$ , and using (7), yields

$$\frac{\partial \epsilon^t}{\partial t} = \Delta \left[ \frac{\partial n}{\partial t} - \frac{n_B - \tilde{n}_B}{\tau_n} \right].$$

150 Combining this result with (8) and using (6) provides

$$q j F = n \frac{k T_e - k T_0}{\tau_T} + \Delta \frac{\tilde{n}_B - n_B}{\tau_n}. \quad (9)$$

151 This equation indicates that the power provided by the field is partially dissipated to the phonon bath,  
152 and partially devoted to distribute the electrons between trapped and mobile states. This equation  
153 allows for the evaluation of the electron temperature in terms of the other unknowns. However,  $T_e$   
154 appears also in  $\tilde{n}_B$ , so that the equations must be solved numerically.

155 iv. Poisson equation: the local carrier density  $n(x, t)$  is related to the local field  $F(x, t)$  by the Poisson  
156 equation:

$$\frac{\partial F}{\partial x} = \frac{1}{\varepsilon} \rho = -\frac{q}{\varepsilon} [n(x, t) - n_0], \quad (10)$$

157 where  $\varepsilon$  is the material's absolute permittivity.

158 It is worth observing that in steady state the second term at the right hand side of (9) vanishes due to (7);  
159 it follows that  $\tau_n$  has no influence on the steady-state behavior of the OTS device (more comments on this  
160 are made in Sect. 3.1).

## 161 2.2 Constraints

162 The four equations (6), (7), (9) and (10) govern the process we are interested in, and are solved, e.g., for  
163 the unknowns  $n$ ,  $F$ ,  $n_B$ , and  $T_e$ . All other variables of interest can be calculated from the set above. A  
164 number of conditions are imposed on the unknowns:

165 a) The electron temperature at the injecting contact is equal to the equilibrium temperature at all times:

$$T_e(0, t) = T_0. \quad (11)$$

166 b) At the source boundary of the device, the contact injects the electrons which are necessary to maintain  
167 local electric neutrality at all times:

$$n(0, t) = n_0, \quad (12)$$

168 which implies:

$$\left. \frac{\partial n(x, t)}{\partial t} \right|_{x=0} = 0 \quad \left. \frac{\partial F(x, t)}{\partial x} \right|_{x=0} = 0$$

169 (the second of the above derives from (10)). Finally,

170 c) an integral condition on the field is imposed by the voltage  $V_P(t)$  across the device:

$$V_P(t) = - \int_0^L F(x, t) dx, \quad (13)$$

171 where  $L$  is the device length.

172 The model illustrated above is of the hydrodynamic type, namely, it assumes that neither the lattice  
173 temperature nor the relaxation time  $\tau_T$  vary within the operating time scale of the device. This is justified  
174 by the fact that the effects of lattice heating can be neglected below threshold and do not alter the intrinsic  
175 time scale of the device above threshold (Piccinini et al., 2016).

## 176 2.3 Numerical solution

177 The non-linear system of equations outlined in Sects. 2.1, 2.2 is solved by iterations, starting from the  
178 equilibrium condition  $n(x, 0) = n_0$ ,  $F(x, 0) = 0$ ,  $n_B(x, 0) = n_0/[1 + (g_T/g_B) \exp[\Delta/(k T_0)]]$ , and  
179  $T_e = T_0$ ; the time and space derivatives are approximated by finite differences. Once the unknowns are  
180 known at time  $t$ , their updated values at  $t + \delta t$  are obtained with the following procedure:

- 181 1. The update  $n(x, t + \delta t)$  is derived from (6).
- 182 2. Equations (5) and (7) provide the update  $n_B(x, t + \delta t)$ .
- 183 3. The update  $F(x, t + \delta t)$  is obtained from (10) apart from the constant  $F(0, t)$ , which is found by  
184 imposing condition (13). The latter, in turn, is to be considered as prescribed if the device is in a  
185 standalone situation, that is, connected to a voltage generator; if, instead, the device is connected to  
186 an external circuit,  $V_P$  must be derived from the solution of the device-circuit system.
- 187 4. The update  $T_e(x, t + \delta t)$  is obtained from (9). Due to the strong non-linearity of this equation  
188 and the strict requirement of a positive solution, the combined bracketing and bisection techniques  
189 (Press et al., 1988, Sect. 9.1) proved to be more efficient and stable than other iterative methods like,  
190 e.g., the Newton-Raphson method.

## 191 2.4 Circuit model

192 In realistic conditions, the device under investigation is coupled with an external circuit that represents the  
193 measuring equipment. Following (Piccinini et al., 2016), the simplest circuit used in studying the response  
194 of an Ovonic device to an external bias includes the Ovonic device in series with a load resistance  $R_L$   
195 and a waveform generator  $V(t)$ . From the viewpoint of the external circuit, the contacts enclosing the

196 chalcogenide layer can be represented by a contact resistance  $R_S$  and a parasitic capacitance  $C_S$ ; wirings  
 197 and probes introduce a further parallel parasitic capacitance  $C_C$ . The resulting circuit is sketched in Fig.  
 198 1, where the Ovonic device is indicated with  $P$ , and  $C = C_S + C_C$ .

199 The inclusion of the circuit into the simulation can be done at different levels of completeness. The first,  
 200 more general level (Sect. 2.4.1), couples the circuit with a numerical model of the Ovonic device; with  
 201 respect to that illustrated in Sects. 2.1, 2.2, here the model is simplified by assuming that the device is  
 202 homogeneous, while the dynamic aspects of the Ovonic device, as described by the relaxations times, are  
 203 kept. The second level, less expensive from the numerical standpoint (Sect. 2.4.2), couples the external  
 204 circuit with a static model of the Ovonic device, namely, a model of the form  $I_P(V_P)$ .

#### 205 2.4.1 Coupling the circuit with a dynamic PCM model

206 To express the voltage drop  $V_P$  across the Ovonic device, in the circuit model we assume a constant-  
 207 field approximation, which is acceptable for devices longer than 10 nm (Piccinini et al., 2016). It follows  
 208  $V_P = L F(t)$ , whence  $V = R_L I + L F + A R_S J_P$ , with  $A$  the cross sectional area of the metallic plates  
 209 and  $J_P = q j$  the current density across the Ovonic device. Using (1) after neglecting the diffusive term  
 210 yields a relation between the field and the mobile carrier concentration:

$$F = \frac{V - R_L I}{L + A R_S q \mu n_B}. \quad (14)$$

211 To complete the coupling with the external circuit, another equation is necessary; in it, the voltage drop  
 212  $V_P$  must appear, which is in turn determined from the microscopic model accounting for the relaxation  
 213 times. One notes from Fig. 1 that  $V - V_P = R_L I + R_S (I - C \dot{V}_C)$ , with  $V_C = V - R_L I$ ; combining  
 214 these two relations yields the equation sought,

$$R_S R_L C \dot{I} + (R_L + R_S) I + V_P = R_S C \dot{V} + V, \quad (15)$$

215 where the right hand side is prescribed. Equations (14, 15) are then added to (6, 7, 9) to determine the  
 216 electric performance of the OTS cell (Piccinini et al., 2016).

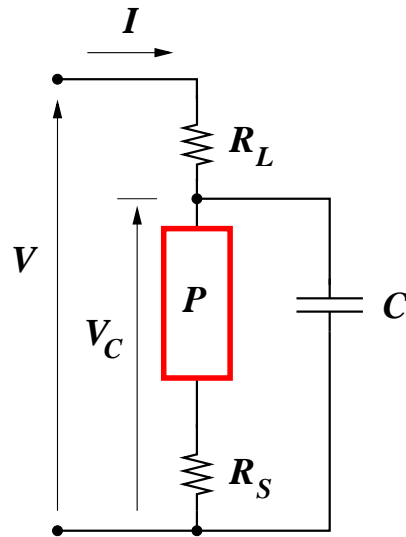
#### 217 2.4.2 Coupling the circuit with a static PCM model

218 Still considering the circuit of Fig. 1, the static characteristic of the PCM is sketched as shown in Fig.  
 219 2; the approximation of considering a piecewise-linear characteristic has the advantage of affording an  
 220 easy analytical approach.<sup>2</sup> Letting  $R_1(R_2)$  be the resistance of the lower (upper) branch ( $R_1 \gg R_2$ ), it  
 221 follows that the resistance of the series made of  $P$  and the heater is  $R_C^- = R_1 + R_S$  when  $V_P < V_{th}$  and  
 222  $R_C^+ = R_2 + R_S$  when  $V_P > V_{th}$ ; balancing the currents at the upper node of  $P$  yields, for  $V_P < V_{th}$ ,

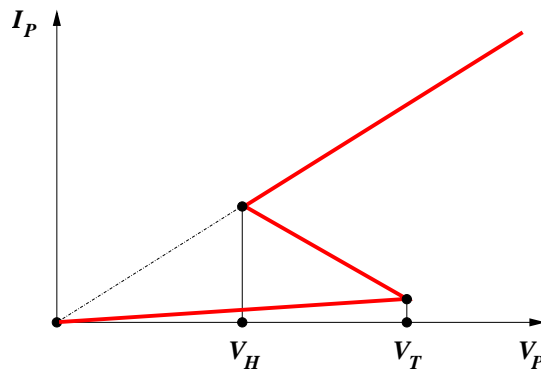
$$C \dot{V}_C + \frac{V_C}{R_C^-} = \frac{V - V_C}{R_L}, \quad \dot{V}_C + \frac{V_C}{\tau_C^-} = \frac{V}{\tau_L}, \quad (16)$$

<sup>2</sup> In principle, the approximation of a piecewise-linear characteristic could be avoided: one may in fact invert  $V_C = V_P + R_S I_P(V_P)$  to extract  $I_P(V_C)$ , then solve  $C \dot{V}_C + I_P(V_C) = (V - V_C)/R_L$  for  $V_C$ , with  $V = V(t)$  prescribed. This procedure would require a separate solution of a non-linear equation in different regions of  $V_C$ .





**Figure 1.** Circuit embedding the PCM (Piccinini et al., 2016). Parameters referred to the PCM take suffix  $P$  in the equations and figures.



**Figure 2.** Schematic model of the S-shaped  $I_P(V_P)$  characteristic of the PCM.

223 with  $\tau_L = R_L C$  and  $\tau_C^- = R_C^- \tau_L / (R_C^- + R_L)$ , this yielding

$$V_C \exp(t/\tau_C^-) = V_C(t_0) \exp(t_0/\tau_C^-) + Y, \quad Y = \frac{1}{\tau_L} \int_{t_0}^t \exp(\theta/\tau_C^-) V(\theta) d\theta. \quad (17)$$

224 As mentioned above, here the applied voltage is a ramp,  $V = \alpha t$ , whence

$$Y = \frac{\alpha \tau_C^-}{\tau_L} (t - \tau_C^-) \exp\left(\frac{t}{\tau_C^-}\right) + \frac{\alpha \tau_C^-}{\tau_L} (\tau_C^- - t_0) \exp\left(\frac{t_0}{\tau_C^-}\right). \quad (18)$$

225 In the first part of the ramp it is  $t_0 = 0$ ,  $V_P < V_{th}$ ,  $V_C(t_0) = 0$ , and

$$V_C = \frac{\alpha (\tau_C^-)^2}{\tau_L} \left[ \frac{t}{\tau_C^-} - 1 + \exp\left(-\frac{t}{\tau_C^-}\right) \right]. \quad (19)$$

226 The voltage across  $P$  is related to  $V_C$  by  $V_C = V_P (1 + R_S/R_1)$ , and reaches the threshold value at a time  
 227  $t_{th}$  such that

$$V_{th} = \frac{\alpha (\tau_C^-)^2 / \tau_L}{1 + R_S/R_1} \left[ \frac{t_{th}}{\tau_C^-} - 1 + \exp \left( -\frac{t_{th}}{\tau_C^-} \right) \right]. \quad (20)$$

228 The  $V_C(t)$  relation (19) is nonnegative and monotonic in the interval  $0 \leq t \leq t_{th}$ . When  $t$  reaches  $t_{th}$ ,  
 229 the resistance of  $P$  changes abruptly, so that  $R_C^- = R_1 + R_S$  and  $R_C^+ = R_2 + R_S \ll R_C^-$ ; due to the  
 230 capacitor connected in parallel, voltage  $V_C$  is continuous at  $t_{th}$ , so that the current  $(V - V_C)/R_L$  provided  
 231 by the bias is continuous as well. On the other hand, current  $I_P$  flowing through  $P$  is discontinuous at  
 232  $t_{th}$  (specifically,  $I_P$  increases due to the decrease in resistance); as the extra current is supplied by the  
 233 capacitor, it follows that  $\dot{V}_C^+ \neq \dot{V}_C^-$ . If necessary, the variation in  $\dot{V}_C$  can be evaluated from (16): writing  
 234 (16) at  $t_{th}^-$  and  $t_{th}^+$ , and subtracting, yields

$$C \dot{V}_C^+ = C \dot{V}_C^- - \frac{R_C^- - R_C^+}{R_C^- R_C^+} V_C < C \dot{V}_C^-. \quad (21)$$

235 In the second part of the ramp ( $t > t_{th}$ ) it is  $t_0 = t_{th}$ ,  $V_P > V_{th}$ , and

$$V_C(t_{th}) = \frac{\alpha (\tau_C^-)^2}{\tau_L} \left[ \frac{t_{th}}{\tau_C^-} - 1 + \exp \left( -\frac{t_{th}}{\tau_C^-} \right) \right]. \quad (22)$$

236 Here the equation to be solved has the same form as (16), with  $R_C^-$  replaced with  $R_C^+$  and  $\tau_C^-$  replaced  
 237 with  $\tau_C^+ = R_C^+ \tau_L / (R_C^+ + R_L)$ ; using again the ramp one finds

$$V_C = V_C(t_{th}) \exp \left( \frac{t_{th} - t}{\tau_C^+} \right) + \frac{\alpha (\tau_C^+)^2}{\tau_L} \left[ \left( \frac{t}{\tau_C^+} - 1 \right) + \left( 1 - \frac{t_{th}}{\tau_C^+} \right) \exp \left( \frac{t_{th} - t}{\tau_C^+} \right) \right]. \quad (23)$$

238 The quantity to be measured is the current  $(V - V_C)/R_L$  provided by the bias, namely, using (19) for  
 239  $0 \leq t \leq t_{th}$ ,

$$I^- = \frac{\alpha}{R_L} t - \frac{\alpha (\tau_C^-)^2}{R_L \tau_L} \left[ \frac{t}{\tau_C^-} - 1 + \exp \left( -\frac{t}{\tau_C^-} \right) \right], \quad (24)$$

240 or, using (23) for  $t \geq t_{th}$ ,

$$I^+ = \frac{\alpha}{R_L} t - \frac{V_C(t_{th})}{R_L} \exp \left( \frac{t_{th} - t}{\tau_C^+} \right) - \frac{\alpha (\tau_C^+)^2}{R_L \tau_L} \left[ \left( \frac{t}{\tau_C^+} - 1 \right) + \left( 1 - \frac{t_{th}}{\tau_C^+} \right) \exp \left( \frac{t_{th} - t}{\tau_C^+} \right) \right]. \quad (25)$$

241 The asymptotic behavior of the current, obtained from (24) and (25) is, respectively,

$$I^- = \frac{\alpha t}{R_L + R_1 + R_S}, \quad I^+ = \frac{\alpha t}{R_L + R_2 + R_S}. \quad (26)$$

### 3 SIMULATION RESULTS

242 The voltage pulse generated by experimental equipments varies from zero to its maximum programmed  
 243 value in a finite time which, at present, can be as short as few ns (Wimmer and Salinga, 2014; Saxena et al.,  
 244 2021). Thus, every “real” voltage pulse contains, *de facto*, ramps with rise and fall times of finite  
 245 duration; this implies the existence of a time transient of the electrical response of the device, during

246 which the internal electric field increases or decreases. This effect may or may not be relevant according  
247 to how the rise time compares with the time scale of the microscopic processes responsible for the carrier  
248 heating at the origin of OTS, and whether or not the maximum voltage applied to the device exceeds  
249 the threshold voltage for the Ovonic switch. The simulations discussed in this section explore different  
250 physical situations of a GST-225 chalcogenide device, starting from ideal cases where circuit parasitic  
251 elements are absent and the external pulses have negligible rise times, then moving towards conditions  
252 closer to the experimental reality. Aim of the study is to test our theoretical model, based on hot-carrier  
253 effects, against experimentally-detected electric properties of amorphous chalcogenides, on time scales  
254 around and below the nanosecond, obtained from the last experimental results appeared in the literature  
255 (Saxena et al., 2021). In absence of information about the cross-sectional area of the devices employed in  
256 the experiments, the value  $5,000 \text{ nm}^2$  has been used in all simulations to convert current densities obtained  
257 from the simulations into charge currents.

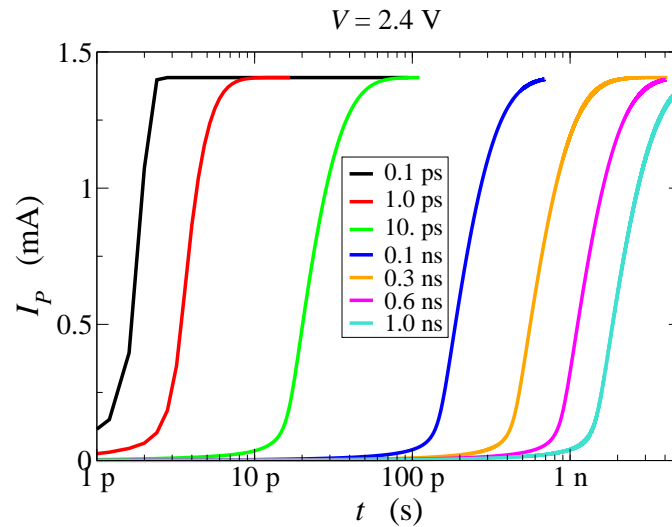
### 258 3.1 The ideal case: the voltage step

259 The exploration starts from the ideal case of negligible parasitic effects and negligible rise time of the  
260 applied voltage. Assuming a step-shaped voltage profile, the time dependence of the quantities relevant  
261 for transport are due only to the microscopic parameters of the model (such parameters are listed in Tab.  
262 1). Some parameters are known from experiments, while others can be tuned on the basis of the details  
263 of the  $I_P(V_P)$  characteristic for a variety of bias conditions. A preliminary study about the influence  
264 of the microscopic parameters on the transport results obtained from the present model is reported in  
265 (Jacoboni et al., 2017); there, in particular, the microscopic parameter  $\tau_T$  of (8) has been proven to control  
266 the heating process of the carriers for a given internal field and, consequently, the value of the threshold  
267 voltage. In the same paper, however, a discrepancy was found between the delay time  $t_d$  predicted by the  
268 model (of the order of tens of ps) and the much longer experimental values (possibly also influenced by  
269 parasitic effects).

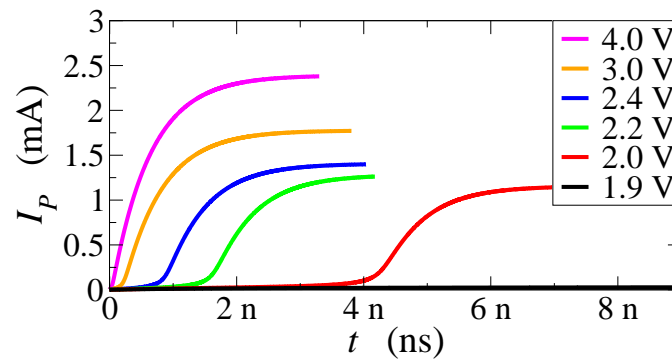
270 In a recent paper by (Saxena et al., 2021) for GST-225, the experimental steady-state OTS voltage ( $V_{\text{th}}$ )  
271 for a device of length  $L = 53 \text{ nm}$ , obtained with very long leading/trailing edges of the applied voltage,  
272 is  $V_{\text{th}} = 2.0 \pm 0.1 \text{ V}$ . This value corresponds to a threshold field  $E_{\text{th}} \sim 10^7 \text{ V/m}$ , and compares well  
273 with that obtained in (Jacoboni et al., 2017) for  $\tau_T = 0.15 \text{ ps}$ . Consequently, this value for  $\tau_T$  is also used  
274 in the present paper. The electric measurements in the time domain also reported in (Saxena et al., 2021)  
275 allow for a theoretical test on the second microscopic parameter  $\tau_n$  of (7), which rules the relaxation of  
276 the mobile carrier population to the steady state value for a given applied field.

277 Based on the set of parameters of (Jacoboni et al., 2017), a batch of simulations is presented here for  
278 different values of  $\tau_n$  in order to assess the effect of this parameter on the rise time of the current after the  
279 application of a voltage step above threshold (here the value  $V = 2.4 \text{ V}$  has been used for the voltage step).  
280 The results are reported in Fig. 3; while no effect of the variation of  $\tau_n$  has been found on the threshold  
281 value, it is seen that a delay time of about  $1 \text{ ns}$  (that is, in the same range of the experiments (Saxena et al.,  
282 2021)) is achieved with  $\tau_n = 0.6 \text{ ns}$ , thus demonstrating that the theoretical model can be tuned in such a  
283 way as to compare well with experiments in the nanosecond scale.

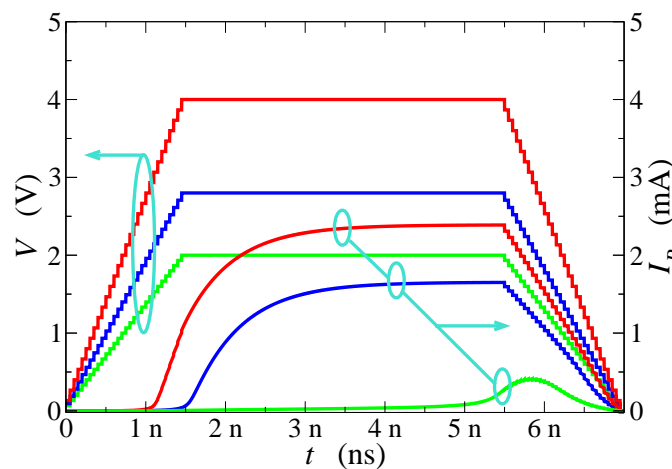
284 Furthermore, Fig. 4 shows current  $I_P$  as a function of time for different values of the step voltage: the  
285 higher the voltage, the shorter the delay time of the current, yielding a delay shorter than a ns at the largest  
286 biases considered. This behaviour is in agreement with experimental evidence (Saxena et al., 2021).



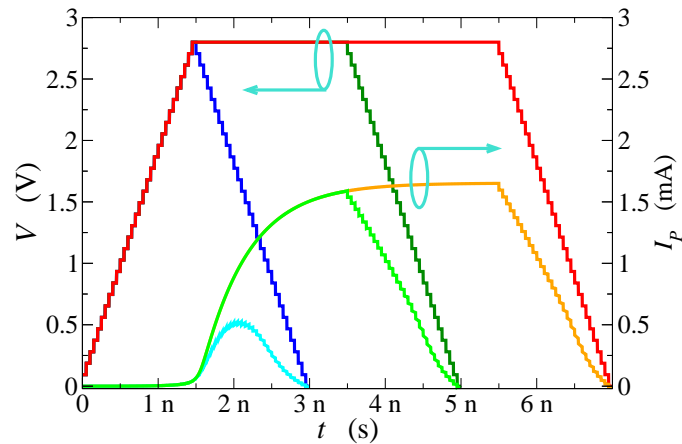
**Figure 3.** Current flowing across the PCM device as a function of time after the application of a 2.4 V external voltage step at  $t = 0$ . Different values for the microscopic parameter  $\tau_n$  have been tested.



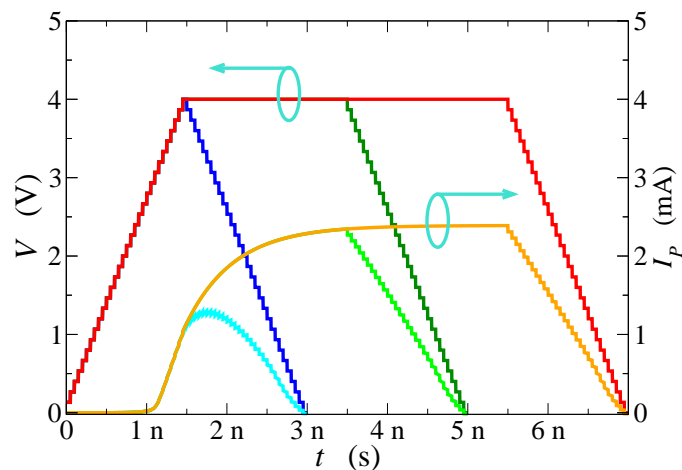
**Figure 4.** Current flowing across the PCM device as a function of time after the application of voltage steps of different amplitudes. The microscopic parameter  $\tau_n$  has been set to 0.6 ns.



**Figure 5.** Current flowing across the PCM device as a function of time (right scale) after the application of voltage trapezoidal profiles of different amplitude (left scale). In all cases, rise and fall times are 1.5 ns and the duration of the plateau is 4 ns.



**Figure 6.** Current flowing across the PCM device as a function of time (right scale) after the application of voltage trapezoidal profiles of 2.8 V amplitude (left scale). Rise and fall times are 1.5 ns in all cases, whereas the plateau durations are 0, 2, and 4 ns.

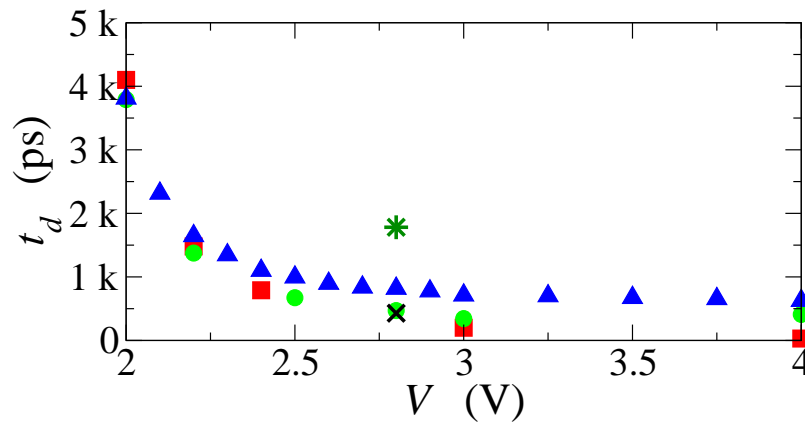


**Figure 7.** Current flowing across the PCM device as a function of time (right scale) after the application of voltage trapezoidal profiles of 4 V amplitude (left scale). Rise and fall times are 1.5 ns in all cases, whereas the plateau durations are 0, 2, and 4 ns.

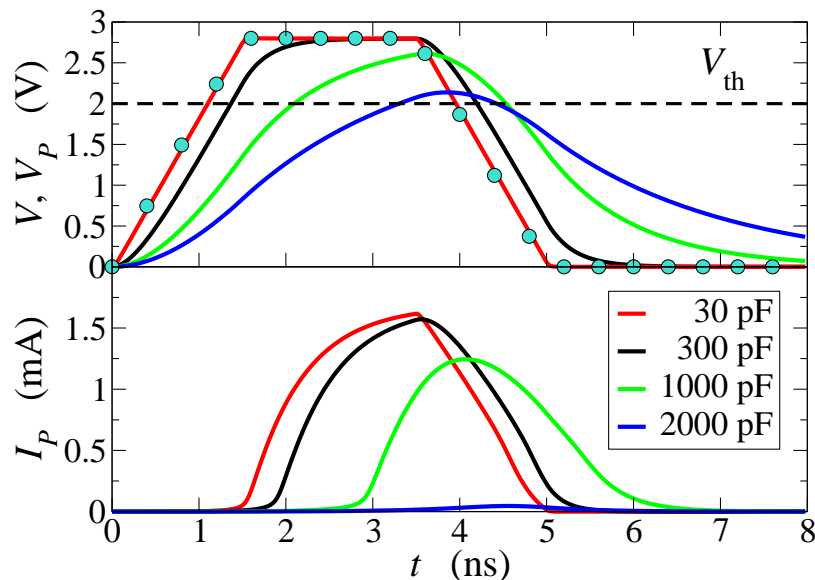
### 287 3.2 Towards the real world: finite rise and fall times, no parasitic effects

288 A step towards realistic bias conditions is achieved by considering that external waveform generators  
 289 provide pulses with finite rise and fall times. Top-level equipments generate voltage pulses with rise and  
 290 fall times as fast as 1 ns, and with 1.5 ns Full-Width Half Maximum (FWHM) (Saxena et al., 2021).  
 291 These times are comparable with the microscopic relaxation times that govern the heating process and  
 292 are assumed to be responsible for the OTS effect. Thus, still in absence of parasitic effects, a comparison  
 293 of the theoretical predictions with the experimental scenario on a ns time scale has been carried on with  
 294 reference to the bias conditions reported in (Saxena et al., 2021).

295 Figure 5 reports the current flowing across the GST layer, as a function of time, due to the application of  
 296 a trapezoidal profile with 1.5 ns rise and fall times, and a 4 ns duration of the plateau. Different values of  
 297 the plateau have been considered, ranging from 2 V (corresponding to the OTS voltage) up to 4 V. Figures  
 298 6 and 7 report similar data for 2.8 and 4 V plateau amplitudes, respectively, with plateau durations of 0, 2,  
 299 and 4 ns in each case.

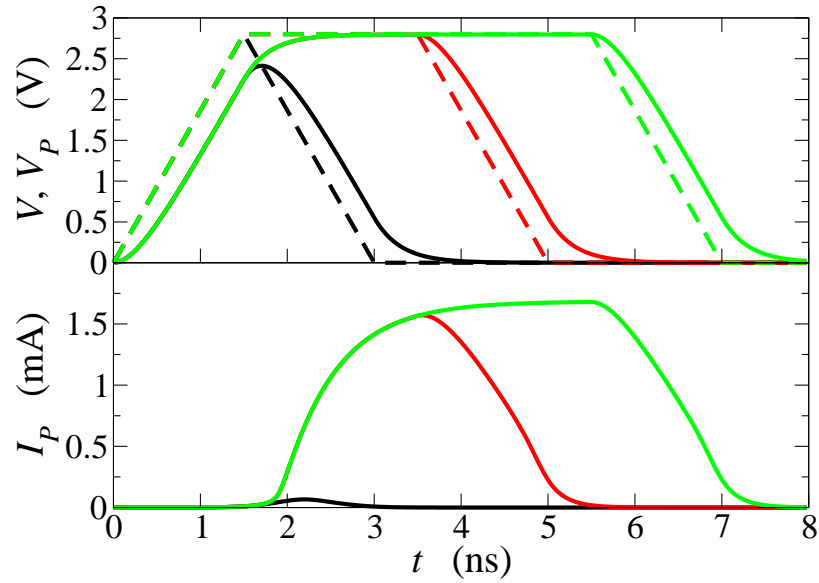


**Figure 8.** Simulated delay time  $t_d$  as a function of the amplitude of the applied signal  $V$ . The red squares and the green circles refer to the case where the input signal is applied directly to the PCM and consists of a voltage step or, respectively, of a trapezoidal voltage pulse like those of Fig. 5. The blue triangles refer to the case where the input signal (still a trapezoidal pulse) is applied through the circuit of Fig. 1, with  $R_L = R_S = 1 \Omega$  and  $C = 300 \text{ pF}$ . The cross (star) shows the delay time for  $V = 2.8 \text{ V}$  when the value of the capacitance is changed to  $30 \text{ pF}$  or  $1000 \text{ pF}$ , respectively.

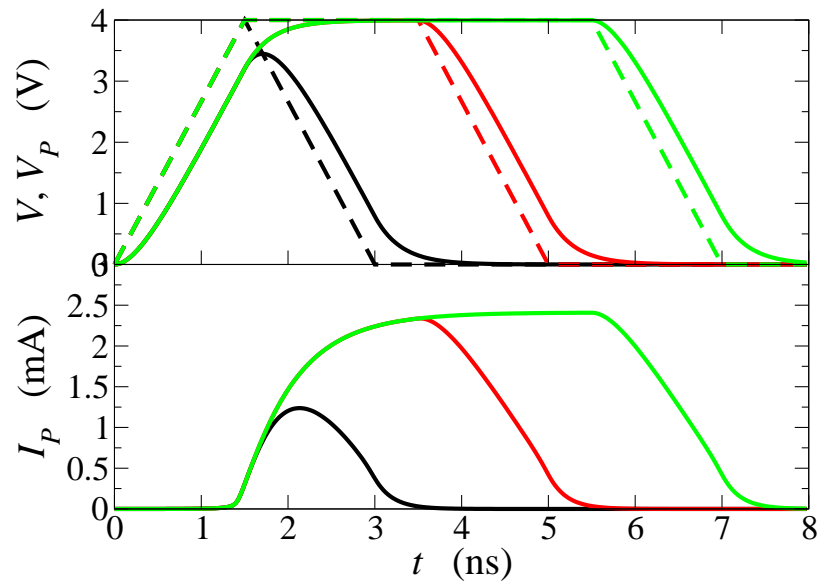


**Figure 9.** Simulated voltage drop  $V_P$  (above) and current  $I_P$  (below) of the PCM. The input signal  $V$  (above, circles) has a trapezoidal form with a plateau at  $2.8 \text{ V}$ , and is applied through the circuit of Fig. 1 with  $R_L = R_S = 1 \Omega$ . Capacitance  $C$  is given different values as shown in the figure. The horizontal, dashed line marks the threshold voltage  $V_{th}$ .

300 In agreement with what reported by (Saxena et al., 2021), ultrafast transient characteristics in the ns scale  
 301 and below have been obtained in all considered cases. These results suggest that the delay time  $t_d$ , defined  
 302 as the time elapsed between the instant at which the external bias exceeds the steady-state threshold value  
 303 and the steep rise in the device current, varies in a wide range of values depending on the shape of the  
 304 applied voltage. In particular, for plateau values significantly above threshold the carrier-heating process  
 305 is very effective well before the maximum value of the voltage is reached; consequently, shorter delay  
 306 times are observed (Fig. 5). Moreover, when the plateau value and the rise and fall times are fixed, the  
 307 duration of the plateau influences the maximum value of the measured current, but does not affect the  
 308 delay time (Figs. 6 and 7).



**Figure 10.** Same as in Fig. 9, with different durations of the plateau of  $V$ ; the latter is set at 2.8 V, and capacitance  $C$  is set at 300 pF.



**Figure 11.** Same as in Fig. 10, with different durations of the plateau of  $V$ ; here the latter is set at 4 V, and capacitance  $C$  is kept 300 pF.

309 All the above results are in agreement with those of (Saxena et al., 2021), and confirm the validity of  
 310 a theoretical model for the OTS process based on purely electronic mechanisms. At least in absence of  
 311 parasitic effects, and provided that the microscopic time constants of the chalcogenide in hand lie in the  
 312 ns range and below, the speed of threshold switching in OTS devices can be pushed below the ns scale by  
 313 a voltage pulse of suitable duration and value. Figure 8 summarises the results for the delay time  $t_d$  as a  
 314 function of the applied voltage amplitude for the bias conditions considered so far. For rise and fall times  
 315 of 1.5 ns, the delay times obtained for the step (red symbols) and trapezoidal profiles (green symbols) are  
 316 almost overlapping near threshold, while at higher biases the response to the trapezoidal shape exhibits

317 still comparable, but longer delay times; this is probably due to a slower carrier heating process when the  
318 voltage ramps up the maximum value in about a ns.

### 319 3.3 The real world: finite rise and fall times, with parasitic effects

320 Parasitic effects connected to the measuring system and wirings can be minimized with a top level  
321 apparatus, but cannot be eliminated in full. To account for their contribution we have repeated the  
322 simulations of the delay time after embedding the PCM device into the circuit of Fig. 1, varying the  
323 equivalent capacitance  $C$ . The series resistances have been set at negligible values, since previous  
324 investigations pointed out a major modulating effect of the capacitance (Piccinini et al., 2016). The  
325 characteristic time of the circuit is thus proportional to  $\tau_L = R_L C$ , and acts as an additional delay  
326 time.

327 Figure 9 reports the voltage drop  $V_p$  across the PCM when the input signal has a trapezoidal form, with  
328 1.5 ns rise and fall times, and a 2.8 V plateau with a 2 ns duration; the equivalent capacitance has been varied  
329 from 30 to 2000 pF. Due to the broadening of  $V_p$  (top panel), the higher the capacitance the shorter is  
330 the time interval during which  $V_p > V_{th}$ . By way of example,  $C = 2000$  pF corresponds to  $\tau_L = 2$  ns,  
331 equal to the duration of the plateau; in this case the electronic switching is hindered (low panel), because  
332 the switching to the ON state occurs only if the applied signal is kept at its plateau value long enough, in  
333 such a way that the electronic processes described earlier can be activated and completed. Similar results  
334 are also shown in Figs. 10 and 11, where the duration of the plateau is increased from 0 to 4 ns, while the  
335 capacitance is kept fixed. Once again, the maximum voltage drop  $V_p$  is always larger than the threshold  
336 voltage but, if the signal drops soon after reaching the maximum value, the threshold switching does not  
337 occur (low panel of Fig. 10, black curve) or is incomplete (low panel of Fig. 11, black curve). These  
338 results are consistent with the findings of (Saxena et al., 2021).

339 For the sake of completeness we point out that the present transport model was developed for the  
340 amorphous OFF phase, and its parameters have been optimised for describing the subthreshold region.  
341 ON state currents are underestimated, and a quantitative comparison with the experimental currents also  
342 in the amorphous ON region preceding the phase change would require a further model enhancement  
343 like, e.g., the inclusion of electron band states and the mobility increase that sets in when electrons  
344 coming from low-mobility states are excited to high-energy mobile states, and a consequent parameter  
345 recalibration. However, an even steeper rise of the current is expected not to alter appreciably the present  
346 findings.

347 In conclusion, we can split the measured delay time into two components: the former one is intrinsic  
348 to the switching phenomenon, and is associated to the time required to promote a significant number of  
349 carriers from localized to mobile states, thanks to carrier heating induced by the electric field (a similar  
350 change in the transport mechanism is also proposed in (Noé et al., 2017)); the latter component is instead  
351 depending on the measuring apparatus and wirings, and acts as a nearly rigid offset. This component can  
352 largely dominate if no particular care is taken in designing the circuitry. To support this statement, we see  
353 in Fig. 8 that increasing the capacitance by about three times nearly doubles the delay time.

354 A simplified analysis of the same issue has been carried out for comparison, with reference to the circuit  
355 of Fig. 1, and to the schematic model of the PCM characteristic of Fig. 2. The delay time  $t_d$  has been  
356 calculated from the relations of Sect. 2.4.2, using the same values of the lumped elements as those of Fig.  
357 8. The S-shaped  $I_P(V_P)$  characteristic of the PCM has been modeled with  $R_1 = 1$  M $\Omega$  and  $R_2 = 1$  k $\Omega$ ,



358 a threshold voltage  $V_{\text{th}} = 2$  V, and a contact resistance  $R_S = 1$   $\Omega$ . It is worth observing that, since the  
359 PCM is described with a static characteristic, here the delay is due to the combined effect of  $R_L$  and  $C$   
360 (in other terms, there would be no delay if  $R_L = 0$  and/or  $C = 0$ ). The ramp slope  $\alpha = 1.87 \times 10^9$  V/s  
361 ( $\alpha = 2.67 \times 10^9$  V/s) corresponds to a rise time of 1.5 ns from  $V = 0$  to  $V = 2.8$  V ( $V = 4$  V); it follows  
362 that  $V = \alpha t$  becomes equal to the threshold voltage at  $t' \simeq 1.07$  ns ( $t' = 0.75$  ns).

363 The results are summarized in Tab. 2; one notes that, as expected, the same value of  $\tau_L = R_L C$  provides  
364 the same value of  $t_d$ . Comparing with Fig. 8, one also notes that the delay times calculated as in Sect.  
365 2.4.2 are lower (by a factor 2.5 at least) than those shown in Fig. 8. Remembering the discussion carried  
366 out in the first part of this section, this outcome is ascribed to the fact that, as the PCM characteristic of  
367 Fig. 2 is purely static, the expressions of Sect. 2.4.2 do not account for the additional delay due to the  
368 internal relaxation times of the PCM.

## 4 CONCLUSIONS

369 The delay time of the OTS onset, i.e., the delay between the instant at which the external voltage applied  
370 to the chalcogenide cell equals the static threshold voltage and the instant at which a steep rise of the  
371 current through the OTS device occurs, is a quantity that is strongly influenced by the time dependence  
372 of the applied voltage. This effect has been studied in this paper by means of theoretical approaches of  
373 different complexities, all based upon the assumption that OTS is mainly due to electronic effects.

374 A purely microscopic model based on a trap-limited transport scheme with appropriate microscopic  
375 parameters provides delay times below the ns limit, as recently measured in GST-225 cells (Saxena et al.,  
376 2021). The availability of new experimental results in the ns-ps time domain allows for a better tuning  
377 of the microscopic parameter  $\tau_n$ , which greatly improves the theoretical quantitative results for the delay  
378 time with respect to our previous work (Jacoboni et al., 2017; Brunetti et al., 2020). Parasitic effects do  
379 not produce a noticeable increase of  $t_d$ , at least for suitably optimised, electrical-test systems like those  
380 used in advanced experiments. Based on the simulation tests performed with detailed microscopic models,  
381 an analytical, computationally efficient approach has been developed which captures the key features of  
382 the voltage-dependent transient characteristic of OTS devices, and is suitable for implementation into  
383 device-simulation tools.

384 The simulated transient currents are in substantial agreement with the experimental values obtained with  
385 similar external bias voltages, this confirming the existence of delay times in the sub-ns time scale on the  
386 basis of the physical process of carrier heating due to energy transfer from the external field. Analytical  
387 calculations confirm that, for realistic values of the parasitic parameters, the internal relaxation times of  
388 the PCM provide a non-negligible contribution to the delay time  $t_d$ .

## CONFLICT OF INTEREST STATEMENT

389 The authors declare that the research was conducted in the absence of any commercial or financial  
390 relationships that could be construed as a potential conflict of interest.

## AUTHOR CONTRIBUTIONS

391 All Authors have contributed equally to this work.

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393 members.

## TABLES

**Table 1.** Microscopic parameters of Eqs. (6), (7), (9), and (10). Apart from  $\tau_n$ , the parameter values are taken from (Jacoboni et al., 2017).

Symbol	Definition	Value	Units
$E_T$	Energy level of traps	0	eV
$E_B$	Energy level of mobile states	0.35	eV
$\Delta$	$E_B - E_T$		eV
$g_T$	DoS of trap states		$\text{eV}^{-1}$
$g_B$	DoS of mobile states		$\text{eV}^{-1}$
$\Gamma$	$g_T/g_B$	$2.5 \cdot 10^{-3}$	
$\gamma$	Coefficient of Poole effect	$3.36 \cdot 10^{-28}$	C m
$\varepsilon$	Relative permittivity of the material	15	
$\mu$	Mobility of mobile electrons	$5.9 \cdot 10^{-4}$	$\text{m}^2(\text{V s})^{-1}$
$n_0$	Equilibrium electron concentration	$6.8 \cdot 10^{25}$	$\text{m}^{-3}$
$\tau_T$	Temperature-relaxation time	$1.5 \cdot 10^{-13}$	s
$\tau_n$	Recombination time	$0.6 \cdot 10^{-9}$	s
$L$	Device length	$53 \cdot 10^{-9}$	m
$T_0$	Room temperature	298	K

**Table 2.** Delay time  $t_d$  as a function of the lumped elements of Fig. 1. Symbol  $\alpha$  indicates the slope of the ramp (see text).

$R_L$ ( $\Omega$ )	$C$ (pF)	$\alpha$ ( $10^9$ V/s)	$t_d$ (ps)
1	30	1.87	30
1	300	1.87	297
1	1000	1.87	854
10	30	1.87	297
1	30	2.67	30
1	300	2.67	291
1	1000	2.67	784
10	30	2.67	291

## REFERENCES

- 394 Servalli G. A 45nm generation Phase Change Memory technology. *IEEE International Electron Devices*  
395 *Meeting (IEDM), Technical Digest* (2009), 1–4.
- 396 [Dataset] Optane (2017a). [http://techinsights.com/about-techinsights/overview/blog/intel-3D-xpoint-](http://techinsights.com/about-techinsights/overview/blog/intel-3D-xpoint-memory-die-removed-from-intel-optane-pcm/)  
397 [memory-die-removed-from-intel-optane-pcm/](http://techinsights.com/about-techinsights/overview/blog/intel-3D-xpoint-memory-die-removed-from-intel-optane-pcm/).
- 398 [Dataset] Optane (2017b). [http://techinsights.com/about-techinsights/overview/blog/memory-selector-](http://techinsights.com/about-techinsights/overview/blog/memory-selector-elements-for-intel-optane-xpoint-memory/)  
399 [elements-for-intel-optane-xpoint-memory/](http://techinsights.com/about-techinsights/overview/blog/memory-selector-elements-for-intel-optane-xpoint-memory/).
- 400 [Dataset] Choe J. Memory/Selector Elements for Intel Optane™ XPoint Memory (2017).  
401 <http://techinsights.com/>.
- 402 Arnaud F, Zuliani P, Reynard J, Gandolfo A, Disegni F, Mattavelli P, et al. Truly Innovative 28nm FDSOI  
403 Technology for Automotive Micro-Controller Applications embedding 16MB Phase Change Memory.  
404 *IEEE International Electron Devices Meeting (IEDM), Technical Digest* (2018), 18.4.1–18.4.4.
- 405 Markram H, Gerstner W, Sjöström PJ. A History of Spike-Timing-Dependent Plasticity. *Frontiers in*  
406 *Synaptic Neuroscience* **3** (2011) 4.
- 407 Le Gallo M, Sebastian A, Mathis R, Manica M, Giefers H, Tuma T, et al. Mixed-precision in-memory  
408 computing. *Nature Electronics* **1** (2018) 246–253.
- 409 Sebastian A, Le Gallo M, Khaddam-Aljameh R, Eleftheriou E. Memory devices and applications for  
410 in-memory computing. *Nature Nanotechnology* **15** (2020) 529–544.
- 411 [Dataset] Sarwat SG, Kersting B, Moraitis T, Jonnalagadda VP, Sebastian A. Phase Change  
412 Memtransistive Synapse (2021).
- 413 Lai S. Current status of the phase change memory and its future. *IEEE International Electron Devices*  
414 *Meeting (IEDM), Technical Digest* (2003), 10.1.1–10.1.4.
- 415 Raoux S, Wuttig M. *Phase Change Material — Science and Applications* (Springer) (2009).
- 416 Kolobov AV, Tominaga J. *Chalcogenides — Metastability and Phase Change Phenomena*. Materials  
417 Science (Springer) (2012).
- 418 Redaelli A, editor. *Phase Change Memory* (Springer) (2019).
- 419 Anbarasu M, Wimmer M, Bruns G, Salinga M, Wuttig M. Nanosecond threshold switching of GeTe<sub>6</sub>  
420 cells and their potential as selector devices. *Appl. Phys. Lett.* **100** (2012) 143505.
- 421 Wimmer M, Salinga M. The gradual nature of threshold switching. *New Journal of Physics* **16** (2014)  
422 113044.
- 423 Shukla KD, Saxena N, Durai S, Manivannan A. Redefining the Speed Limit of Phase Change Memory  
424 Revealed by Time-resolved Steep Threshold-Switching Dynamics of Ag-In-Sb-Te Devices. *Sci. Rep.* **6**  
425 (2016) 37868.
- 426 Saxena N, Raghunathan R, Manivannan A. A scheme for enabling the ultimate speed of threshold  
427 switching in phase change memory devices. *Sci. Rep.* **11** (2021) 6111.
- 428 Shukla KD, Saxena N, Manivannan A. An ultrafast programmable electrical tester for enabling time-  
429 resolved, subnanosecond switching dynamics and programming of nanoscale memory devices. *Rev.*  
430 *Sci. Instrum.* **88** (2017) 123906.
- 431 Ielmini D. Threshold switching mechanism by high-field energy gain in the hopping transport of  
432 chalcogenide glasses. *Phys. Rev. B* **78** (2008) 035308.
- 433 Cappelli A, Piccinini E, Xiong F, Behnam H, Brunetti R, Rudan M, et al. Conductive preferential paths  
434 of hot carriers in amorphous phase-change materials. *Appl. Phys. Lett.* **103** (2013) 083503.
- 435 Buscemi F, Piccinini E, Cappelli A, Brunetti R, Rudan M, Jacoboni C. Electrical bistability in amorphous  
436 semiconductors: A basic analytical theory. *Appl. Phys. Lett.* **104** (2014a) 022101.

- 437 Brunetti R, Jacoboni C, Piccinini E, Rudan M. Band transport and localised states in modelling the electric  
438 switching of chalcogenide materials. *J. Comp. Elect.* **19** (2020) 128.
- 439 Bogoslovskij NA, Tsendin KD. Electronic–thermal switching and memory in chalcogenide glassy  
440 semiconductors. *J. of Non-Crystalline Solids* **357** (2011) 992–995.
- 441 Le Gallo M, Athmanathan A, Krebs D, Sebastian A. Evidence for thermally assisted threshold switching  
442 behavior in nanoscale phase-change memory cells. *J. Appl. Phys.* **119** (2016) 025704.
- 443 Piccinini E, Brunetti R, Bordone P, Rudan M, Jacoboni C. Transient and oscillating response of ovonic  
444 devices for high-speed electronics. *J. Phys. D: Appl. Phys.* **49** (2016) 495101.
- 445 Jacoboni C, Piccinini E, Brunetti R, Rudan M. Time- and space-dependent electric response of ovonic  
446 devices. *J. Phys. D: Appl. Phys.* **50** (2017) 255103.
- 447 Poole HH. VIII. On the dielectric constant and electrical conductivity of mica in intense fields. *The*  
448 *London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science* **32** (1916) 112–129.  
449 Ser. 6.
- 450 Ielmini D, Zhang Y. Analytical model for subthreshold conduction and threshold switching in  
451 chalcogenide-based memory devices. *J. Appl. Phys.* **102** (2007) 054517.
- 452 Buscemi F, Piccinini E, Cappelli A, Brunetti R, Rudan M, Jacoboni C. Electrical bistability in amorphous  
453 semiconductors: A basic analytical theory. *Appl. Phys. Lett.* **104** (2014b) 022101.
- 454 Press WH, Flannery BR, Teukolsky SA, Wetterling WT. *Numerical Recipes — The Art of Scientific*  
455 *Computing* (New York: Cambridge University Press) (1988).
- 456 Noé P, Vallée C, Hippert F, Fillot F, Raty JY. Phase-change materials for non-volatile memory devices:  
457 from technological challenges to materials science issues. *Semicond. Sci. Technol.* **33** (2017) 013002.