

Gate-Controlled Magnetotransport and Electrostatic Modulation of Magnetism in 2D Magnetic Semiconductor CrPS₄

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Using field-effect transistors (FETs) to explore atomically thin magnetic semiconductors with transport measurements is difficult, because the very narrow bands of most 2D magnetic semiconductors cause carrier localization, preventing transistor operation. Here, it is shown that exfoliated layers of CrPS₄—a 2D layered antiferromagnetic semiconductor whose bandwidth approaches 1 eV—allow the realization of FETs that operate properly down to cryogenic temperature. Using these devices, conductance measurements as a function of temperature and magnetic field are performed to determine the full magnetic phase diagram, which includes a spin-flop and a spin-flip phase. The magnetoconductance, which depends strongly on gate voltage, is determined, reaching values as high as 5000% near the threshold for electron conduction. The gate voltage also allows the magnetic states to be tuned, despite the relatively large thickness of the CrPS₄ multilayers employed in the study. The results show the need to employ 2D magnetic semiconductors with sufficiently large bandwidth to realize properly functioning transistors, and identify a candidate material to realize a fully gate-tunable half-metallic conductor.

1. Introduction

Atomically thin van der Waals (vdW) semiconducting magnets (i.e., 2D magnets) exhibit phenomena resulting from the interplay between semiconducting and magnetic functionalities, absent in other material platforms.^[1–3] Recently reported examples include the observation of a strong electric field modulation of the spin-flip field in CrI₃ bilayers,^[4,5] of the dependence of the luminescence wavelength on the magnetic state of CrSBr,^[6] and of giant tunneling magnetoresistance of barriers made of 2D magnetic multilayers.^[7–12] Theory predicts more phenomena that remain to be observed, such as the possibility to create gate-tunable half-metallic conductors by populating fully spin-polarized bands of 2D semiconductors.^[13–15] Experiments, however, have been drastically limited by the extremely narrow bandwidths of most

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2D magnetic semiconductors explored so far (frequently ≈ 100 meV),^[16,17] which causes these materials to behave very differently from conventional high-quality semiconductors such as Si or GaAs. Indeed, in narrow bandwidth semiconductors Coulomb interactions and disorder potentials easily exceed the kinetic energy of charge carriers, often resulting in their localization. To progress, it is essential to identify 2D semiconducting compounds with the largest possible bandwidth.

These considerations are particularly pertinent for the realization of field-effect transistors (FETs) enabling gate-tunable transport measurements well below the magnetic transition temperature T_C . For the majority of 2D magnets investigated so far (e.g., chromium trihalides,^[7–12] MnPS₃^[18]), either no transistor action was observed, or the devices were found to exhibit extremely poor characteristics and to function exclusively for $T > T_C$. In materials such as VI₃ or Cr₂Ge₂Te₆ the bandwidth is slightly larger (a few hundreds meV^[19] and 0.5 eV,^[20,21] respectively) and clear transistor action is seen, but even then experiments are drastically limited by the device quality.^[22–25] Very recently, CrSBr—whose bandwidth exceeds 1.5 eV^[6,26]—and NiI₂—whose bandwidth is estimated to be 0.8–1 eV^[27]—enabled the first realization of FETs operating down to cryogenic temperature,^[26,28] confirming that a large bandwidth is indeed key to observe gate-induced in-plane transport at low-temperatures in these systems. However, in neither of these two compounds electrostatic modification of their magnetic phase boundaries has been reported. Currently, therefore, identifying more 2D magnetic semiconductors with a sufficiently large bandwidth to realize FETs enabling the magnetic state of 2D magnetic semiconductors to be probed—and possibly controlled—remains a key target.

Here, we explore CrPS₄—a 2D semiconducting layered antiferromagnet, whose bandwidth approaches 1 eV—to show experimentally that FETs based on this material operate properly up to the lowest temperature reached in our experiments ($T = 250$ mK), and to demonstrate that the magnetic state of the material can be tuned by acting on the gate voltage V_G . Measurements at fixed V_G show that the dependence of the device conductance on temperature and applied magnetic field enables the boundaries between the different magnetic states of CrPS₄ to be precisely determined. With magnetic field applied perpendicular to the layers, the magnetoconductance exhibits clear features associated to the spin-flop and spin-flip transitions $\mu_0 H \approx 0.6$ T and 8 T, at $T = 2$ K, respectively—that shift to smaller fields upon increasing T , before eventually disappearing for $T = T_N$ (the Néel temperature of CrPS₄ multilayers, $T_N \approx 35$ K). When the field is applied parallel to the layers, the behavior and magnitude of the magnetoconductance are similar, except for the absence of the spin-flop transition (as expected, since in CrPS₄ the easy axis is perpendicular to the layers). The dependence of transport on V_G shows the possibility to drastically increase the magnetoconductance, which exceeds 5000% as V_G approaches the threshold voltage. A shift of the spin-flip and spin-flop fields, as well as of T_N , is also unambiguously detected, signaling that the magnetic state can be gate-tuned. Besides confirming that large bandwidth 2D magnetic semiconductors enable the magnetic state of 2D magnetic semiconductors to be probed by means of magnetotransport and to be tuned electrostatically, our results identify a first viable experimental candidate for the realization of a gate tunable half-metallic conductor.

2. Results and Discussion

CrPS₄ crystallizes into a monoclinic structure formed by the vdW stacking of distorted CrS₆ octahedra and PS₄ tetrahedra as shown in Figure 1a.^[15,29–34] It is an air-stable, weakly anisotropic layered antiferromagnet with an easy axis perpendicular to the layers.^[32,35,36] The Néel temperature— $T_N = 38$ K in bulk crystals—is somewhat reduced in atomically thin exfoliated multilayers.^[32,35,36] Band structure calculations for the antiferromagnetic and ferromagnetic spin configurations of the material (see Figure 1b,c) show that the conduction band is fully spin-polarized in the ferromagnetic state and in individual monolayers, potentially enabling the realization of a fully gate-tunable half-metallic conductors if gate-induced transport at low temperature can be achieved.^[15] Most importantly, the calculations also show that the conduction band disperses by approximately 1 eV, which is the main reason for us to select this system to nanofabricate FET devices.

CrPS₄ crystals purchased from HQ Graphene are characterized by energy-dispersive X-ray and Raman spectroscopy (see Supporting Information), then exfoliated with an adhesive tape, and transferred onto doped silicon substrates covered with a 285 nm-thick thermally grown oxide layer (see Figure 1d). Using by now conventional pick-up and transfer techniques,^[37] selected exfoliated layers are placed onto bottom multilayer graphene strips acting as source and drain electrodes, and encapsulated between 20 and 30 nm-thick h-BN crystals. Even though the material is air-stable, exfoliation, transfer and encapsulation are performed in a glove-box with sub-ppm concentration of oxygen and water to maximize the quality of the final device. The structures are then taken out of the glove-box and metal contacts are attached to the graphene strips by means of electron beam lithography, reactive ion etching of the top hBN layer with a CF₄/O₂ mixture, electron beam evaporation of a Cr–Au film (20/30 nm), and lift-off. An optical microscopy image of one of our devices is shown in the inset of Figure 1e. We realized devices containing multiple transistors on 4 different exfoliated CrPS₄ multilayers, with thickness in the 6–11 nm range (as determined by atomic force microscopy), all exhibiting comparable behavior.

Multilayer CrPS₄ FETs exhibit transfer curves (conductance G vs V_G) typical of n-type semiconductors, as shown in Figure 1e with data measured on a 10 nm-thick device, whose behavior is representative of that of all transistors investigated in our work (all data shown in the main text have been measured on this same 10 nm device; data from another device are shown in Supporting Information to illustrate that our observations are reproducible). The relatively small threshold ($V_{th} = +10$ V) indicates that the Fermi level is located close to the conduction band edge, due to unintentional dopants present in the material. The field-effect (two-probe) mobility estimated from the room-temperature transconductance ($\partial G/\partial V_G$) of this device is 0.2 cm² V⁻¹ s⁻¹. Other devices exhibit values reaching up to 1 cm² V⁻¹ s⁻¹, comparable to values reported in CrSBr and NiI₂ transistors, where measurements were performed in a four-probe configuration.^[26,28] The output characteristics (source–drain current I versus applied bias V , measured for different V_G) are rather linear at room temperature (see Figure 1f), but upon cooling the behavior changes: the threshold voltages shift to larger positive values (as expected

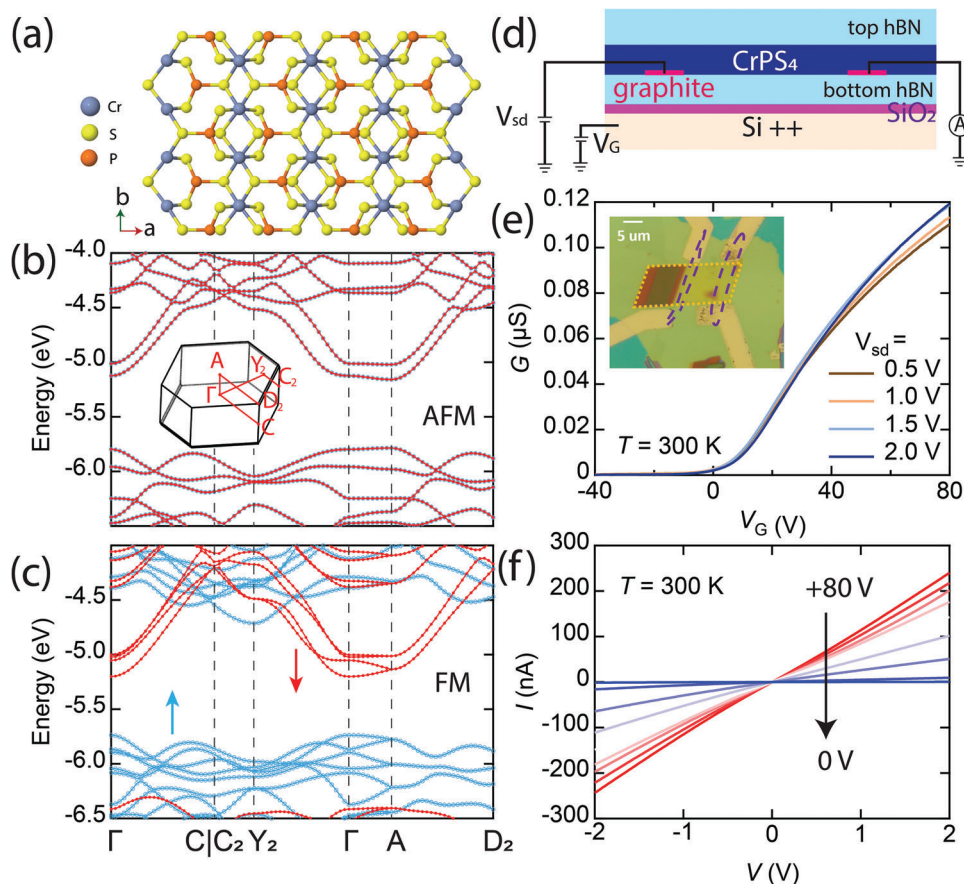


Figure 1. Properties and device characterization of CrPS₄ FETs. a) Crystal structure of layered semiconductor CrPS₄. The blue, yellow, and orange balls represent Cr, S, and P atoms, respectively. b,c) First-principles calculations of the band structure of bulk CrPS₄ in antiferromagnetic and ferromagnetic ground state, respectively. The same (doubled) unit cell is adopted for both FM and AFM states for ease of comparison. Lines connecting filled red circles and empty blue circles represent spin-up and spin-down states. The inset shows the Brillouin zone and the high-symmetry path along which the bands are computed. d) Schematic representation and electrical circuitry of our CrPS₄ FETs. CrPS₄ is encapsulated with top and bottom hBN and electrical contact to the crystal is provided by inserting few-layer graphene stripes in the stack. e) Room temperature transfer curves of a CrPS₄ FET under biasing conditions indicated in the legend. The sublinear shape of the curve indicates the presence of a contact resistance (the carrier mobility and subthreshold swing extracted from the transfer curve are 0.2 cm² V⁻¹ s⁻¹ and 4 V per decade, respectively). The inset shows an optical microscopy image of the device (the CrPS₄ layer is 10 nm thick). The yellow dashed lines delimit the CrPS₄ crystal and the graphene electrodes are delimited by the purple dashed lines. f) Room-temperature *IV*-characteristics for gate voltages ranging from +80 to 0 V in 10 V steps.

for a doped semiconductor; **Figure 2a**), and a pronounced non-linearity of the output characteristics becomes apparent (see **Figure 2b**; data measured at $V_G = +80$ V), indicating the presence of a contact resistance. For applied biases $V_{SD} > 1.0$ V, however, the contacts appear not to influence significantly the measurements, as the extracted electron mobility becomes almost bias independent (see **Figure S3**, Supporting Information; at low temperature the mobility measured at $V_{SD} > 1.0$ V ranges between 1 and 4 cm² V⁻¹ s⁻¹ depending on the device, again comparable to values extracted from four-terminal measurements in CrSBr and NiI₂^[26,28]). We conclude that the quality of our CrPS₄ transistors is comparable to that of similar devices recently reported on CrSBr and NiI₂, and that it is amply sufficient to allow transport to be measured to temperatures much lower than T_N , and to be gated continuously. This conclusion confirms the need to select 2D magnetic semiconductors with sufficiently large bandwidth for the realization of transistors properly functioning at low temperature.

The onset of the magnetically ordered state in CrPS₄ is clearly visible in the transistor conductance measured as a function of T , at fixed V_G . Upon cooling down the devices from room temperature, the conductance decreases slowly (as carriers freeze out into the dopants where they originate from [38]), before exhibiting an abrupt increase as T is lowered just below the Néel transition (see **Figure 2c**). The abrupt increase results from the transition into the layered antiferromagnetic state that occurs at $T_N \approx 35$ K (as determined by the position of the minimum of dG/dT in **Figure 2c**), slightly lower than the value of T_N in bulk CrPS₄ crystals, confirming the trend demonstrated in recent magneto-optical studies that the critical temperature of CrPS₄ decreases with decreasing thickness of the crystal.^[36] The observed conductance increase below T_N is due to the onset of long-range spin ordering that suppresses disorder associated to spin fluctuations within each CrPS₄ layer. At $V_G = +80$ V the effect is sizable, as the conductance increases by more than a factor of 3 before eventually decreasing again and saturating at low temperature.

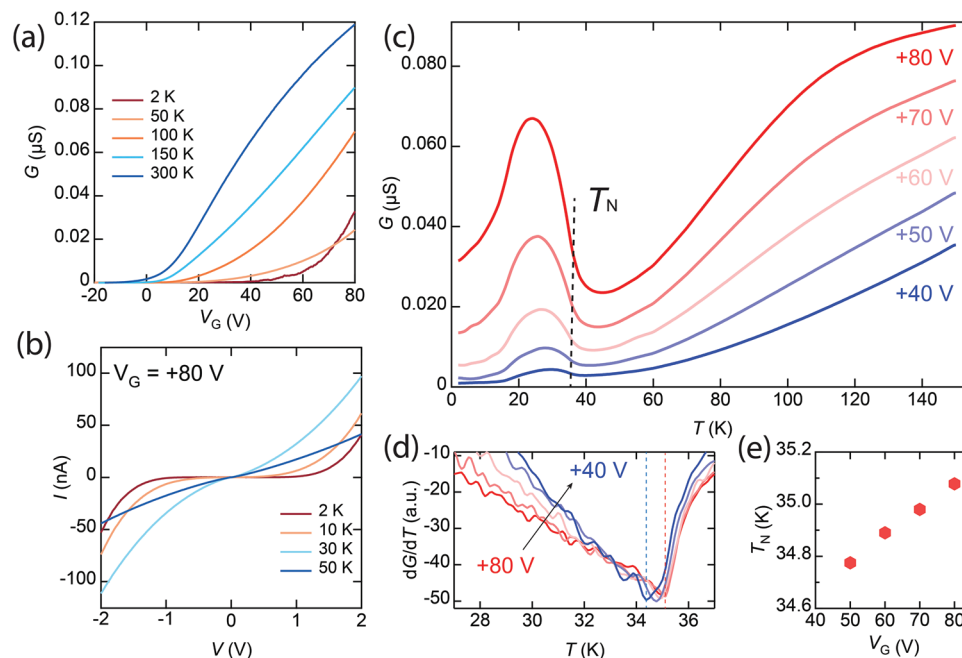


Figure 2. Temperature-dependent transport in CrPS₄ FETs. a) Transfer curves of a CrPS₄ FET at selected temperatures indicated in the legend. b) Low-temperature output characteristics measured at fixed $V_G = +80$ V and selected temperatures of $T = 2, 10, 30,$ and 50 K. c) Conductance as a function of temperature measured at selected V_G values (from $+40$ to $+80$ V in 10 V steps) with fixed source–drain bias $V_{SD} = 2$ V to eliminate the effect of the contact resistance present at low bias. The onset of magnetic order coincides with a sharp conductance increase. The dashed line marks the Néel temperature T_N . d) Derivative of the conductance as a function of temperature for the same gate voltages shown in (c). The Néel transition temperatures is determined from the position of the minimum in dG/dT . Measurements at different V_G between $+40$ and $+80$ V exhibit a small but unambiguous shift of transition temperature. e) Dependence of the Néel temperature T_N on V_G , extracted from (d). For the $V_G = +40$ V trace, the transistor is in the subthreshold regime, and the small current prevents a reliable quantitative determination of T_N .

Whether the sizable increase in conductance upon passing from the paramagnetic to the antiferromagnetic state implies that the devices should also exhibit sizable magnetoconductance $\delta G = (G(H) - G(0))/G(0)$ (since an applied magnetic field can modify the magnetic state of the material) is not clear a priori. Large magnetoconductance in magnetic materials commonly occurs when the current flows across regions with spatially inhomogeneous magnetization (such as domain walls,^[39–41] spin valves,^[42,43] tunnel barriers made of layered antiferromagnetic insulators,^[7–12] etc.). This is not the case in our FETs, since the current in the transistor channel propagates parallel to the CrPS₄ layers, and the magnetization of each layer is uniform at low temperatures. Another known mechanism that—by analogy—may seem relevant for our devices is the one responsible for the magnetoconductance of metallic magnetic multilayers.^[44–46] When current flows parallel to the layers, the conductance is typically higher in the ferromagnetic state (i.e., when all layers are magnetized in the same direction) than in the antiferromagnetic one (when adjacent layers are magnetized in opposite directions), because the different scattering rates of majority and minority spin electrons result in a different electron mobility in the two magnetic states.^[47] This mechanism normally leads to magnetoconductance values well below 100% (i.e., changes that are less than a factor of two), that is, smaller than the change that associated to the transition from the paramagnetic to the antiferromagnetic state upon lowering T (with $V_G = +80$ V see Figure 2c). There is therefore no established mechanism suggesting that a very

large magnetoconductance should be observed in CrPS₄ FETs for $T < T_N$, and indeed, recent measurements on FETs based on CrSBr and NiI₂^[26,28]—which are also 2D semiconducting layered antiferromagnets—have shown only a modest magnetoconductance (well below a factor of two).

Figures 3 and 4 show that—in contrast to CrSBr and NiI₂ transistors—CrPS₄ FETs do exhibit a very large magnetoconductance, which appears upon cooling, as the Néel temperature is approached. The large magnetoconductance (see Figure 3a,b) observed above and just below the critical temperature originates from spin fluctuations, because in this temperature range (i.e., in the paramagnetic state or in the antiferromagnetic one, when magnetic order is not yet fully developed) the magnetic susceptibility is largest, so that the applied magnetic field is most effective in polarizing the spins and thereby in reducing spin-induced disorder.^[48] What is however more surprising and unexpected—because far below T_N the magnetic state is robust and spins not easily polarizable—is that upon lowering the temperature further, the magnetoconductance remains large. Irrespective of whether the magnetic field is applied perpendicular or parallel to the layers, the magnetoconductance reaches values as large as a factor of 50 (i.e., 5000%, see Figure 3a,b), for an applied magnetic field $\mu_0 H = 10$ T, and is gate tunable (the extremely strong, nearly exponential, dependence of δG on V_G is shown in Figure 4b). Finding that the large magnetoconductance persists when the field is applied in the plane of CrPS₄—in conjunction with the low electron mobility—implies that the orbital effects of

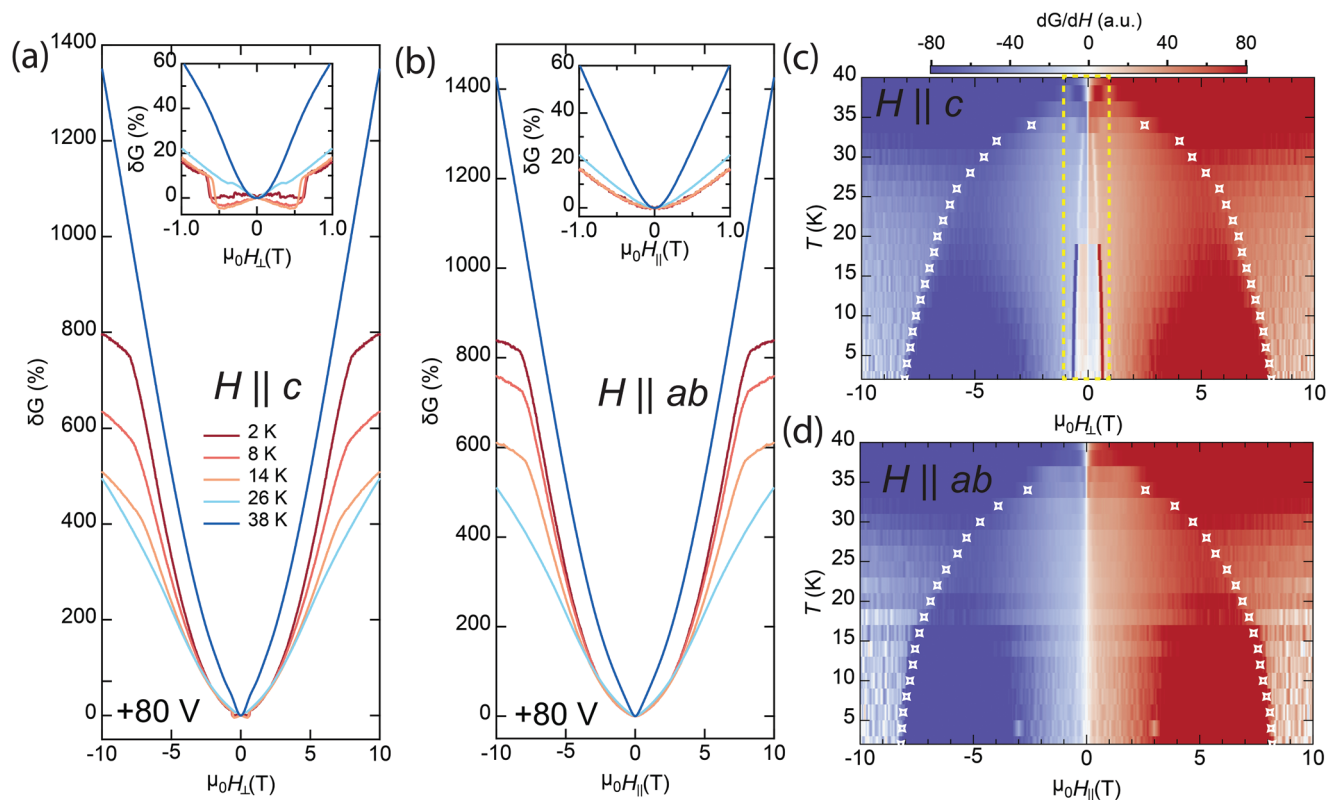


Figure 3. Magnetic phase diagram of CrPS₄. a,b) Magnetoconductance ($\delta G = (G(H) - G(0))/G(0)$) measured at $V_G = 80$ V, $V_{sd} = 2$ V and $T = 2, 8, 14, 26,$ and 38 K, as a function of magnetic field applied respectively perpendicular and parallel to the basal planes. The sharp saturation of the magnetoconductance at high field is due to the spin-flip transition occurring at $\mu_0 H \simeq 8$ T at low temperature. The insets zoom-in on the low field range ($\mu_0 H$ between -1 and 1 T), where the spin-flop transition is visible when the magnetic field is applied perpendicular to the crystalline planes (inset of (a)). c,d) Color plot of dG/dH as a function of temperature and magnetic field applied out-of and in-plane, respectively. The white open symbols mark the spin-flip transition. The yellow dashed box in (c) delimits the region around the spin-flip transition.

the magnetic field (as well as the influence of the graphene contacts) are not the reason for the observed large magnetotransport response. Indeed, the experiments indicate that the large magnetoconductance originates from the magnetic-field induced modifications of the magnetic state of CrPS₄.

To illustrate the relationship between magnetoconductance and magnetic state we start by discussing Figure 3c,d, where we plot the derivative of the conductance dG/dH as a function of field and temperature. For perpendicular fields (Figure 3a,c), two distinct features are observed. First, for T well below T_N the conductance exhibits a kink and stops increasing rapidly above approximately 8 T (see Figure 3a). The phenomenon originates from the spin-flip transition, above which all spins fully align along the applied field (in the color plot of dG/dH in Figure 3c, the transition—marked by the white diamonds—manifests itself in a more pronounced way, and can be followed all the way up T_N). The second feature is a smaller, but clearly distinct change in magnetoconductance at much lower field ($\mu_0 H \simeq \pm 0.6$ T at $T = 2$ K), shown in the inset of Figure 3a, and clearly apparent in the region delimited by the yellow dashed line in Figure 3c. It is a manifestation of the spin-flop transition that occurs because CrPS₄ is a weakly anisotropic layered antiferromagnet. The color plot of dG/dH in Figure 3c illustrates clearly how the spin-flip and spin-flop fields decrease as the temperature is increased, and

eventually vanish at approximately 35 K, that is, the Néel temperature T_N of the material. Similar considerations can be made by looking at Figure 3b,d, when the magnetic field is applied parallel to the layers, but in that case no spin-flip transition is observed (as expected, since the easy axis of CrPS₄ is perpendicular to the layers). Measuring the magnetoconductance of our FETs, therefore, allows us to trace the complete magnetic phase diagram of CrPS₄ multilayers, and even to identify features that are often complex to detect experimentally in atomically thin layers (such as the spin-flop transition, which has not been detected in any exfoliated 2D magnet by means of magneto-optics experiments, the technique possibly the most commonly employed to study magnetism in these systems).

Having established the ability to map the magnetic phase diagram through magnetoconductance measurements, we analyze whether the different magnetic states can be influenced electrostatically, by varying the voltage applied to the gate. A strong effect is only expected in devices realized with crystals that are one or few layers thick because electrostatic screening forces the charge accumulated in the transistor channel to reside exclusively in the first few layers next to the gate electrode (in the range of accumulated electron densities—a few 10^{12} cm⁻²—the screening length is approximately 1 nm, which is why most charges are accumulated in the first CrPS₄ layer next to the

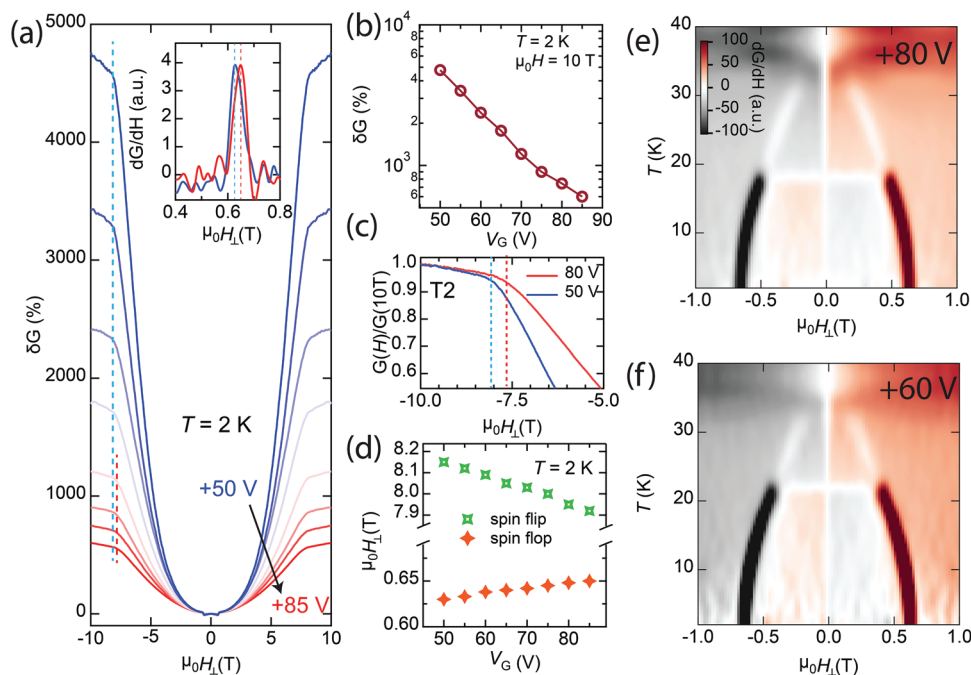


Figure 4. Gate modulation of magnetotransport and of the magnetic state of CrPS₄. a) Magnetoconductance measured at $V_{sd} = 2$ V and $T = 2$ K for different values of V_G between +50 and +85 V. The blue and red dashed lines indicate the onset of saturation of δG occurs at slightly different magnetic field at $V_G = +50$ and +85 V, showing that the spin-flip transition can be tuned electrostatically. The inset shows the derivative of the magnetoconductance in the 0.4–0.8 T range, with the peak corresponding to the spin-flop transitions field. Data taken at $V_G = +50$ V (blue line) and +85 V (red line) show that the spin flop transition shifts by approximately 20 mT upon varying V_G . b) Gate voltage dependence of the magnetoconductance value at 10 T, showing a nearly exponential dependence of δG on V_G . c) $G(H)/G(10T)$ measured at $T = 2$ K on another device based on a 10 nm CrPS₄ exfoliated multilayer, zooming in on the shift of the spin-flip field when increasing V_G from 50 V (blue line) to 80 V (red line). d) Gate dependence of the spin-flip (open green symbols) and spin-flop (open orange symbols) transition fields. Data measured at $T = 2$ K. e, f) Zoom-in on the spin-flop transition region in the color plot of dG/dH measured at $T = 2$ K, for $V_G = +60$ and +80 V, respectively. Besides the shift of the spin-flop field (see inset of (a)), also the details of the magnetoconductance along the phase boundary exhibit a pronounced influence on the gate voltage, with the temperature at which dG/dH changes sign that varies by nearly 5 K as V_G varies from +60 to +80 V. The effect, whose origin remains to be understood, further illustrates the electrostatic tunability of the magnetic properties of CrPS₄ multilayers.

gate). Nevertheless—despite our devices being 10-to-20 monolayers thick—magnetoconductance measurements unambiguously show that systematic gate-induced changes in the magnetic state are present. To demonstrate this conclusion, we focus on specific points of the boundaries between the different magnetic phases that can be precisely determined, and look at their evolution upon varying V_G .

First clear evidence for the modification of the CrPS₄ phase boundaries by the electrostatic gate is seen in the critical temperature T_N at zero applied magnetic field, which experimentally can be precisely determined by looking at the position of the minimum in dG/dT (Figure 2d). Upon varying V_G from +50 to +80 V, the minimum in dG/dT —and hence T_N —increases by approximately 0.5 K (Figure 2e; in the different devices that we measured the change ranges between 0.5 and 1 K, see for instance Figure S5 (Supporting Information) for data from another transistor. Varying the gate voltage also affects the spin-flip transition field, which decreases by about 0.3 T when the gate is changed in approximately the same range at $T = 2$ K (see the blue and red dashed line in Figure 4a,c), and modulates the spin-flop transition as well (compare Figure 4e,f): the magnetoconductance along the phase boundary changes and the spin-flop field increases by approximately 20 mT as V_G is increased from +50

to +85 V (see the inset of Figure 4a). The evolution of both transitions as a function of gate voltage is summarized in Figure 4d. Since, at the simplest level, the spin-flip field is proportional to the interlayer exchange interaction J , and the spin-flop field to \sqrt{JK} (where K is the magnetic anisotropy),^[49] finding that these two quantities change in opposite directions (the first decreases whereas the second increase as V_G is increased) implies that both J and K are affected by the gate voltage.

Finding that CrPS₄ FETs allow controlling the magnetic state electrostatically and probing the resulting changes by transport measurements is worth emphasizing because the only 2D magnetic semiconductors on which continuous FET operation could be achieved at low temperature so far (CrSBr^[26] and NiI₂^[28]) did not exhibit any modulation of the magnetic phase boundaries upon varying the gate voltage. Indeed, among all 2D magnetic semiconductors studied, only in mono- and bilayers of CrI₃ a continuous gate-tuning of the magnetic state has been observed, by means of magneto-optical techniques.^[4,5] In that case, all layers were affected by the gate-accumulated (reaching up to 10^{13} cm⁻²)—owing to the atomic thickness of the material—and for monolayer CrI₃, a 10 K gate-induced change in critical temperature was reported.^[5] In our transistors the effect is somewhat smaller, probably because the charge is accumulated predomi-

nantly in the individual layer closest to the gate electrode, but the CrPS₄ multilayers are 10-to-20 layers thick, and we expect that in devices based on CrPS₄ mono- or bilayers a stronger dependence of the magnetic state on gate voltage will be observed. Exploring how the magnetic state depends on thickness and how thin multilayers are influenced by charge accumulation is certainly worth addressing in future work, to reveal the microscopic mechanism through which charge accumulation modifies magnetism that is currently unknown.

3. Conclusion

The ability to accumulate electrostatically charge carriers at the surface of 2D magnetic semiconductors to induce electronic transport and control the magnetic state discloses opportunities for future experiments targeting unexplored phenomena. Identifying the microscopic mechanism responsible for the interplay between transport electrons and the magnetic state reported here—causing the magnetoconductance to reach values up to 5000%—provides a first clear objective. More in general, the occurrence of gate-induced low-temperature transport in CrPS₄ enables a much broader variety of experiments to be done, for instance in multiterminal devices (e.g., to search for the anomalous Hall effect and investigate its gate dependence), in devices based on few-layer crystals (where the influence of gating on the magnetic state is expected to be much stronger), and in monolayers (where it will be possible to realize gate-tunable half-metallic conductors). Of great interest is also the implementation of local gates, to control the magnetic state locally in different parts of the device (to explore, for instance, whether the presence of interfaces between different magnetic states within the transistor channel allows the magnetoconductance to be increased even further). It should be realized, however, that the scope of possibilities is much broader, because CrPS₄ is only the first large-bandwidth magnetic 2D semiconductor that enables the realization of transistors properly functioning at low temperature. We envision that many more 2D magnetic semiconductors with bandwidth comparable to (or larger than) that of CrPS₄ will be introduced in the future, hosting a rich variety of magnetic states, providing experimental access to an even much broader variety of interesting physical phenomena.

4. Experimental Section

Sample Fabrication: CrPS₄ multilayers were obtained by exfoliating bulk crystals, purchased from HQ Graphene, onto 285 nm-thick SiO₂ grown on heavily doped silicon wafers in a nitrogen-gas-filled glove box, with sub-ppm oxygen and water concentration to exclude any degradation and maximize the quality of the final device. The multilayer thickness was determined by means of atomic force microscopy. The multilayers were contacted electrically with few-layer graphene stripes and encapsulated with exfoliated hBN layers between 20 and 30 nm thick, employing a conventional pick-up and release technique based on PC/PDMS polymer stacks placed on glass slides. A total of four devices have been fabricated and the graphene stripes contacted with metallic electrodes (Cr/Au: 10/40 nm), using a conventional process based on electron-beam lithography, reactive ion etching, electron-beam evaporation, and lift-off.

Transport Measurements: All transport measurements were performed in a Heliox 3He insert system (Oxford Instruments) equipped with a 15 T superconducting magnet. A Keithley 2400 source/measure was used to

apply the gate voltage to the transistors. The bias voltage was applied using a homemade low-noise source. The current and voltage signals were amplified with homemade low-noise electronics and the amplified signals were recorded with an Agilent 34410A digital multimeter unit.

DFT Calculations: First-principles simulations were performed using the Quantum ESPRESSO distribution.^[50,51] To account for van der Waals interactions between the layers, the spin-polarised extension^[52] of the revised vdW-DF-cx exchange-correlation functional^[53,54] was adopted, which gives lattice parameters in good agreement with experiments. The Brillouin zone was sampled with a 6 × 6 × 3 Γ -centered Monkhorst–Pack grid, considering a doubled unit cell in the vertical direction (containing 24 atoms) both in the ferro- and antiferromagnetic configurations. Pseudopotentials were taken from the Standard Solid-State Pseudopotential (SSSP) accuracy library (v1.0)^[55] with cutoffs of 40 Ry and 320 Ry for wave functions and density, respectively. Atomic positions and lattice parameters were relaxed, reducing forces and stresses below thresholds of 3 meV Å⁻¹ and 0.5 kbar, respectively. The band structure was computed along a high-symmetry path obtained by selecting the most interesting directions provided by SeekPath.^[56]

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are openly available in Yareta at <https://doi.org/10.26037/yareta:ciakqdhfdne35dyn6le54ns0y4>.

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