Thermo-Electrical Digital Twin-Assisted Aging Assessment of SiC MOSFETs in Switching-Cell-Array Power Converters

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***Abstract*—Accurate aging assessment of switching power semiconductors in power converters is essential due to their critical influence on converter reliability and operational lifespan. Traditional aging evaluation methods rely on intrusive sensors embedded within the power devices, which complicate electromagnetic interference management and limit the practicality of real-time monitoring. This paper proposes a comprehensive digital-twin framework and a simple algorithm to assess the state of health (SOH) of SiC power devices in switching-cell-array based power converters. The digital twin replicates the system electro-thermal behavior from the existing converter control current and voltage measurements and the modulation parameters. The algorithm estimates the power devices on-state resistance through the digital twin outputs and easy-to-integrate temperature sensors within the converter leg printed-circuit board. The on-state resistance provides a direct estimation of the power devices SOH. This framework delivers real-time insights into the converter SOH and degradation patterns, allowing predictive maintenance strategies. The proposed health assessment strategy is validated through simulations.**

Keywords*—*SiC MOSFET, digital twin, switching-cell array, state of health, aging assessment

I. Introduction

Reliability in power converters is critical due to the high cost of failures. The Switching-Cell Array (SCA) design enhances reliability by building converters from modular Switching Cells (SCs), each with a power device and driver. These SCs form multilevel NPC legs, enabling voltage/current scaling and improving efficiency over traditional two-level designs [1].

SCA-based converters improve fault tolerance using redundant switching states and features like the iFuse, which isolates failed SCs while maintaining operation [2]. Reliability is further boosted by distributing stress both topologically (placing SCs in high-loss spots) and via control (selectively switching SCs), balancing thermal profiles and reducing aging [3].

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Advanced control strategies can shift stress from aged SCs to healthier ones, using state-of-health (SOH) monitoring. Traditional methods track thermal/electrical indicators like junction temperature or saturation voltage, which correlate with degradation but add cost and EMI concerns [4] [5]. To reduce intrusiveness, alternatives like infrared thermography and gate charge analysis offer easier deployment with trade-offs in precision [6] [7].

Machine learning (ML) enhances RUL prediction by analyzing voltage/current/temperature data to detect aging trends, though generalization can be limited [8][9]. Digital twins (DTs), combining physics-based models with ML and real-time sensing, offer robust fault detection and predictive maintenance. Nowadays, their high computation requirements are met by modern field-programmable gate arrays and multicore computing units [10] [11].

SiC metal-oxide semiconductor field-effect transistor (MOSFET) on-state resistance (R_{on}) degrades with thermal cycles, bias stress, and mobility loss, affecting efficiency and complicating modeling [12]. R_{on}'s sensitivity to factors like electron mobility and dielectric properties demands advanced monitoring and packaging to ensure reliable operation [13].

To simplify power converters online health assessment, this paper proposes a SOH calculation method of SiC MOSFET in SCA converters through an estimation of its on-state resistance with a DT model comprising the electro-thermal model of the SCA and cooling system. The remainder of the paper is organized as follows: Section II introduces the thermo-electrical DT model for SCA converters. Section III presents the implementation of the DT framework for aging assessment of SiC MOSFETs, and Section IV provides the simulation validation. Section V is the conclusion and outlook.

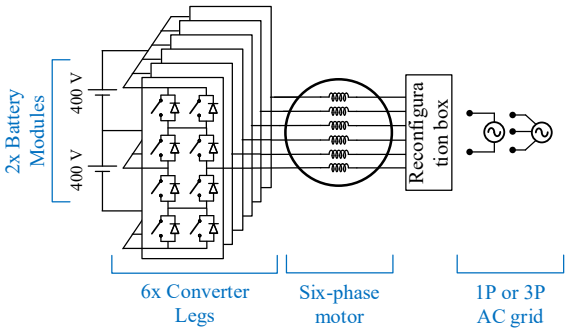
II. Thermo-Electrical DT Model for SCA Converters

This section presents a DT model for SiC MOSFET-based converters by examining three key elements. First, it introduces the power-losses model for the considered SiC power device, the C3M0015065K MOSFET from WolfSpeed Inc. Next, it discusses the SCA converter and operation.

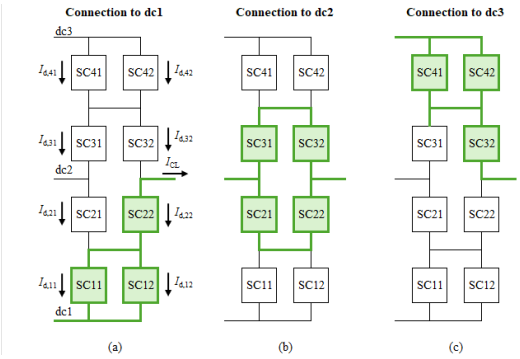
Finally, it explains the CL thermal model, focusing on the heat-flow paths and SC electrical losses model.

A. Electrical Model of the SCA Converter

In the framework of project SCAPE, partners have developed a powertrain architecture featuring SCA technology, consisting of an integrated inverter-charger (IIC), featuring a three-level NPC hexaphase dc-ac converter connected to an hexaphase open-ended electrical ac motor, as shown in Fig. 1(a). The IIC can either operate as traction inverter or on-board charger by properly configuring the motor open connections. The converter is operated by employing the virtual-vector pulse-width modulation (VVPWM) [14] adapted to the hexaphase case.



(a). Powertrain architecture with detail on the IIC topology.



(b). Switching states of a given converter leg in the IIC

Fig. 1. EV powertrain developed in project SCAPE.

Fig. 1(b) shows the switching states to connect the output of the CL to the three dc-link points (dc1, dc2, and dc3). SCs in on state and current paths shown in green. Three parallel conduction paths can be identified: SC11//SC12, SC21+SC22//SC31+SC32, and SC41//SC42, where the "+" sign indicates a series connection and "//" a parallel connection. The SC MOSFET on-state resistance ($R_{on,rc}$), where $r \in \{1, 2, 3, 4\}$ and $c \in \{1, 2\}$ are the row and column number occupied by the SC in the SCA CL (see Fig. 1(b)), are used to calculate the current flowing through each MOSFET ($I_{d,rc}$) as a function of the CL output current (I_{CL}, see Fig. 1(b)). The current on the conducting MOSFETs for connection to dc1 is

$$\begin{aligned} I_{d,11} &= -I_{CL} \cdot (1 - k_1) \\ I_{d,12} &= -I_{CL} \cdot k_1 \\ I_{d,22} &= -I_{CL}, \end{aligned} \tag{1}$$

for dc2 is

$$\begin{aligned} I_{d,21} = -I_{d,22} &= I_{CL} \cdot (1 - k_2) \\ I_{d,31} = I_{d,32} &= I_{CL} \cdot k_2, \end{aligned} \tag{2}$$

and for dc3 is

$$\begin{aligned} I_{d,41} &= I_{CL} \cdot (1 - k_3) \\ I_{d,42} &= I_{CL} \cdot k_3 \\ I_{d,32} &= I_{CL}, \end{aligned} \tag{3}$$

where

$$k_1 = \frac{R_{on,11}}{R_{on,11} + R_{on,12}}$$

$$k_2 = \frac{R_{on,21} + R_{on,22}}{R_{on,21} + R_{on,22} + R_{on,31} + R_{on,32}} \tag{4}$$

$$k_3 = \frac{R_{on,41}}{R_{on,41} + R_{on,42}}$$

B. Power Losses Model of SiC MOSFET

In this section, both conduction losses and switching losses will be discussed.

When the MOSFET is on-state, conduction losses stem from the MOSFET on-state channel resistance (R_{on}) and the drain current (I_d). The on-state resistance is temperature and current dependent, with an increase of R_{on} when the MOSFET junction temperature (T_j) and drain current rise. The C3M0015065K datasheet provides data on the R_{on} dependence on the drain current and junction temperature at a gate-source voltage equal to 15 V. Using linear approximations, the on-state resistance can be expressed as

$$\begin{aligned} R_{on} &= f(T_j, I_d) \\ &= K_R + K_{RT} \cdot T_j + (K_{RI} + K_{RIT} \cdot T_j) I_d \end{aligned} \tag{5}$$

where K_R = 14.24 mΩ, K_{RT} = 30.5 μΩ/K, K_{RI} = 2.73 μΩ/A, and K_{RIT} = 0.0187 μΩ/A·K.

Conduction losses are calculated as

$$P_{cond} = I_{d,rms}^2 R_{on}, \tag{6}$$

where $I_{d,rms}$ is the root mean square (rms) value of I_d.

Switching losses are dependent on the drain current at switching time (I_d), the junction temperature, and the external gate resistance (R_G). Moreover, for the same operating conditions, switching energy losses during a turn-on and turn-off transition are different, therefore distinguishing between E_{on} and E_{off}, respectively. C3M0015065K datasheet provides the energy lost for both cases as a function of I_{sw}, R_G and T_j, showing an almost null dependency on T_j and a linear dependency between E_{on} and I_{sw} or E_{off} and I_{sw} for the considered current range ([20, 100] A). Therefore, let us set a fixed R_G value equal to 11 Ω and define a linear relationship between switching losses and the device blocking voltage (V_{DD}). Thus, the energy switching losses in a given MOSFET at switching transition number h can be approximated by

$$E_{on,h} = \left(\frac{E_{on,n}}{I_{sw,n} V_{DD,n}} \right) \cdot V_{DD} \cdot |I_d| \tag{7}$$

$$E_{off,h} = \left(\frac{E_{off,n}}{I_{sw,n} V_{DD,n}} \right) \cdot V_{DD} \cdot |I_d| \tag{8}$$

where $V_{DD,n}$ and $I_{sw,n}$ are the normalized voltage and current (equal to 400 V and 55.8 A, respectively), $E_{on,n}$ and $E_{off,n}$ are the turn-on and turn-off loss energy under those normalized conditions (597 μJ and 462 μJ, respectively). During a switching period (T_{sw}), each SC may be turned on and/or off multiple times. Thus, the power switching losses in a given SC during a switching period are

$$P_{sw} = \frac{1}{T_{sw}} \cdot \sum_{h} \left(E_{on,h} + E_{off,h} \right) \quad (9)$$

These first-order fits offer a concise and low-computing-effort method to approximate turn-on and turn-off switching losses for the C3M0015065K device.

Expressions (1) to (9), together with the expressions for the duty cycles from the VVPWM, and the measurements of the dc-link voltage and the current at the output of each CL (already available from the converter control), allow computing the MOSFETs rms and switching current. The dc-link voltage and CL output current are sampled once every switching period (T_{sw}), updating the calculations DT at the same rate. Since the output-current fundamental period is considerably larger than T_{sw}, the CL output current can be considered constant within a T_{sw}.

C. Thermal Model of SCA Converter

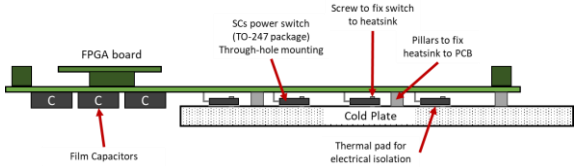
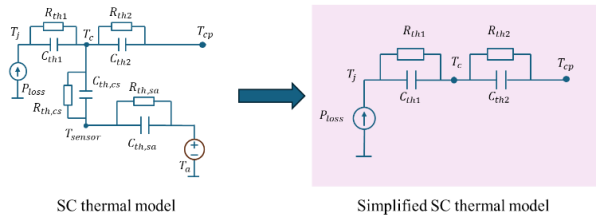
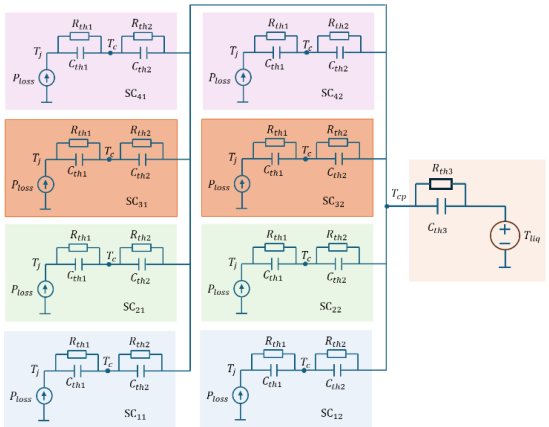


Fig. 2. Cross-section view of the CL with a liquid-cooled coldplate.

The temperature on the MOSFET is used as the key parameter for the proposed SOH assessment. For this reason, in the CL prototype currently under development in SCAPE, a temperature sensor has been placed next to the MOSFET drain connection to measure the MOSFET case temperature. Then, this measured temperature is compared to its DT counterpart. Thus, a proper thermal model of the SC and CL is required for the DT.



(a) Simplification of the SC thermal model



(b) Thermal model of the CL, including the coldplate.

Fig. 3. CL thermal model employed in the DT.

Fig. 3(a) shows the SC thermal model. It includes two thermal paths: from junction (T_j) to cold plate (T_{cp}) via resistances R_{th1} and R_{th2}, and from case (T_c) to ambient (T_a) and sensor (T_s) via $R_{th,cs}$ and $R_{th,sa}$. A thermal bond between the sensor and the drain connection (case) is ensured using thermal grease. The sensor's small footprint minimizes heat dissipation via conduction and convection. Thus, since $\{R_{th,cs}, R_{th1}, R_{th2}\} << R_{th,sa}$ and $T_s \approx T_c$. Such assumption results in the simplified SC thermal model shown on the right side of Fig. 3(a), which is based on a foster network with 2 RC elements [15], with the junction, case, and ambient temperatures (T_j, T_c, and T_a, respectively) and the SC losses ($P_{loss} = P_{cond} + P_{sw}$).

Fig. 3(b) shows the CL thermal model. The coldplate is shared between all SCs and its temperature is homogeneous across its surface. The coldplate features a thermal path to the cooling liquid characterized by thermal impedance R_{th3}, with a constant liquid temperature (T_{liq}). Thermal capacitances C_{th1}, C_{th2}, and C_{th3} allow characterizing the thermal inertia of the junction-to-case, case-to-coldplate, and coldplate-to-liquid, respectively, with $C_{th1} << C_{th2} << C_{th3}$. The differential equations characterizing the thermal network are solved with the Trapezoid method to obtain the individual temperatures.

III. Implementation of a Digital Twin Framework For SOH Assessment of SiC MOSFET

This section integrates the electrical, losses, and thermal models' data with the SC temperature sensors, and proposes an estimation algorithm for the MOSFETs on-state resistance, without requiring intrusive and complex voltage or current measurements.

A. Overall Calculation Structure Based on the DT Model

As introduced in Section I, MOSFETs' on-state resistance increases as the MOSFET degrades and leads to a rise in the MOSFET temperature. The proposed estimation process, (shown in Fig. 4) leverages on this fact by employing the described DT model of the IIC prototype. The case temperature T_c in each SC MOSFET measured by the temperature sensor T_{sensor} serves as an indicator to estimate the SCs SOH.

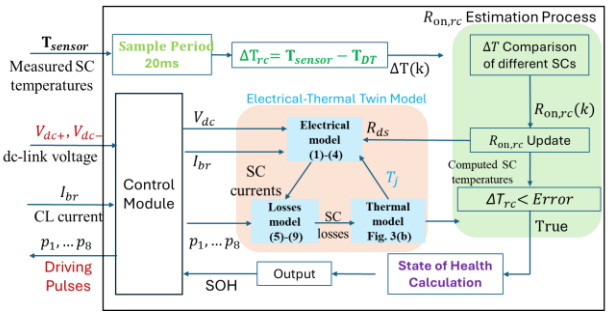


Fig. 4. Simplified view of the converter SOH estimatin algorithm.

There are three steps involved in calculating SOH. The first step is to understand the relation between the SCs degradation and their temperatures and determine the location of degraded SC in the converter. The second step is to estimate the $R_{on,rc}$ value of each degraded SC. The last step is to calculate the SOH in the SCs.

At first glance, the identification of the degraded SC might seem simple, since an increase in the SC's R_{on} leads to an increase in T_c because of the increased conduction losses. Thus, it might seem that simply computing the temperature difference between the measured SC T_c and the computed T_c with the non-degraded DT model is enough. However, the parallel conduction paths shown in Fig. 1(b) and the

degradation-induced rise of R_{on} in the SCs, cause a thermo-electrical coupling between the SCs. For instance, in the pair SC41 and SC42, an increase on $R_{on,41}$ causes a shift of the current from SC41 to SC42. This results in an increase of both SC41 and SC42 temperatures; on the former due to the R_{on} increase (albeit offset by the reduction in the current) and on the latter due to its current increase. This thermo-electrical coupling exists in SC11-SC12, SC41-SC42, and SC21-SC22-SC31-SC32. Fig. 5 shows in detail the temperature differences between the coupled SCs in these groups. Fig. 5 results also identify that a great increase in SC22 or SC32 temperatures means that these are degraded. However, a degradation of SC21 or SC31 results in a slight increase of their temperature, the temperature of the SCs in the opposite parallel conduction paths, and a slight decrease in SC32 and SC22.

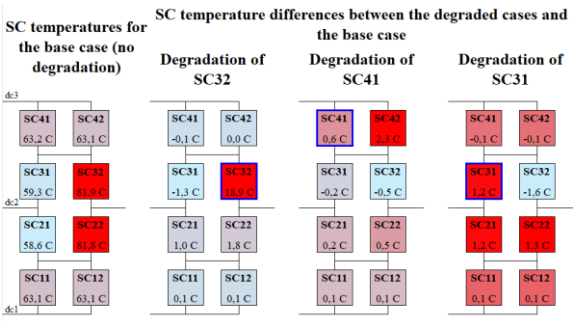


Fig. 5. Simulation results showing the SC temperatures for different SC degradations.

The above thermal pattern lets us define an algorithm that identifies the degraded SCs and estimates its R_{on} value. This algorithm is shown in Fig. 6 for groups SC11-SC12 and SC41-SC42 and in Fig. 7 for SC21-SC22-SC31-SC32 group.

B. *MOSFET On-State-Resistance Estimation Algorithm*

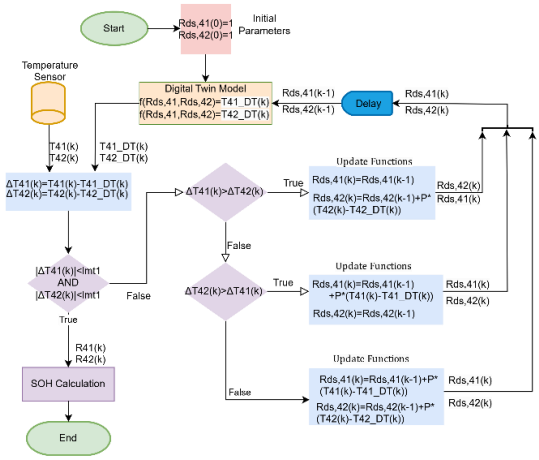


Fig. 6. $R_{on,rc}$ estimation algorithm for SC41 and SC42 (also valid for SC11 and SC12).

In Fig. 6, the estimation process consists of two stages within a while loop. On each iteration, the first stage identifies whether SC41, SC42, both or none are degraded. It performs it by computing the difference between DT model and the sensor temperatures, that is $\Delta T_{rc} = T_{rc}(k) - T_{rc,DT}(k)$, where k is the current iteration step. If any of ΔT_{41} and ΔT_{42} is over error-threshold $lmt1$, then it is considered that one or both SCs are degraded. If $\Delta T_{41} > \Delta T_{42}$, then SC42 is considered to be degraded. If $\Delta T_{41} < \Delta T_{42}$, then SC41 is degraded. If $\Delta T_{41} > lmt1$ and $\Delta T_{42} > lmt1$ then both SCs are degraded.

On the second stage, the estimation of $R_{on,rc}$ is performed for those SCs that have been identified as degraded, following

$$R_{on,rc}(k) = R_{on,rc}(k-1) + P_{SC} \cdot \Delta T_{rc}(k) \qquad (10)$$

where P_{SC} is a proportional parameter and $k-1$ is the previous time-step index.

The DT then calculates the DT-model temperatures $[T_{41,DT}(k), T_{42,DT}(k)]$ using the updated resistance values $[R_{on,41}(k), R_{on,42}(k)]$ and the algorithm starts a new iteration. The algorithm continues until both ΔT_{41} and ΔT_{42} converge to $lmt1$. The computed R_{on} value in the ending sampling period (end) $[R_{on,41}(end), R_{on,42}(end)]$ are the estimated SCs R_{on} values, employed to compute the SCs SOH. The same method applies to SC11 and SC12.

In the algorithm for SC21-SC22-SC31-SC32 group (Fig. 7), two stages are used to decouple the interaction between [SC31, SC21] and [SC32, SC22]. The first step involves identifying whether SC32 or SC22 are degraded following:

- If $\Delta T_{32}(k) > lmt2$, then $R_{on,32}$ is degraded.
- If $\Delta T_{22}(k) > lmt2$, then $R_{on,22}$ is degraded

Then, the R_{on} value of SC22 and SC32 are updated following (10).

The DT model then calculates the temperatures $[T_{32,DT}(k), T_{22,DT}(k)]$ using the updated resistance values $[R_{on,32}(k), R_{on,22}(k)]$. The value of $[R_{on,31}(k), R_{on,21}(k)]$ is assumed to be [1.0,1.0] during the this first stage. After $R_{on,22}(k)$ and $R_{on,32}(k)$ converge, stage two starts. In this stage $R_{on,31}(k)$ and $R_{on,21}(k)$ are estimated following:

- If $\Delta T_{21}(k) - \Delta T_{31}(k) > lmt3$, then $R_{on,21}$ is degraded.
- If $\Delta T_{21}(k) - \Delta T_{31}(k) < lmt3$, then $R_{on,31}$ is degraded.
- If $|\Delta T_{21}(k) - \Delta T_{31}(k)| < lmt3$, then both $R_{on,21}$ and $R_{on,31}$ are degraded.

Similarly to the previous stage, the R_{on} value of each degraded SC is updated following (10) in each iteration. The process continues until all $\Delta T_{rc} < lmt3$. The ending iteration computed Ron values are employed to compute the SCs SOH.

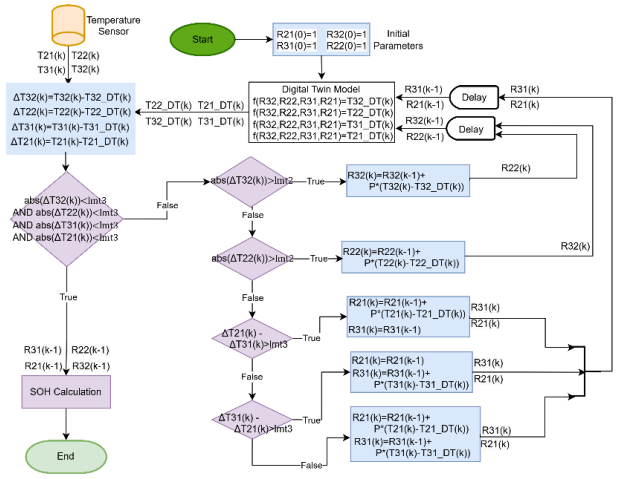


Fig. 7. $R_{on,rc}$ estimation algorithm for SC21, SC22, SC31 and SC32.

C. SOH Calculation

With the estimated R_{on} values, the following equation is used to calculate the SOH value of the SCs

$$SOH_{SC,rc} = \left(2 - \frac{R_{on,rc}}{R_{on,nom}}\right) \quad (11)$$

where $R_{on,nom}$ is the nominal value of the on-state resistance; i.e., the R_{on} value when the SC is in good-health condition.

IV. Simulation Validation

Simulations have been performed with MATLAB-Simulink. The switching model of the IIC has been implemented in this software, together with look-up tables to define the power losses model and the same thermal model as the DT but including a separate thermal model for the heat exchanger. This model is used to obtain the temperatures from the SC sensors. The DT model and SOH assessment algorithm have been implemented also in the same simulation, running in parallel with the switching model. To validate the effectiveness of the proposed estimation method, multiple degradation scenarios were simulated.

In these simulations, I_{CL} = 80 A, the modulation index is 0.8, and the power factor is 0.8. At this operating point, temperature error threshold *lmt1* and *lmt3* are set to 0.4, $lmt2$ is set to 1.2. The results show change on ΔT_{rc} and the estimated $R_{on,rc}$ in the SCs.

Fig. 8 shows the case where a degradation is emulated by setting $[R_{on,11}, R_{on,22}] = [1.5,1.5]\ (pu)$ in the IIC converter switching model. The top plots display the temperature differences (ΔT_{rc}, deltaT *rc* in the legend). The lower plots compare the estimated and real $R_{on,rc}$ for each switching component. Results shows that the estimated resistance of the degraded SCs (SC11, SC22) closely follows the real value, indicating effectiveness of the R_{on} estimation algorithm in Fig. 6. For the rest of SCs (in good health condition), the estimated R_{on} remains at 1 p.u..

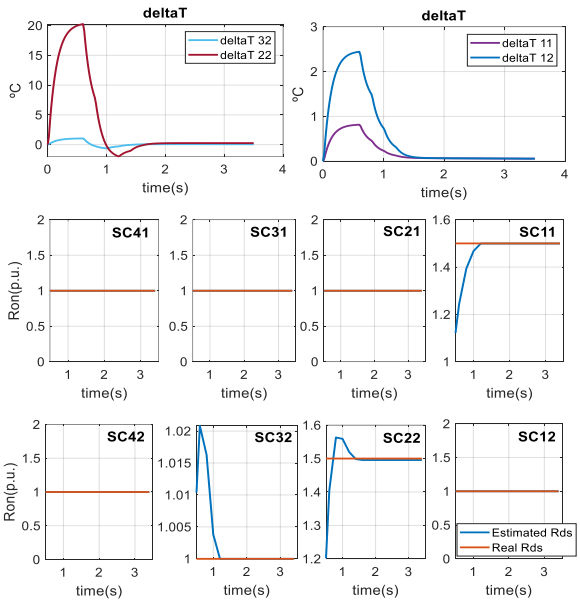
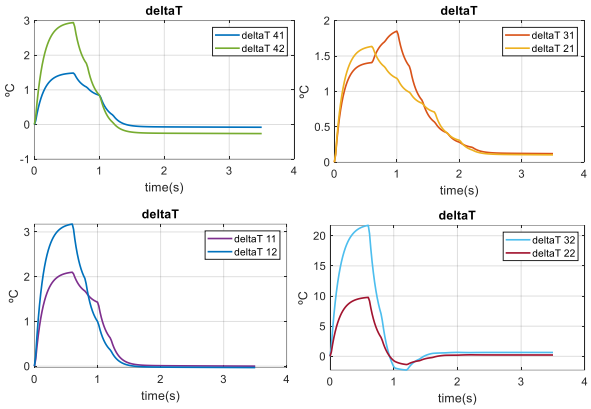
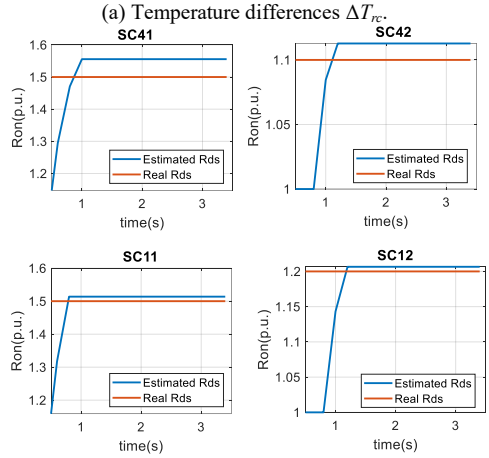


Fig. 8. Simulation results when $[R_{on,22}, R_{on,11}] = [1.5,1.5]$ p. u. is set in the switching model.

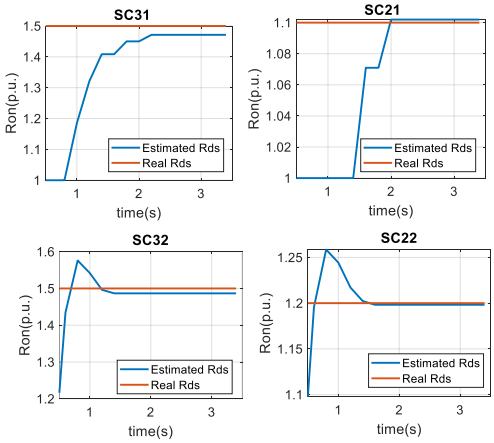
Fig. 9 illustrates the results for degradation in multiple components, in which the value of the degradation is set to $[R_{on,41}, R_{on,31}, R_{on,21}, R_{on,11}, R_{on,42}, R_{on,32}, R_{on,22}, R_{on,21}] = [1.5, 1.5, 1.1, 1.5, 1.1, 1.5, 1.2, 1.2]$ p.u. Fig. 9(a) portray the evolution of the computed temperature differences (ΔT_{rc}) as the algorithm keeps updating the estimated R_{on} values and the computed DT-model temperatures are updated. Fig. 9(b) and Fig. 9(c) show the evolution of $R_{on,rc}$ $\forall r,c$ as the algorithm iterates. These results demonstrate that the R_{on} estimation algorithm accurately tracks degraded cases of all eight SCs. It can be found that the estimator performs well when multiple SCs are degraded and with varying degrees of degradation, from mild aging ($R_{on,rc} \approx 1.1$) to more severe cases ($R_{on,rc} \approx 1.5$), indicating strong adaptability to different CL degradation configurations and aging levels.



(a) Temperature differences ΔT_{rc}.



(b) Estimated $R_{on,rc}$ values for SC41, SC42, SC11 and SC12.



(c) Estimated $R_{on,rc}$ values for SC31, SC21, SC32 and SC22.

Fig. 9. Estimation results when multiple SCs are subject to degradation.

In Fig. 8 and Fig. 9, the estimated R_{on} aligns closely with the real (or reference) value after a brief transient period, indicating that the estimation algorithm is able to estimate the R_{on} values after a few iterations. The results in Fig. 9 are summarized in Table I. SC21 shows an exact match between the estimated and real values, resulting in 0% error and a corresponding SOH of 90%. In contrast, SC41 presents the largest estimation offset (3.33% error), with an SOH of 45%. The remaining switching cells (SC31, SC11, SC42, SC32, SC22, and SC12) exhibit small differences, reflected by accuracy figures ranging from 0.167% to 2%. Their SOH values vary accordingly, from 49% up to approximately 89–90%.

TABLE I. ESTIMATION RESULTS AND SOH CALCULATIONS

Switch Cell	Estimated Value	Real Value	Error (%)	SOH (%)
SC41	1.55	1.5	3.33	45
SC31	1.47	1.5	2	53
SC21	1.10	1.1	0	90
SC11	1.51	1.5	0.67	49
SC42	1.11	1.1	0.91	89
SC32	1.48	1.5	1.33	52
SC22	1.198	1.2	0.167	80.2
SC12	1.21	1.2	0.833	79

V. CONCLUSION

This paper has presented the design and analysis of a comprehensive thermo-electrical DT for SiC MOSFET-based switching-cell-array converters for the use case of an EV three-level NPC hexaphase converter. By combining detailed electrical loss modeling—including the conduction and switching behaviors of C3M0015065K SiC device—and a multi-stage thermal model, the approach captures both fast and slow thermal dynamics, thereby enabling more accurate predictions of device temperatures under diverse operating conditions. The DT powers an algorithm for the estimation of the SCA MOSFET on-state resistance from easy-to-implement sensors measuring the MOSFET case temperatures and the already available battery voltage and converter output current sensors. The on-state resistance estimation allows for an assessment of the converter power devices SOH. The simulations results show excellent accuracy in the estimation procedure, even in scenarios with multiple degraded SCs and with different aging levels. The health assessment opens the door to advanced health management strategies and proactive maintenance scheduling for the power converters.

The next phase of development will involve constructing and testing a hardware prototype of the proposed system to validate the accuracy and robustness of the thermo-electrical DT in real-world conditions.

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