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Original Paper

An SEM Based System for a Complete Characterization of Latch-up in CMOS Integrated Circuits

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Summary

An electron beam testing system was established for a complete and detailed analysis of latch-up in CMOS integrated circuits. Problems which can be studied include:
(a) identification of latch-up current paths in steady state condition;
(b) measurement of the local latch-up sensitivity of the various parts of the circuit;
(c) observation of the time evolution of latch-up from the firing event to the final condition.

1. Introduction

Because of its low power dissipation, wide range of power supply voltages, high noise immunity and low alpha-particle sensitivity, CMOS technology is more and more frequently used in the manufacture of very large scale integrated circuits. As the distance between n and p channel transistors is scaled, however, the sensitivity of CMOS ICs to latch-up phenomena (*Eistreich* 1980) is greatly enhanced, owing to the increase in the current gain (β) of the parasitic bipolar transistors.

In fact, in a CMOS inverter (Fig. 1a) there exist two parasitic bipolar transistors: a vertical NPN, Q_1, formed by the n-substrate (collector), the p-well (base), the n^+ regions in p-well (emitters), and a lateral PNP, Q_2, consisting of the p^+ regions in substrate (emitters), the n-substrate (base), the p-well (collector). These transistors are linked in a configuration which resembles a semiconductor controlled rectifier (SCR), Fig. 1b, the only difference being the two resistances R_s and R_w, which shunt the base-emitter junctions of the parasitic transistors, and which may be omitted here for the sake of simplicity.

Normally, the two parasitic transistors Q_1 and Q_2 are in the **off** state; however, if one of the two transistors, for example Q_2 (Fig. 1c), is brought into the **on** state and if current gain product $\beta_1 \cdot \beta_2$ is sufficiently high the circuit latches and both transistors are kept in the **on** state. In general β_1 and β_2 are functions of collector current; to achieve regeneration a minimum current should therefore flow through the device. Parasitic transistors may be switched on owing to electrical noise, electromagnetic interference, or photocurrents induced by ionizing radiations.

Both e-beam and laser induced currents have been used to induce latch-up in CMOS ICs (*Burns* and *Kendall* 1983, *Dressendorfer* and *Armendariz* 1980), Fig. 1a. In Fig. 1b the current generator I represents the current injected when the beam scans the p-well/n-substrate junction (the NPN and PNP's collector junction). As a result of latch-up condition, a high current flows through the IC frequently causing permanent damage to the device. In the latched area both a marked increase of the p-well potential and a decrease of n-substrate potential take place.

Experimental techniques capable of identifying latch-up sites in order to correct the circuit layout are therefore needed. For complete characterization of the device under test the technique should allow:
(a) identification of various latch-up current paths in steady state condition;
(b) identification of those parts of the circuit more sensitive to a locally injected current and the measurement of their sensitivity;
(c) observation of the time evolution of latch-up from the firing event to the steady-state condition.

The aim of this paper is to demonstrate that an SEM based system equipped with digital control of the beam position, digital image acquisition and processing, a computer-controlled beam blanking and a stroboscopic imaging and waveform recording system allows a complete characterization of latch-up phenomena in CMOS integrated circuits.

For a better appreciation of the capability of the apparatus the known observation techniques are briefly reviewed and discussed in Section 2. Section 3, 4 and 5 are devoted to a description of SEM configurations and operating modes respectively for localization of latch-up current paths, sensitivity measurement and observation of latch-up time evolution. Lastly, the techniques described are discussed in Section 6.

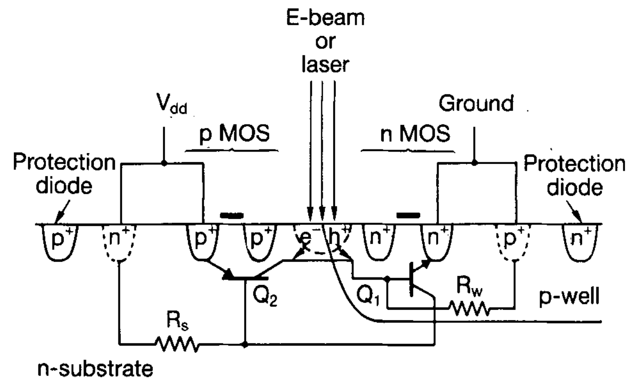


Fig. 1a

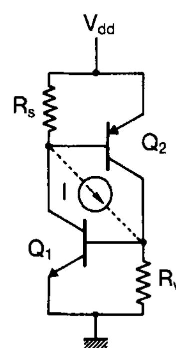


Fig. 1b

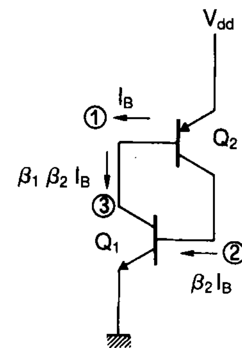


Fig. 1c

Fig. 1 (a) Schematic cross-section of a CMOS inverter showing bipolar parasitic transistors; (b) actual CMOS IC parasitic SCR structure with shunt resistances R_s and R_w. Current I is induced by a laser or an electron beam; (c) parasitic SCR equivalent structure.

2. State of the Art

2.1 Techniques for the localization of latch-up current paths in steady state conditions

These techniques aim to identify the conducting parasitic SCR structures once the IC has been brought into the latched state by suitable electrical stimuli and has reached the steady state condition. Previously described techniques are based on thermal mapping (*Payne* et al. 1980, *Hiatt* 1981), observation of the IR recombination radiation emitted by the parasitic structures in the latched state (*Khurana* 1984), supply current modulation in the latched state by an electron beam or a laser (*Burns* and *Kendall* 1983, *Davidson* 1983, *Dressendorfer* and *Armendariz* 1980, *Lange* and *Winnerl* 1983), SEM Voltage Contrast (*Davidson* 1983).

2.1.1 Thermal mapping

The technique is based on the observation of the "hot spot" in the neighbourhood of the parasitic SCR structure, where, due to the large currents flowing, high temperatures are reached. The "hot spot" can be detected either by infrared microscopy (*Payne* et al. 1980) or liquid crystal techniques (*Hiatt* 1981). Both methods offer poor lateral resolution with best results in the range of 10 μm.

2.1.2 Measurement of IR radiation due to carrier recombination

In the latched state large currents flow through the parasitic SCR structure. Latched areas can therefore be identified by detecting the near-IR radiation (λ = 1.1 μm) due to electron-hole recombination in Si junctions crossed by large forward current. Owing to

the extremely low radiative efficiency of Si, small radiation intensities result and this may give raise to sensitivity problems. However, resolution is much higher than that obtained with thermal mapping and the possibility of identifying the sequence of latch-up occurrences when several sites latch in the IC has been demonstrated (*Khurana* 1984).

2.1.3 Supply current modulation by a laser or an electron beam

The device is electrically forced into the latched state and the device supply current is monitored while the circuit is scanned by a He-Ne laser (*Burns* and *Kendall* 1983) or an electron beam (*Davidson* 1983, *Dressendorfer* and *Armendariz* 1980). The scanning beam generates hole-electron pairs in the semiconductor (Fig. 1a). Carriers generated within about a diffusion length of reverse biased junctions are collected and appear as changes in the supply current of the device.

A large change in the device supply current is observed when the beam scans the area involved in latch-up, thus enabling latch-up sites to be identified. The high current magnification in the latched parasitic SCR structures can be due to transistor action or avalanche multiplication (*Burns* and *Kendall* 1983, *Davidson* 1983).

When supply current is modulated by a scanning electron beam the device supply current is observed by an SEM in the EBIC mode using an AC coupled current amplifier to derive the video signal. The electron beam energy must be sufficiently high to penetrate through the various metal, polysilicon and oxide layers of the device. This, however, may cause alterations in the threshold of MOS transistors, and, possibly, alterations in the logical state of the device. For the same reason the electron beam may also alter the latch-up behaviour of the device.

Compared to the EBIC technique in the SEM, a scanning laser system offers two main advantages: (a) the threshold voltage of MOS devices is not influenced during testing, and (b) photocurrent signals are more intense (20 μA typical using a 1 mW He-Ne laser compared to 10^{-2} μA using EBIC with 30 kV accelerating potential and 10^{-11} A beam current (*Burns* and *Kendall* 1983, *Dressendorfer* and *Armendariz* 1980)). On the other hand, a laser based system requires the construction of a dedicated scanning system; depth of carrier generation cannot be easily varied; calibration of the system must be frequently repeated owing to drift in the latch-up current during measurement (*Burns* and *Kendall* 1983). Moreover, both EBIC and laser systems do not reveal the details of the latch-up current paths (*Burns* and *Kendall* 1983, *Davidson* 1983).

2.1.4 SEM voltage contrast

Conventional Voltage Contrast (CVC) cannot be succesfully applied to the study of latch-up in passivated CMOS because MOS structures must be observed at low energies (below 2 keV) in order to avoid MOS threshold voltage alterations due to charge injection and trapping in the gate oxide. At such low energies electrons are halted within the outermost layers of the passivation and it is impossible to extract any information about the potential distribution in substrate and diffused regions. It is, however, possible to detect such potential distribution by means of a quasi-state operating technique known as Capacitively Coupled Voltage Contrast (CCVC). Briefly, if the device bias is suddenly switched on, a potential distribution, reproducing the potential pattern in the underlying conductors, is instantaneously induced by capacitive coupling on the outer surface of the insulator. This potential distribution, however, usually decays so fast that it cannot be used for the formation of a voltage contrast image. Therefore, in order to obtain a meaningful image it is necessary to switch the device bias on and off faster than this decay time (*Kotorman* 1980). In this way it is possible to observe the potential present on metals covered by the passivation layer and on semiconductor diffusions covered by thermal oxide (Fig. 2).

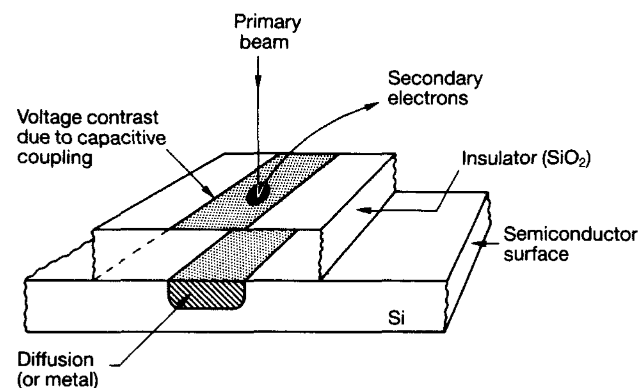


Fig. 2 Mechanism of capacitively-coupled voltage contrast

A technique based on this principle has been developed by *Davidson* (1983), who was able to identify potential drops induced in p-well and n-substrate by latch-up currents; nevertheless, the superimposition of voltage and topographical contrast makes identification of potential drops along these current paths difficult.

2.2 Techniques for the measurement of local latch-up sensitivity

The evaluation of latch-up sensitivity on CMOS ICs has been performed by means of laser scanner analyzers (*Henley* et al. 1983, *Shiragasawa* et al. 1984). The device is kept normally biased; parasitic SCR structures are initially in the **off** state. A focussed laser beam is scanned on the area under investigation so that hole-electron pairs are generated in the semiconductor (Fig. 1a). The photocurrent generated at the p-well/n-substrate junction (the PNP and NPN's collector junction which has the largest collection efficiency) is simulated by the generator I in Fig. 1b. The light intensity is increased until latch-up occurs and the inverse of this intensity, for each position of the light spot, is taken as a sensitivity measure.

Major drawbacks of the technique are:

(a) it is necessary to establish a correlation between electrical behaviour and photoelectric measurements, and this correlation must be updated with changing technology;
(b) the large currents resulting from carrier generation can alter the normal behaviour of the device;
(c) the relatively high laser power densities required may induce unwanted thermal effects;
(d) the amount of carrier generated in the semiconductor markedly depends on the absorption of the upper layers;
(e) the time required to form a 50 × 50 image is reported to be of the order of 12 min (*Henley* et al. 1983).

2.3 Techniques for the observation of latch-up time evolution

Lastly, it is worth stressing that up to now no technique for the observation of time evolution of latch-up from the triggering event to the steady state condition has been reported.

3. The SEM Technique for the Identification of Latch-up Current Paths

The latch-up condition induces a large potential increase in the p-well and a decrease in n-substrate potential; therefore, as stressed by *Davidson* (1983), latch-up current paths in CMOS can be effectively localized if a technique for revealing the voltages on the surface of p-well and substrate is available.

In Fig. 3a the SEM micrograph of an unpassivated, unbiased CMOS device is shown while Fig. 3b shows the conventional voltage contrast image of the same device biased at $V_{dd} = 5\,V$ ($E_b = 2$ keV, $I_b = 10^{-9}$ A). As can be seen, by removing the passivation the voltage contrast on the metal lines has been made visible, i.e. grounded lines appear white in the micrograph, while metallizations at higher potentials appear black; however, no information is available about the potential of semiconductor diffused areas, covered by thermal oxide.

If the voltage applied to the device is switched on and off and the SEM electron beam is blanked synchronously during the **off** period a pseudostatic voltage contrast on p-well and substrate is obtained because the voltages on the silicon substrate are capacitively coupled through the thermal oxide to the surface (Fig. 3c).

Unfortunately, owing to the superimposition of voltage contrast with topographic and compositional information on the micrograph, a great difference in contrast between metal lines and diffused areas is visible even when the metallization and the semiconductor are at the same potential; voltage information from the diffused areas may thus be compromised.

As is known, topographic and compositional information may be effectively reduced by subtracting the signal detected when the device is unbiased from that obtained in the biased condition; this enables the resolution of small potential differences as required for indirect localization of latched structures.

A new technique was therefore developed combining the principles of capacitively coupled voltage contrast and topography subtraction; this was achieved thanks to digital beam control and image acquisition, overcoming the noise and speed problems affecting previous techniques (*Piwczyk* and *Siu* 1974).

Figure 3d shows the "Digital Differential Voltage Contrast" (DDVC) image of the device. Potentials on both p-well and n-substrate can now be easily seen and the apparent potential difference between grounded metal lines and p-well is effectively cancelled.

Digital beam control and image acquisition offer several advantages over analog processing; first, all

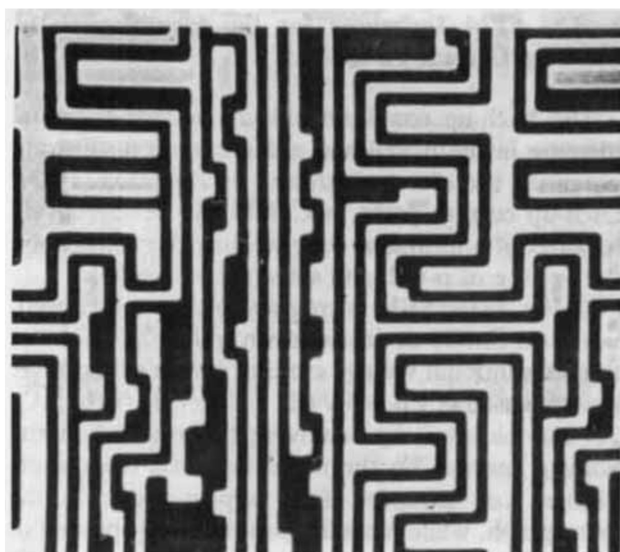


Fig. 3a

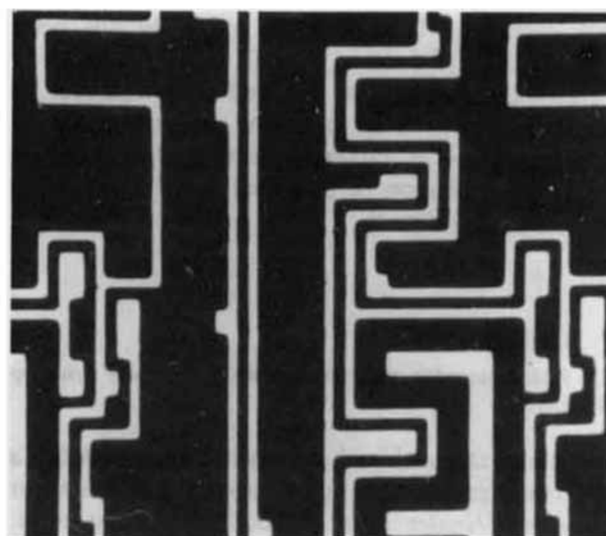


Fig. 3c

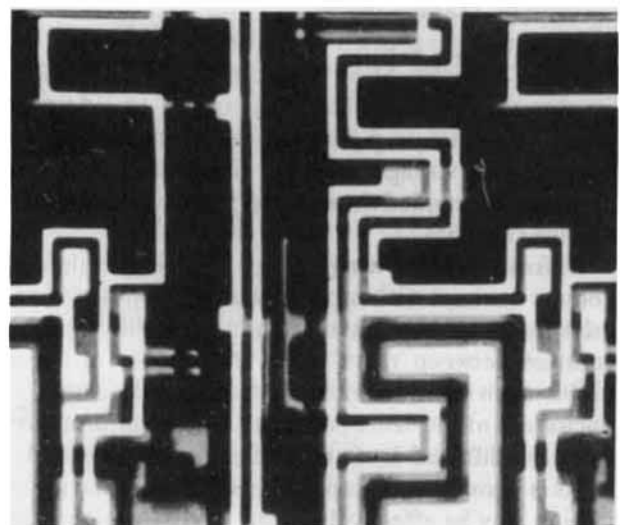


Fig. 3b

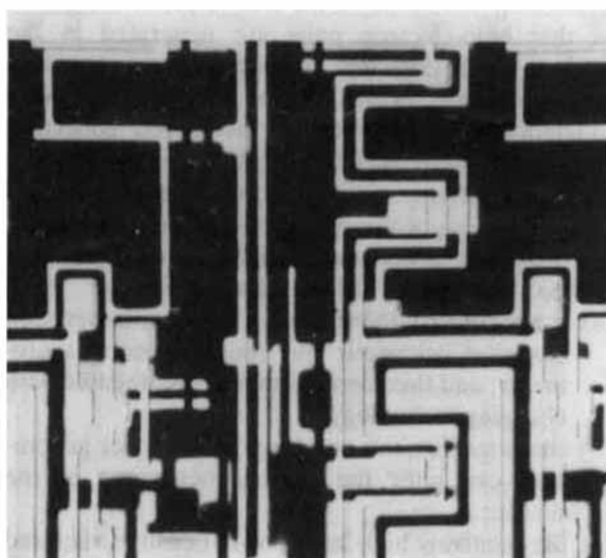


Fig. 3d

Fig 3 (a) SEM micrograph of an unpassivated CMOS IC with no bias; (b) conventional voltage image of the same device, biased; (c) capacitively coupled voltage contrast image; (d) capacitively coupled voltage contrast image with topography subtraction. Higher potentials are coded as dark. Horizontal field width = 280 μm.

operations are performed with the beam at rest in a specified position rather than on fly during a line scan; secondly, the availability of data in digital form enables the use of averaging techniques with consequent enhancement of signal/noise ratio. Finally, acquisition times can be reduced. Topography subtraction and digital processing are the key features of the proposed Digital Differential Voltage Contrast technique.

The implemented digital system proposed in the present work (Fig. 4) controls beam position, converts data from analog to digital and performs via hardware

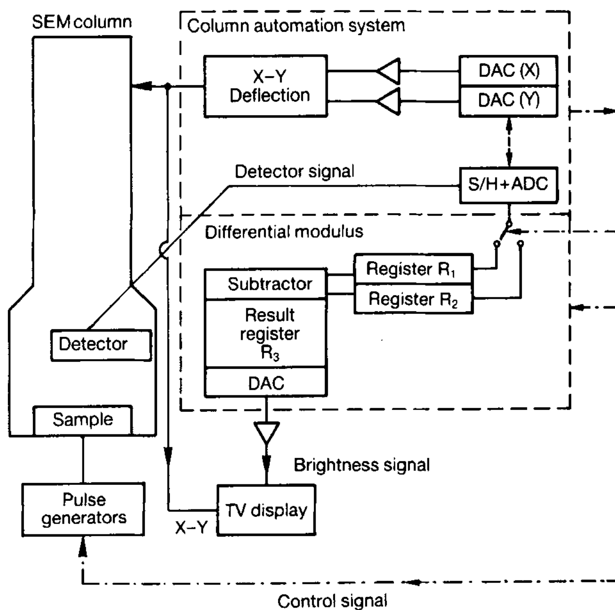


Fig. 4 Block diagram of the DDVC system consisting of the SEM, the column automation system and the differential modulus.

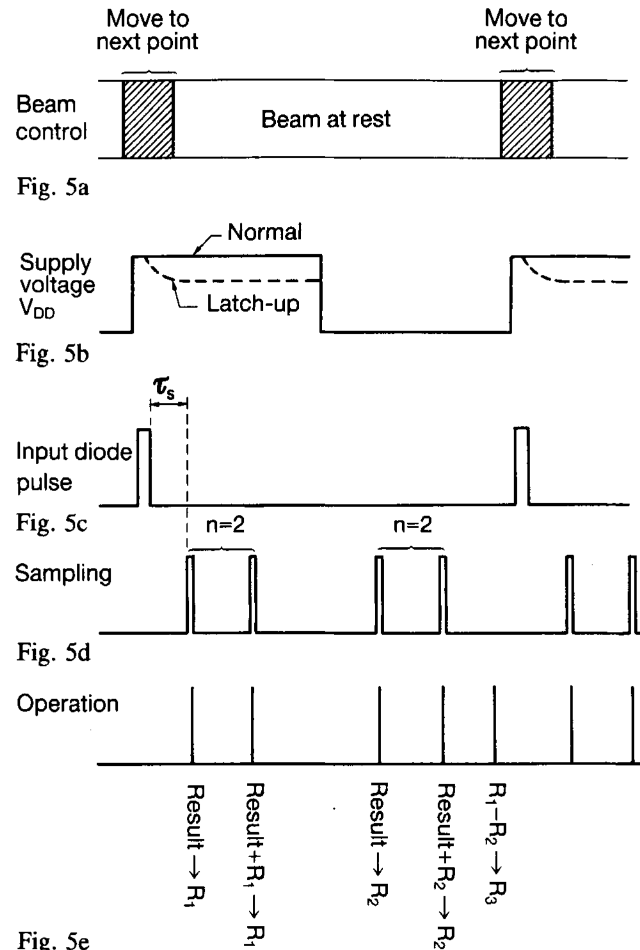


Fig. 5 System operation: (a) beam position control; (b) supply voltage applied to the IC; (c) input diode pulse used to induce latch-up; (d) sampling of the SEM detector signal; (e) ADC conversion of detector signal and topography subtraction.

the whole cycle of data acquisition, specimen bias control, digital subtraction and display of the difference for each image point, without involving the relatively slow memory of the computer controlling the SEM (*Sardo* and *Vanzi* 1984). The pulse generators controlled by the column automation system provide bias supply and the pulse applied to the IC to induce latch-up.

The operation of the system can be summarized as follows: the SEM electron beam scans in a raster fashion the $N \times M$ image points where N and M range from 64 to 4096. As Fig. 5 shows, while the beam moves to the next position the IC bias is switched on and latch-up is forced. In the example shown in the figure this is obtained by forward biasing an input diode. A drop in V_{dd} takes place as a consequence of latch-up. After allowing a settling time τ_s which should be chosen long enough to allow the device to reach a stable condition the detector signal is sampled and A/D converted n times ($0 < n < 256$).

To obtain an averaged value the n results of the sampling operation are sequentially added, storing the final value in a first register (R_1). The bias is then switched off and the same sequence of operation is repeated, storing the result in a second register (R_2). The difference between R_1 and R_2 is then loaded into a third register (R_3), D/A converted and used as brightness signal for the SEM display. At the end of these operations the beam moves to the next point and the cycle is repeated.

The minimum acquisition time is 4 μs per pixel picture element for $n = 1$: a 512×512 pixels image, with 8 bit grey resolution, may thus be completed within 1.2 s. By way of comparison with the technique described by *Davidson* (1983) it is worth stressing that the higher frequency bias modulation (up to 250 kHz) allows for capacitively coupled voltage contrast even in adverse conditions (short decay time of the capacitively induced potential distribution).

The analysis of latch-up paths mainly consists of the comparison between images taken in the latched and non latched state and it is difficult to provide well defined, generally applicable analysis rules: the only *suggestion* is that the technology and layout of the device to be investigated should be well known to the analyst. All the reported DDVC images were digitized in a 512 × 512 format, with positive regions coded dark. Beam energies in the range 1.2–1.5 keV and beam currents = 10^{-9} A were used.

Because the aim of this paper is mainly to describe experimental apparatus and techniques for latch-up characterization all the following observations described will refer to the same circuit part. The example chosen is an analog block in a fully custom CMOS IC, manufactured with a standard 7 μm, metal-gate, p-well, junction insulation technology. The layout of this block is shown in Fig. 6a. The device was found to latch when a positive spike ($V_{spike} > 15$ V with a measured $I_{spike} > 120$ mA for $V_{dd} = 5$ V and $t_{spike} >$ 1 μs) was applied to a specific input, thus forward biasing the protection diode.

Figures 6b and 6c report the DDVC image of the device on non-latched and latched states respectively. As a consequence of the latch-up condition the substrate region indicated by arrows in Fig. 6a, not covered by metal lines and adjacent to the p-well, becomes whiter, while the p-well immediately beside it becomes darker. To enable better appreciation of this effect a magnification of the latched area is presented in Fig. 7.

In the substrate area included between the arrows a potential drop between the extremes and the center can be observed; in particular the appearance of the substrate region becomes darker und darker as points farther from the current path are considered because they remain tied to the V_{dd} voltage, while the central region, nearly short circuited to ground by the latch-up phenomenon, appears whiter. A reciprocal effect is also visible in the adjacent p-well.

The potential drop observed in Figs. 6c and 7b enables identification of actual current path within the pnpn structure responsible for the latch-up, thus providing useful information for layout design and correction (*Fantini* et al. 1985).

4. The SEM Apparatus for the Measurement of Local Latch-up Sensitivity

In this configuration the electron beam in the SEM is used as a localized current injector. The method consists of irradiating a certain area of the chip under test with the electron beam and measuring the primary electron beam current needed to induce latch-up at a fixed beam energy in controlled electrical conditions. Because the injected carriers are used to induce the latch-up state rather than to visualize its paths, the technique is intrinsically different from the EBIC technique described by 1 *Dressendorfer* and *Armendariz* (1980).

The main problem in operating the SEM as a current injector is the damage to MOS devices which takes place if the high energy electron beam is scanned in the neighbourhood of MOS gates.

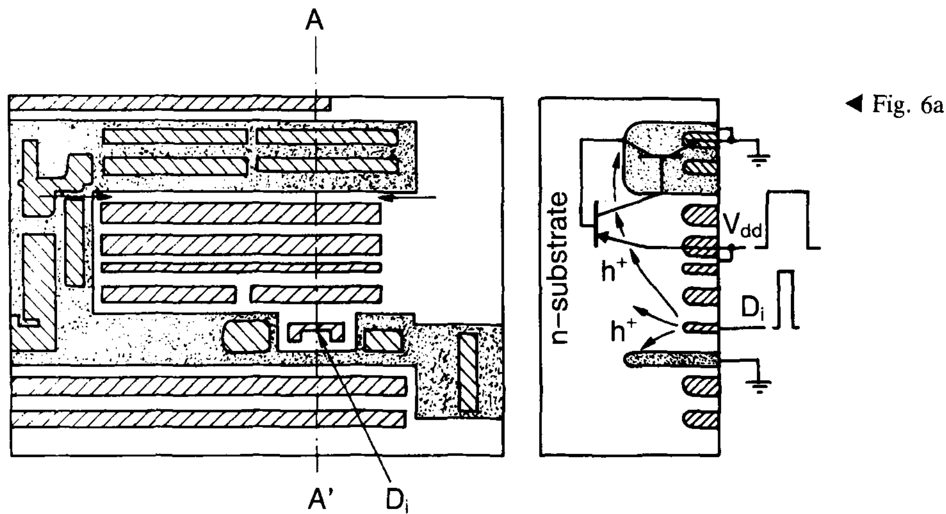
To minimize the effects of charge injection in the gate oxide of MOS devices we had recourse to digital control of the beam position. A minicomputer-based system (Tracor-Northern TN 1310) was adopted to obtain scans only along arbitrarily defined paths or areas. The minicomputer also allows electron beam blanking when MOS gate areas are crossed to avoid charge trapping, and controls the pulse generation which provide bias supply.

Figure 8 describes the SEM configuration implemented for latch-up sensitivity measurements. Operations can be summarized as follows:

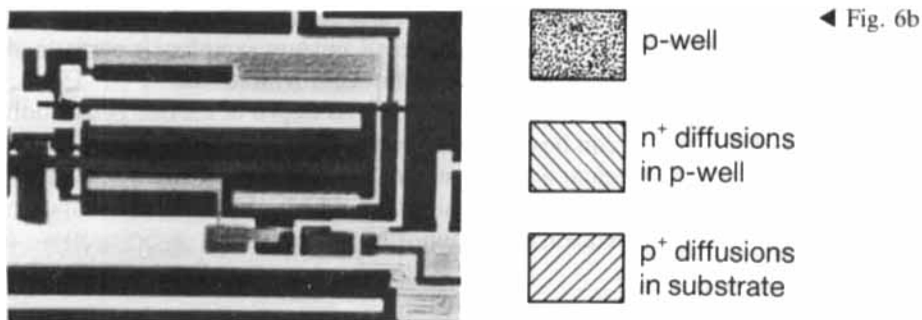
(a) to minimize charge injection the secondary image of the device under test taken at very low beam current is stored in the display memory and the beam is blanked;
(b) the operator can then define the scan paths or scanned areas on the stored image which is continuously displayed on the TV screen; areas which should be protected from charge injection can also be identified; the microcomputer will automatically blank the beam if the scan path had to cross these areas.

Figure 9 reports main control signals during the scanning; while the beam moves to the next position the IC bias is switched on and after allowing a delay time τ_d, the beam is turned on; the electron beam pulse duration can be chosen in the 50 μs–5 ms range. Latch-up occurrence can be monitored, after turning off the beam, by measuring the device supply current; in fact, a great increase in supply current (up to hundreds of mA) is observed in the latched condition. The cycle can be repeated and an averaged value of supply current can be associated with each point on the defined path. Results can be visualized in graphic form on the TV display.

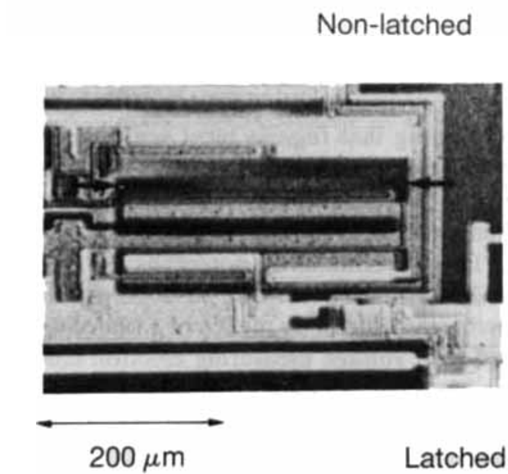
Figure 10a shows the SEM micrograph of the CMOS analog block previously analyzed; the superimposed polygon ABCDEF runs across the p-well/n-substrate junction where the circuit is more sensitive to the beam induced current. Figures 10b, c, d show



◀ Fig. 6a



◀ Fig. 6b



◀ Fig. 6c

Fig. 6 (a) Layout of the diffusions of the input circuit of analog block and cross section along AA^l axis; (b) DDVC image of the same area in the non latched state; (c) in the latched state. Arrows indicate the substrate region where a strong voltage drop is observed. Higher potentials are coded as dark. Horizontal field width = 500 μm.

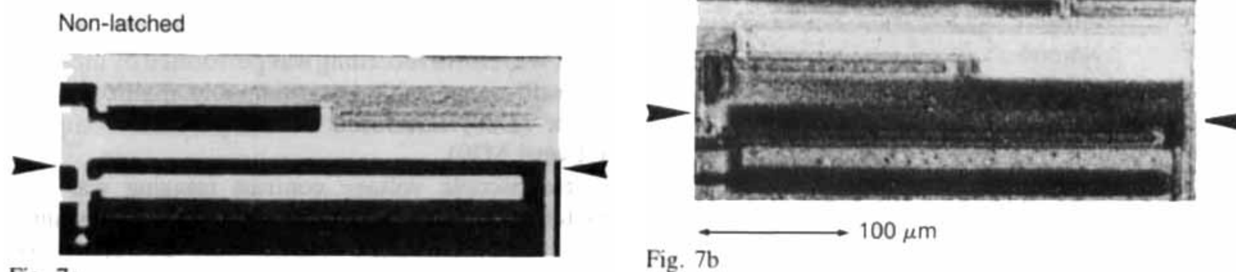


Fig. 7a

Fig. 7b

Fig. 7 Enhanced DDVC image of the latched area. (a) in the non-latched state; (b) in the latched state. Horizontal field width = 300 μm.

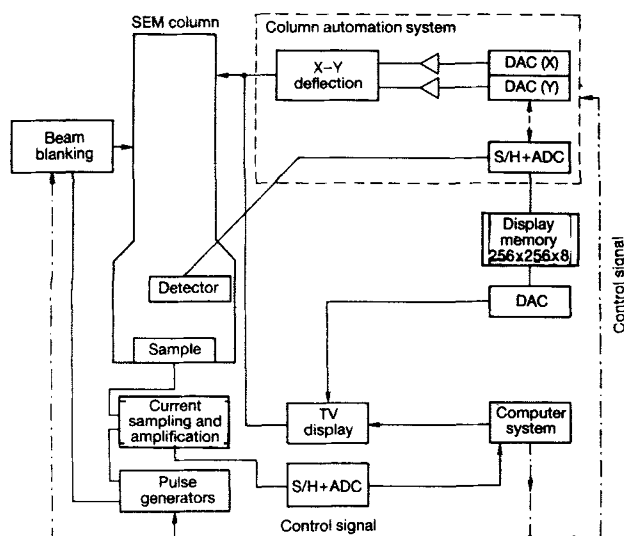


Fig. 8 Block diagram of the SEM configuration adopted for latch-up sensitivity measurements consisting of the SEM, the beam blanking unit, the column automation system, the display memory and the current sampling unit. All blocks are under control of the computer system.

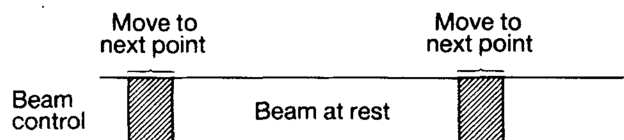


Fig. 9a

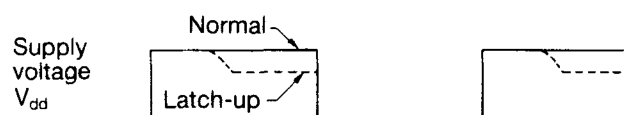


Fig. 9b

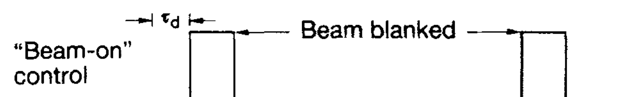


Fig. 9c

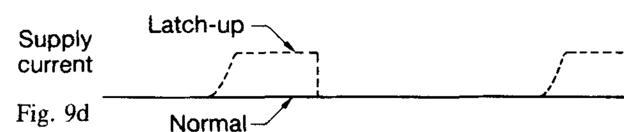


Fig. 9d

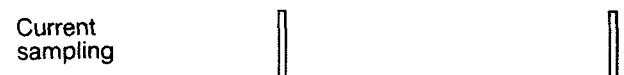


Fig. 9e

Fig. 9 Main control signals during latch-up sensitivity measurements: (a) beam position control; (b) supply voltage applied to the IC; (c) beam blanking control; (d) supply current; (e) current sampling.

the supply current during the scan with a beam energy of 25 keV and a primary beam current I_b of 120 nA, 170 nA, 260 nA respectively. Primary beam current was measured by means of a withdrawing Faraday cup and a current amplifier. By measuring the primary electron beam current sufficient to induce latch-up in fixed electrical conditions a relative measurement of the sensitivity of the various areas can be obtained. As is evident in Fig. 10a, the most sensitive area is found in the upper part of the p-well involved in the latch-up path at the p-well/n-substrate junction along the AB segment.

Further latch-up firing points with a lower sensitivity are found for higher beam currents, Figs. 10 c and d.

Alternatively, the beam-induced supply current increase in the non-latched condition at fixed primary beam energy and current can indicate local latch-up sensitivity; in this case, current sampling is performed in synchronism with beam irradiation.

Beam penetration and depth of carrier generation can be controlled by varying the beam energy; this is a clear advantage over laser-based systems where depth of carrier generation which depends on radiation wavelength cannot be easily varied.

5. Observation of Latch-up Time Evolution in an SEM

As mentioned above, we developed a technique capable of confirming that regions most sensitive to locally injected, electron beam or laser induced current also play a fundamental role in latch-up triggering when latch-up is caused by electrical noise at I/O pins. Time evolution of potentials on the surface of an integrated circuit can be observed in stroboscopic voltage contrast by means of a sampling SEM equipped with voltage measuring electron collector, e-beam blanking, sampling and delay unit for stroboscopic imaging and waveform recording (Fig. 11).

A Cambridge Stereoscan 250 scanning microscope equipped with a Lintech SSEM 2 sampling system was used. Waveform recording was performed by means of an oscilloscope with programmable digitizer (Tektronix 7D20) interfaced with a personal computer (Olivetti M20).

Stroboscopic voltage contrast imaging was first applied; in this method the primary electron beam is pulsed in synchronism with the periodic supply bias V_{dd} waveform applied to the IC under test. The primary electrons only strike the IC at a particular phase of the cycle. In this way, the resulting secondary

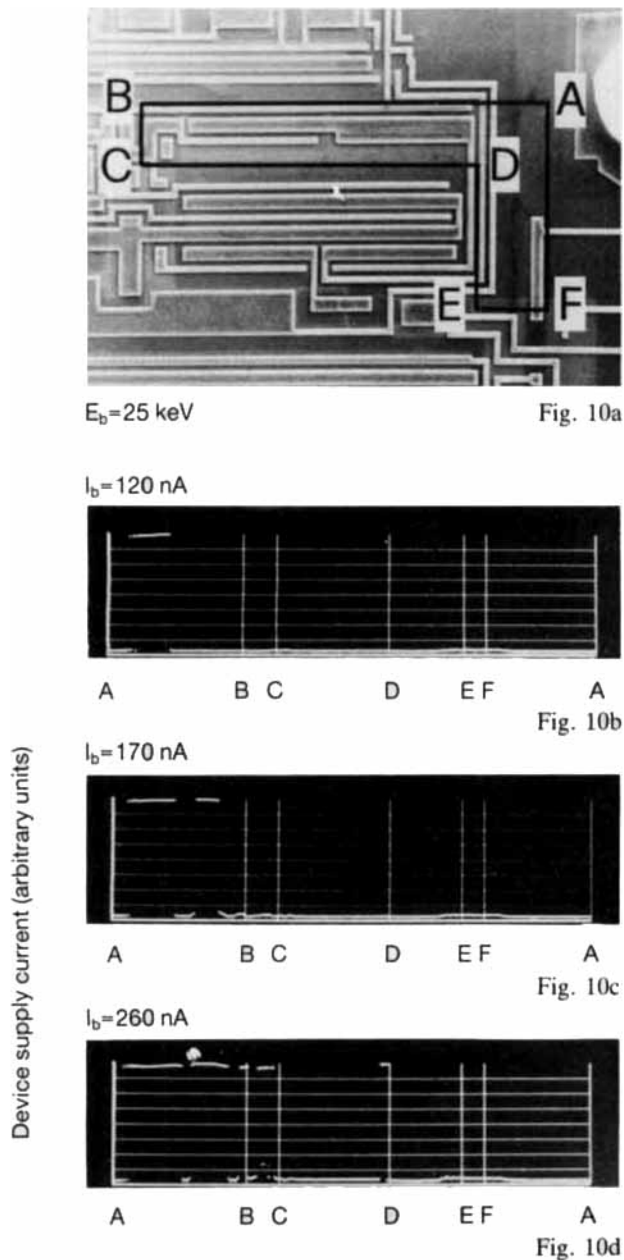


Fig. 10 (a) SEM micrograph of the CMOS analog block under test; the electron beam scans along the ABCDEF path at a fixed energy: 25 keV; (b) supply current during the scan with I_b = 120 nA; (c) I_b = 170 nA; (d) I_b = 260 nA. Horizontal field width = 600 μm.

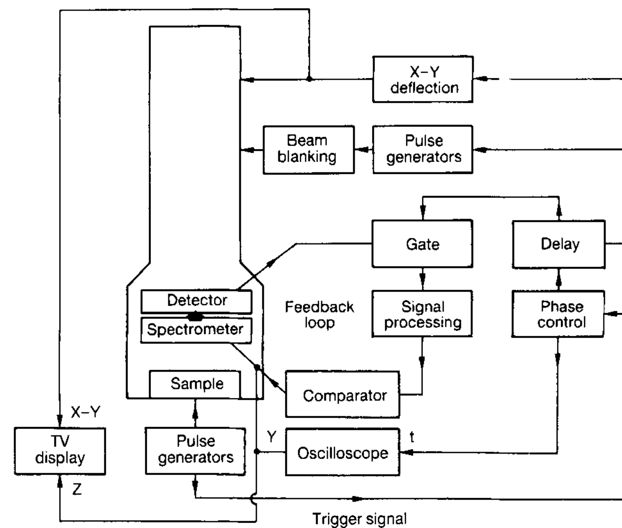


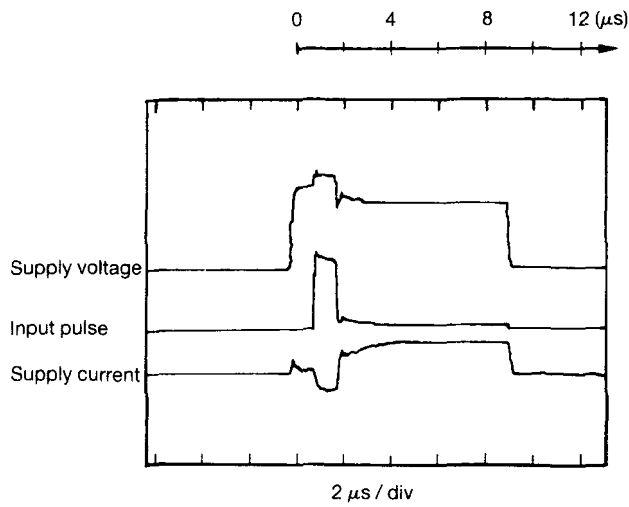
Fig. 11 Block diagram of the SEM system for stroboscopic imaging and waveform recording consisting of the e-beam blanking unit, the voltage measuring collector, the delay unit and phase shifter.

electron image shows a voltage contrast which is related to local voltage distribution at that particular phase of the test waveform. The Lintech VMEC (Voltage Measuring Electron Collector) unit gives a linear correspondence between local voltage value and contrast of the image point.

The previously described device was depassivated and observed at 2 keV beam energy and at low currents ($I_b = 10^{-11}$ A); the supply bias was pulsed at 50 kHz; latch-up was initiated by applying a positive spike ($V_{spike} = 15$ V, $I_{spike} = 120$ mA, $t_{spike} = 1$ μs, $V_{dd} = 5$ V); supply current was monitored to recognize latch-up occurrence. At the top of Fig. 12 are shown supply voltage and current and input pulse waveforms as measured at the IC terminals by an oscilloscope. Figure 12a shows the stroboscopic voltage contrast micrograph of the previously described CMOS analog block at t = 0, i.e. in the non-latched state, before applying the noise pulse. A duty cycle of 2% was used; boxcar averaging was adopted to improve signal-to-noise ratio and image contrast (*Menzel* and *Kubalek* 1983).

Figure 12b shows the stroboscopic micrograph of the device shortly after the input pulse was turned off (at t = 2.2 μs); a large potential increase is visible in the p-well adjacent to the p^+n input protection diode (D_i in Fig. 6a), while the p-well area above has not yet reached the latched condition and holds a low potential (thus appearing white in the micrograph).

As the time elapsed from the input spike increases, a large voltage drop appears in the upper p-well; in fact, an increase in potential appears at the extreme right of the upper p-well (which becomes black) and gradually propagates to the whole p-well area.



◀ Fig. 12 top

Fig. 12 Top: Supply voltage and current and input voltage waveforms as measured at the IC terminals.
Bottom: stroboscopic voltage contrast micrograph of the CMOS analog block under test: (a) t = 0; (b) t = 2.2 μs; (c) t = 4.0 μs; (d) in steady-state condition, t = 8.0 μs. Horizontal field width 420 μm.

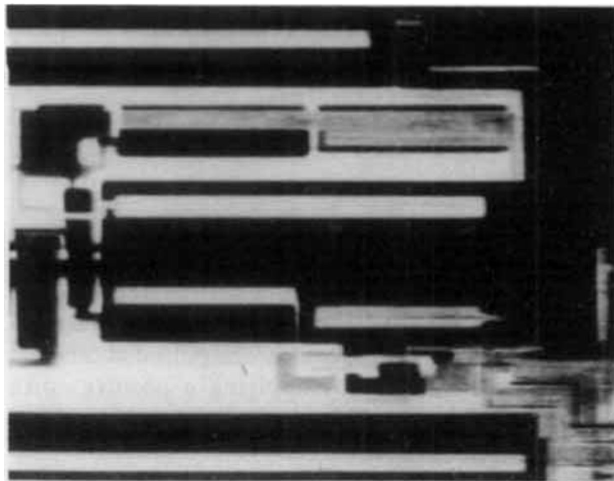


Fig. 12a

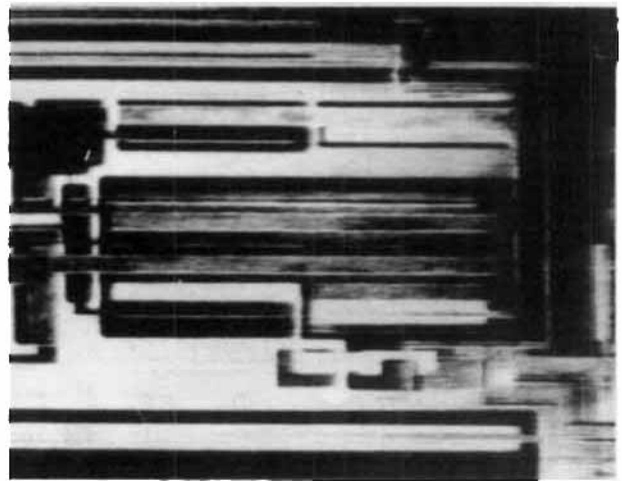
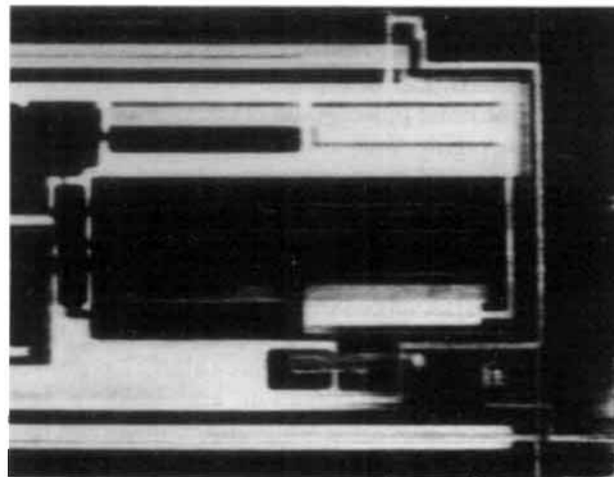


Fig. 12c



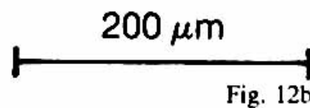
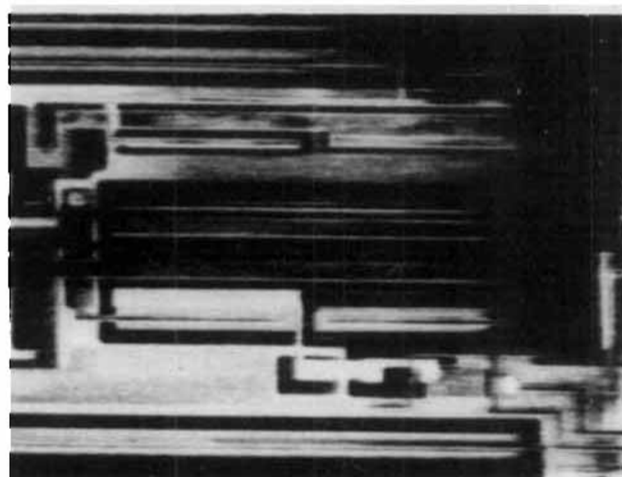


Fig. 12b



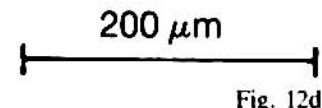


Fig. 12d

In particular, at t = 4 μs (Fig. 12c) the potential of the p-well adjacent to the input protection diode drops to a low value, while the p-well above shows a potential increase exactly in those sites identified in Fig. 10 as areas of maximum sensitivity to current injection, i.e. at the extreme top right of the micrograph.

Latch-up steady state is reached at 8 μs, along with maximum current absorption, and a marked increase in potential is visible in the whole p-well area (Fig. 12d).

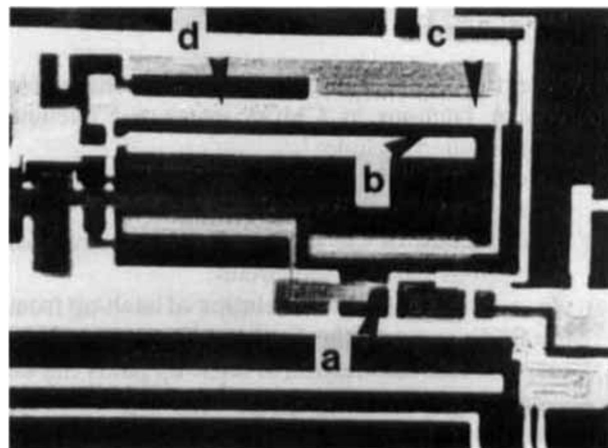
To confirm the results obtained, stroboscopic waveform analysis was performed. The waveform measurement set-up consists of a delay unit for phase definition and a signal processing unit. Voltage contrast linearization obtained by means of the VMEC unit enables measurements to be made.

The stationary beam is positioned at a fixed point of the IC under test. The periodic supply bias waveform triggers the phase control of the delay unit and the phase of the e-beam pulse (i.e. the sampling phase) is swept through one or more complete periods of the trigger signal so that the whole cycle of the waveform to be measured is repeatedly sampled. The collected and amplified secondary electron signal is displayed on an oscilloscope; it can be digitized and averaged.

Waveform measurement on p-well and substrate, which are covered by a SiO_2 layer is still possible thanks to capacitive coupling between the oxide surface and the semiconductor below. To avoid contaminating and charging the oxide surface very low probe current and duty cycle should be used (*Todokoro* et al. 1983; *Ura* et al. 1982).

Figure 13 shows a voltage contrast image of the device in the non-latched state; points of interest for studying latch-up triggering are identified; e-beam measured voltage waveforms in points a, b, c, d are shown together with supply voltage, supply current and input pulse measured at IC terminals. Clock frequency was 50 kHz; a duty cycle of 0.1% was adopted; a beam energy of 2 keV and a primary beam current of 10^{-11} A were used.

The observed measurements confirm the voltage increase induced by latch-up in the p-well and the higher sensitivity of point (c) to the phenomenon as already found during sensitivity measurements (Fig. 10). After the supply voltage V_{dd} has been turned off the surface of the p-well thermal oxide remains charged and an apparent high potential status is measured. As already found during voltage contrast measurements on passivated semiconductors (*Fujioka* et al. 1983) the induced charge is cancelled only when the device is again biased.



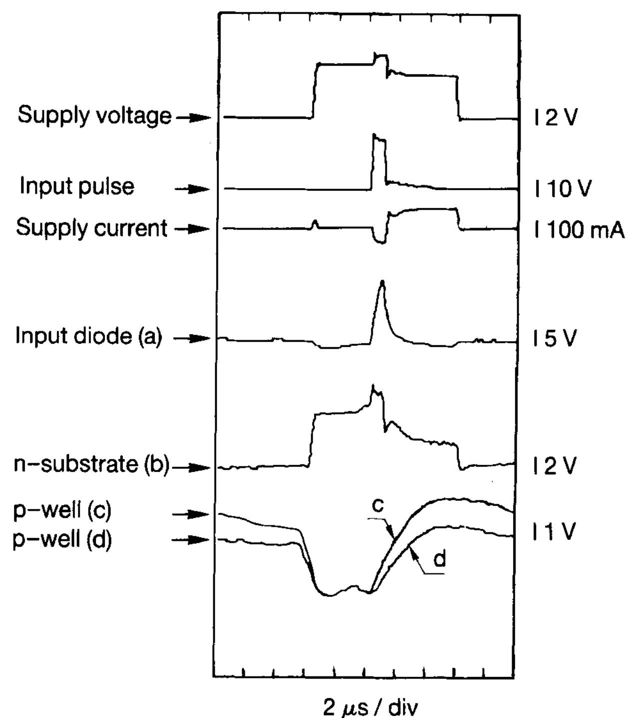


Fig. 13 Supply voltage, supply current and input pulse measured at the IC terminals; stroboscopic e-beam waveforms measured in points a, b, c, d as identified in the voltage contrast image at the top of the figure. Horizontal field width = 500 μm.

The technique enables the identification of latch-up firing points, thus providing further valuable information for layout correction. The high temporal (≅ 2 ns) and voltage (≅ 20 mV) resolution achievable in the waveform recording mode provides a useful tool for the validation of theoretical models of latch-up dynamic triggering (*Pinto* and *Dutton* 1985).

6. Discussion and Conclusions

An electron beam testing system was established for analysis of latch-up in CMOS integrated circuits. Problems studied include:

(a) identification of latch-up current paths in the steady state condition;
(b) measurement of the local latch-up sensitivity of the various parts of the circuit;
(c) observation of the time evolution of latch-up from the firing event to the final condition.

Complete characterization of latch-up paths can be achieved in an SEM equipped with digital beam control and image acquisition, beam blanking and linearization unit for stroboscopic voltage contrast imaging and waveform recording.

Capacitively coupled voltage contrast and topography subtraction enables voltage drops in substrate and p-well to be identified, thus revealing the details of the latch-up current paths. Passivated devices are studied at low beam energies without interfering with their electrical behaviour.

For latch-up sensitivity measurements the electron beam is used as a localized current generator (Fig. 1a). Primary beam current needed to induce latch-up at a certain beam energy in fixed electrical conditions can be taken as a measurement of the local latch-up sensitivity. Valuable information is obtained for layout correction, in particular as regards placement of protection diodes and guard-rings which can become dangerous current injectors in the presence of electrical noise at I/0 nodes (*Eistreich* 1980). Damage to MOS devices caused by high energy electron beam irradiation is almost completely eliminated by careful choice of the scanning paths obtained by means of digital control of beam position and beam blanking.

Unlike previously proposed techniques based on a scanning laser beam this method does not require the construction of a dedicated scanning system. Furthermore, the depth of carrier generation can be easily controlled by varying the beam energy.

Finally, observation of latch-up evolution from the firing event to the steady state condition is only possible with stroboscopic voltage contrast techniques in the SEM. The actual starting point of latch-up when the device is subjected to electrical noise at I/0 pins or at supply terminals can be observed. In particular it is possible to verify whether points of maximum sensitivity to external electron beam or laser induced current also play a significant role in firing latch-up when the device is subjected only to electrical overvoltages. A temporal resolution of $\cong 2$ ns can be achieved, sufficient to observe latch-up transients in VLSI CMOS circuits. We also believe that the sampling SEM in the stroboscopic waveform recording mode can provide a valuable tool for the validation of models of latch-up dynamic triggering (*Pinto* and *Dutton* 1985) by means of an experimental technique.

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