UNIVERSITA' DEGLI STUDI DI MODENA E REGGIO EMILIA

Dottorato di ricerca in Electronics and Telecommunications
(nell'ambito della Scuola di dottorato in Information and Communication Technologies)

Ciclo XXIV

Tesi di dottorato

Characterization and numerical simulations of GaN HEMTs for power and innovative applications

Candidato: Valerio Di Lecce

Relatore (Tutor): Prof. Alessandro Chini

Coordinatore del Dottorato: Prof. Mattia Borgarino
Direttore della Scuola di dottorato: Prof. Matteo G. Vitetta

Gennaio 2012

Contents

Sommario

Negli ultimi decenni il mercato tecnologico ha visto una evoluzione sempre crescente nella direzione di applicazioni ad alto contenuto informativo, quali la telefonia mobile, comunicazioni broadband/multiband o satellitari, oltre ad applicazioni militari come i radar o applicazioni in ambienti estremi. Le specifiche richieste ai dispositivi deputati a soddisfare queste esigenze sono una elevata velocità di trasmissione, una elevata efficienza, e la possibilità di operare a maggiori frequenze e a maggiore potenza. In questa ottica, due materiali hanno attirato massicci investimenti per le loro attraenti proprietà in questo senso: il Nitruro di Gallio (GaN) e il Carburo di Silicio (SiC). Il loro ampio bandgap li rende due ottimi candidati, ma è la grande versatilità del GaN ad avvantaggiare questo composto, grazie alla sua possibilità di formare eterogiunzioni con altri nitruri del gruppo III e al suo bandgap diretto, dando così vita ad un'ampia varietà di sistemi per applicazioni sia elettroniche che ottiche. Nel corso degli anni l'affidabilità dei dispositivi in GaN è stata oggetto di numerosi studi, e diverse soluzioni tecnologiche sono state studiate per ovviare ai problemi riscontrati sia in funzionamento dc che in frequenza. L'adozione di field-plate, ad esempio, ha permesso di migliorare le caratteristiche di breakdown di tali dispositivi, mentre la passivazione si è dimostrata efficace nel migliorarne le prestazioni RF.

Ad oggi svariati dispositivi basati sui nitruri del gruppo III hanno attirato l'attenzione della comunità scientifica. I diodi in GaN hanno dalla loro un'alta tensione di breakdown e un'alta velocità dei portatori; le applicazioni di potenza quali switch RF, convertitori dc-dc, nonché l'amplificazione di segnali RF rappresentano i principali campi in cui gli HFET in AlGaN/GaN trovano applicazione grazie all'alto breakdown, alla capacità di operare ad alte temperature e alle alte correnti sostenute. Diversi restano tuttavia i problemi di affidabilità, tra cui i fenomeni di degradazione osservati sia durante il funzionamento in continua, sia a radiofrequenza. Da tempo nuovi studi e nuove ricerche vengono costantemente portati avanti per ottenere un quadro sempre più ampio ed esaustivo dei fenomeni fisici che compromettono l'operatività di questi dispositivi.

In questa tesi verrà investigata l'affidabilità degli HEMT in GaN sia sul fronte del funzionamento dc sia a radiofrequenza, tramite analisi sperimentali e simulazioni, in modo da identificare e spiegare i nuovi fenomeni osservati, aggiungendo ulteriori tasselli allo studio dell'affidabilità degli HEMT in GaN. Verranno inoltre investigate le possibilità di applicazioni innovative dei nitruri del gruppo III, e in particolare del GaN: da una parte le attraenti proprietà fisiche, dall'altra la libertà di ingegnerizzazione, rendono interessante la

prospettiva di strutture deputate alla conduzione per lacune, con l'obiettivo di ottenere degli HEMT in GaN a canale p: finora, nonostante previsioni teoriche promettenti, l'osservazione di lacune nel nitruro di gallio è stata sporadica, pertanto verrà studiata la possibilità di ottenere un gas bidimensionale di lacune in nuove strutture basate sui nitruri del gruppo III. Verranno studiate inoltre le proprietà dell'ossido di alluminio come dielettrico di gate ad alta costante dielettrica su GaN, da una parte per le basse correnti di leakage consentite, e dall'altra per verificare la possibilità di ottenere un gas bidimensionale di lacune in strutture con GaN di tipo p.

Abstract

In the last decades the technological market has been experiencing a constant increase towards applications requiring a high information content like mobile, broadband/multiband or satellite telecommunications, beside military-oriented applications like radars or extreme-environment applications. The requirements of the devices meant to satisfy these needs are a high transmission speed, a high efficiency, and the possibility to work at higher frequency, with higher efficiency. Two materials have gained attention and investments thanks to their properties: Gallium Nitride (GaN) and Silicon Carbide (SiC). They both have high bandgap, which makes them excellent candidates, but GaN is favored by its versatility, being able to form heterojunctions with other III-Nitrides, and thanks to its direct bandgap. A wide variety of systems both for electronic and optic applications can therefore be exploited. In the last years the reliability of GaN-based devices was intensively studied, and several technological solutions were engineered to overcome the problems found both in dc and RF operation. The use of field-plates, for instance, has proven to be useful to increase the breakdown voltage, whereas passivation was found to be beneficial for the RF performance.

To date, several III-N-based devices have gained the attention of the scientific community. GaN-based diodes have a high breakdown voltage and a high carrier velocity; power applications like RF switches, dc-dc converters, and RF signal amplification are among the main areas of application for AlGaN/GaN HFETs thanks to their high breakdown voltage, high operation temperature, and high currents. However, reliability problems affecting such devices include degradation both during dc and RF operation. Research has been consistently carried out to gain more and more insight on the physical phenomena compromising the behavior of such devices.

In this dissertation the reliability of GaN HEMTs will be investigated in both dc and RF working conditions by means of experimental analyses and numerical simulations, in order to identify and explain the observed new phenomena. Also, the possibilities of innovative devices based on III-Nitrides, and GaN in particular, will be studied: the attractive physical properties and the degrees of freedom offered in designing such structures make the perspective of structures for hole conduction appealing in order to put the bases for actual p-channel HEMTs: so far, despite theoretical predictions, few observations of 2-dimensional hole gas (2-DHG) have been reported, therefore the possibility of hole conduction in new III-N structures will be investigated. The properties of Al_2O_3 as high-k dielectric on GaN will be

also studied, due to the low gate leakage currents allowed, and the theoretical possibility to obtain a 2-DHG with p-type GaN.

Acknowledgments

The first person I want to thank for contributing to the completion of my PhD is Alessandro. I couldn't be happier to study with him and to learn from him notions, methods, and much more. He is the advisor every student would like to have. He gave me the opportunity to join Siddharth's group and to work with excellent people and researchers. The next person I want to thank is Siddharth. Under his supervision I had the opportunity to expand the horizon of my research studies including design, fabrication, and more.
Thank you Ale and Siddharth, working with you was truly a remarkable experience.

I want to thank my lab mates in Modena: Enrico, Davide, Paolo, Vincenzo, Federica. A very special thank you goes to Michele, for the help he's provided me with throughout my PhD years. I learned the first things about working in a cleanroom with him, and his help was always very important. Thank you everybody.

I want to thank also my lab mates in Professor Rajan's Group in Columbus: Pil Sung (you're the man), Sriram, Digbijoy, Fatih, Edwin, Ting. I am not a grower and therefore want to thank the growers (Sriram and Digbijoy) for the hours they've spent in the MBE lab and the advice. You are a super group and your support during my time with you was very important, I always learnt new things and I appreciated it very much indeed.

Devo inoltre dei ringraziamenti speciali a:

Mamma e Papà, per aver sopportato la mia lontananza.
Francesca, per il prezioso supporto e l'insostituibile compagnia.

Vita

Born in Modena, Italy, on 30 September 1982

October 2005

B.S. in Electronic Engineering

Information Engineering Department

University of Modena and Reggio Emilia, Modena, Italy

April 2008

M.S. in Electronic Engineering

Information Engineering Department

University of Modena and Reggio Emilia, Modena, Italy

2009-2011

PhD student in Electronics and Telecommunication Engineering

Information and Communication Technologies Doctorate School

Information Engineering Department

University of Modena and Reggio Emilia, Modena, Italy

2011

Visiting Research Scholar at the Electrical and Computer Engineering Department, The Ohio State University, Columbus (Ohio), U.S.A.

Publications

Journal Papers

1. A. Chini, **V. Di Lecce**, M. Esposto, G. Meneghesso, and E. Zanoni, "Evaluation and Numerical Simulations of GaN HEMTs Electrical Degradation", ***IEEE Electron Device Letters***, Vol. 30 no. 10, Oct. 2009, pp. 1021–1023.

2. **V. Di Lecce**, M. Esposto, M. Bonaiuti, G. Meneghesso, E. Zanoni, F. Fantini, and A. Chini, "Experimental and simulated dc degradation of GaN HEMTs by means of gate-drain and gate-source reverse bias stress", ***Microelectronics Reliability***, Vol. 50, no. 9-11, Sep.-Nov. 2010, pp. 1523–1527

3. **V. Di Lecce**, M. Esposto, M. Bonaiuti, F. Fantini, G. Meneghesso, E. Zanoni and A. Chini, "An Investigation of the Electrical Degradation of GaN High-Electron-Mobility Transistors by Numerical Simulations of DC Characteristics and Scattering Parameters", ***Journal of Electronic Materials***, Vol. 40, no. 4, Apr. 2011, pp. 362–368.

4. M. Esposto, **V. Di Lecce**, M. Bonaiuti, and A. Chini, "The influence of interface states at Schottky junction on the large signal behavior of Copper-gate GaN HEMTs", *submitted on* ***Microelectronics Reliability***.

5. A. Chini, **V. Di Lecce**, F. Fantini, G. Meneghesso, and E. Zanoni, "Analysis of GaN HEMTs Failure Mechanisms during DC and large-signal RF Operation", *submitted on* ***IEEE Transaction on Electronic Devices***.

6. **V. Di Lecce**, S. Krishnamoorthy, M. Esposto, T.-H. Hung, A. Chini, and S. Rajan, "Metal-oxide barrier extraction by Fowler-Nordheim tunnelling onset in Al2O3-on-GaN MOS diodes", *submitted on* ***IET Electronics Letters***.

Conferences and Workshops

1. A. Chini, **V. Di Lecce**, M. Esposto, G. Verzellesi, S. Lavagna, A. Cetronio, and C. Lanzieri, "Trapping phenomena in field-plated high power GaAs pHEMTs", *17th European Heterostructure Technology Workshop—**HETECH 2008***, Venice (Italy), Nov. 2008

2. E. Zanoni, M. Meneghini, A. Tazzoli, N. Ronchi, A. Stocco, **V. Di Lecce**, M. Esposto, A. Chini, and G. Meneghesso, "Reverse gate bias stress induced degradation of GaN HEMT", *36th International Symposium on Compound Semiconductors—**ISCS 2009***, Santa Barbara CA (USA), Sep. 2009

3. M. Esposto, **V. Di Lecce**, A. Chini, S. De Guido, A. Passaseo, and M. De Vittorio, "Comparison of Cu-gate and Ni/Au-gate GaN HEMTs large signal characteristics", *39th European Solid-State Device Research Conference—**ESSDERC 2009***, Athens (Greece), Sep. 2009

4. A. Chini, **V. Di Lecce**, M. Esposto, G. Meneghesso, and E. Zanoni, "RF Degradation of GaN HEMTs and its correlation with DC stress and I-DLTS measurements", *European Microwave Week—**EuMW 2009***, Rome (Italy), Sep. 2009

5. G. Meneghesso, M. Meneghini, A. Tazzoli, N. Ronchi, A. Stocco, E. Zanoni, **V. Di Lecce**, M. Esposto, and A. Chini, "GaN HEMT Degradation Induced by Reverse Gate Bias Stress", *8th International Conference on Nitride Semiconductors—**ICNS-8 2009***, Jeju (South Korea), Oct. 2009

6. **V. Di Lecce**, M. Esposto, M. Bonaiuti, F. Fantini, A. Chini, G. Meneghesso, and E. Zanoni, "Influence of RF drive and switching frequency on degradation mechanisms in GaN HEMTs", *18th European Heterostructure Technology Workshop—**HETECH 2009***, Günzburg/Ulm (Germany), Nov. 2009

7. M. Esposto, **V. Di Lecce**, M. Bonaiuti, F. Fantini, G. Verzellesi, S. De Guido, M. De Vittorio, A. Passaseo, and A. Chini, "Influence of interface states at Schottky junction on

the large signal behaviour of Cu-gate standard AlGaN/GaN HEMTs", *18th European Heterostructure Technology Workshop—**HETECH 2009***, Günzburg/Ulm (Germany), Nov. 2009

8. D. Saguatti, **V. Di Lecce**, M. Esposto, A. Chini, F. Fantini, G. Verzellesi, S. Boulay, A. Bouloukou, B. Boudjelida, and M. Missous, "Design of field-plated InP-based HEMTs", *18th European Heterostructure Technology Workshop—**HETECH 2009***, Günzburg/Ulm (Germany), Nov. 2009

9. A. Chini, F. Fantini, **V. Di Lecce**, M. Esposto, A. Stocco, N. Ronchi, F. Zanon, G. Meneghesso, and E. Zanoni, "Correlation between dc and RF degradation due to deep levels in AlGaN/GaN HEMTs", *2009 International Electron Devices Meeting—**IEDM 2009***, Baltimore MD (USA), Dec. 2009

10. **V. Di Lecce**, M. Esposto, M. Bonaiuti, F. Fantini, and A. Chini, "Study of GaN HEMTs Electrical Degradation by Means of Numerical Simulations", *40th European Solid-State Device Research Conference—**ESSDERC 2010***, Sevilla (Spain), Sep. 2010

11. **V. Di Lecce**, M. Esposto, M. Bonaiuti, G. Meneghesso, E. Zanoni, F. Fantini, and A. Chini, "Experimental and simulated dc degradation of GaN HEMTs by means of gate-drain and gate-source reverse bias stress", *21st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis—**ESREF 2010***, Gaeta (Italy), Oct. 2010

12. M. Esposto, P. S. Park, D. N. Nath, S. Kryshnamoorthy, F. Akyol, **V. Di Lecce**, A. Chini, and S. Rajan, "Design of GaN HEMTs for Power Switching Operation", *19th European Heterostructure Technology Workshop—**HETECH 2010***, Fodele (Crete), Oct. 2010

13. **V. Di Lecce**, M. Esposto, M. Bonaiuti, G. Meneghesso, E. Zanoni, F. Fantini, and A. Chini, "Study of GaN HEMTs degradation by numerical simulations of scattering parameters", *19th European Heterostructure Technology Workshop—**HETECH 2010***, Fodele (Crete), Oct. 2010

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Introduction to Gallium Nitride Electronics

The need for high-speed and high-power electron devices is constantly increasing, following the demand for affordable and reliable solutions capable of supporting the advances in the field of Information and Communication Technology. In the last decades, two requirements have become more and more important in order to follow the demands of the market for telecommunications: the increase in the amount and speed of information to be carried, and in the power to be transmitted. On one hand, this requires devices capable of operating at higher frequencies, and materials suitable to sustain high voltages and currents in order to obtain higher power levels. Silicon, though its mature state, has proven by now to be inappropriate for such applications. The attention was therefore shifted to new materials, in particular III-V compound semiconductors, Gallium Arsenide (GaAs) being one of the most representative and mature of them.

The first studies on the accumulation of charges at an heterojunction date back to the late 1960s. In the 1970s the fabrication of such devices became possible thanks to the development of more precise epitaxial growth techniques. In the first 1980s the first GaAs-based HFETs were fabricated. GaAs-based devices pushed the limit of operation frequency further than Silicon, thanks to new structures like the Heterojunction Field-Effect Transistor (HFET) or Modulation-Doped Field-Effect Transistor (MODFET). In such structures, heterojunctions were used to create two-dimensional carrier gas thanks to the principle of modulation doping, that is, putting doping in a different region to add carriers in the device channel. This led to much higher mobility values and higher currents, since no scattering would occur. However, Gallium Arsenide's bandgap (1.42 eV) is not much higher than Silicon (1.12 eV), and therefore the improvements in terms of power or temperature of operation were not as significant as they appeared to be when GaN HFETs were fabricated,

in the 1990s. In Table 1.1 some material parameters are summarized for Silicon, Gallium Arsenide, Silicon Carbide, Gallium Nitride, and Diamond.

	Si	GaAs	4H-SiC	GaN	Diamond
E_g *(eV)*	1.12	1.42	3.26	3.39	5.45
n_i *(cm^{-3})*	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}	1.6×10^{-27}
ε_r	11.8	13.1	10	9	5.5
μ_n *(cm^2/V s)*	1400	8500	700	1200 / 2000 *	1900
v_{sat} *(10^7 cm/s)*	1	1	2	2.5	2.7
E_{br} *(MV/cm)*	0.3	0.4	3	3.3	5.6
λ_T *(W/K cm)*	1.5	0.43	3.3–4.5	1.3	20

* for Bulk / 2DEG

Table 1.1: Material properties for different semiconductors [1]

Thanks to its wide bandgap, GaN has a higher breakdown field and a much higher temperature of operation. The higher mobility yields a much faster operation compared to Silicon, and the higher carrier velocity leads eventually to a higher cutoff frequency and a higher current. Therefore, it appears as an exceptional candidate for high-power, high-frequency, and high-temperature applications. An additional confirmation comes from specific figures of merit (FOM). Johnson's FOM describes the power-frequency product per unit width [2]:

$$FOM_{Johnson} = \frac{(v_{sat} E_{br})^2}{2\pi} \tag{1.1}$$

Y. Wu [3] indicated Baliga's FOM [4] as a proper indicator for the efficiency of GaN HEMTs:

$$FOM_{Baliga} = \mu E_{br}^2 \tag{1.2}$$

High-efficiency devices have high breakdown field and high mobility (therefore low access resistance). If we compare these FOMs for the materials in Tab. 1.1, we notice again the superiority of GaN (Tab. 1.2).

	Si	GaAs	4H-SiC	GaN	Diamond
$FOM_{Johnson}$	0.014	0.025	5.7	10.8	36.4
FOM_{Baliga}	126	1360	6300	13 000	60 000

Table 1.2: Figures of merit for different semiconductors (a.u.)

The III-Nitride system includes mainly binary materials Gallium Nitride (GaN), Aluminum Nitride (AlN), Indium Nitride (InN). Boron Nitride (BN) is still a someway immature semiconductor material [5]. At room temperature, the bandgap of InN has been recently suggested to be about 0.8 eV [6] and the bandgap of AlN is 6.2 eV [7], so the III-N material system covers a very broad range of energies (and emission wave lengths) from the infrared to the deep ultraviolet like no other system or material. The possibility to combine these compounds in ternary or quaternary alloys, together with the relatively small variation in the lattice constants, leads eventually to an enormous variety of structures thanks to band engineering. In Fig. 1.1 the bandgap of III-N and other semiconductor materials are reported versus the lattice constant at a temperature of 300 K.

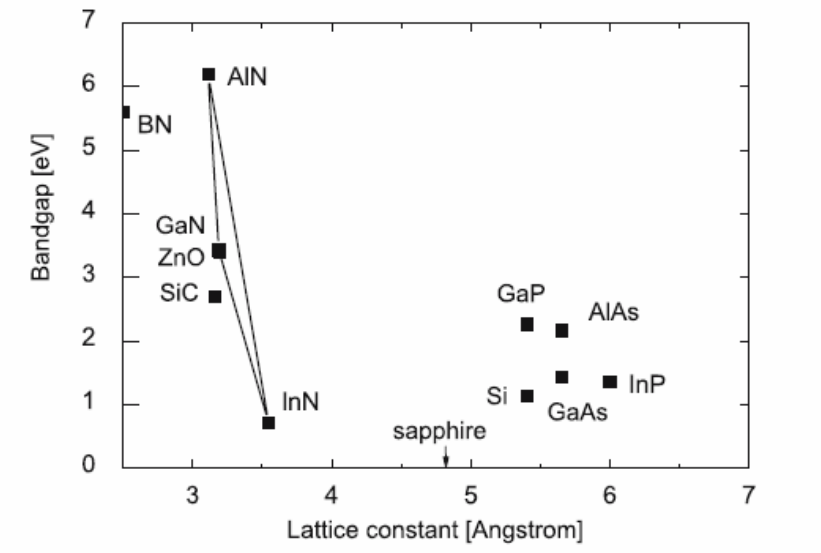

Fig. 1.1: Bandgap of III-N and other semiconductor materials versus the lattice constant at 300 K [8]

One distinctive feature of the III-N system materials is their strong polar nature, which will be discussed further in section 1.2. Due to this, any change in a III-N alloy composition changes the crystal properties and therefore the interface charge is modified too. So, in the end it appears clear that one key of the success of III-N materials is the interface properties rather than intrinsic bulk material transport properties.

1.2 Polarization of III-Nitrides for Electronics

1.2.1 Zinc Blende lattice structure

The Zinc Blende is the less common, less useful, and less stable lattice structure in which III-N semiconductors can be grown. It is reported here for the sake of completeness.
It is composed by the interpenetration of two Face Centered Cubic (fcc) lattices, displaced from each other by a distance $(\frac{a}{4}\ \frac{a}{4}\ \frac{a}{4})$ along the body diagonal, where a is the lattice constant. If the two atoms of the basis are identical, the structure is called Diamond (Si, Ge, C fall in this category). If the two atoms are different, the structure is called the Zinc Blende structure (GaAs, AlAs, CdS fall in this category, as well as III-Nitrides in their most unstable form).

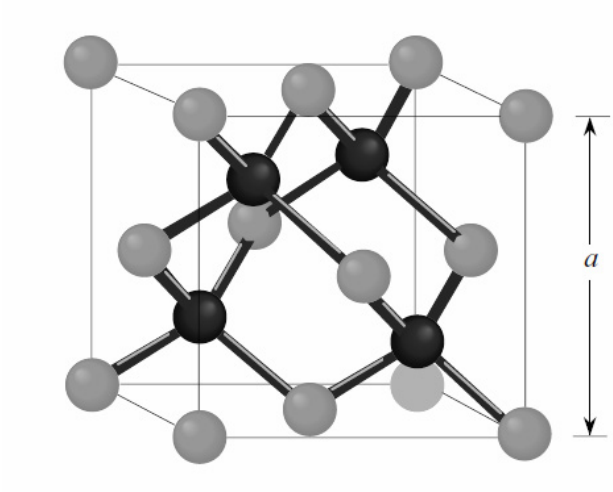

Fig. 1.2: The Zinc Blende crystal structure [9]

One thing to note is that in this structure inversion symmetry is absent. Therefore materials with this lattice structure are piezoelectric, i.e., when they are strained an electric potential is developed across the opposite faces of the crystal. Without any strain applied, no spontaneous polarization is present.

1.2.2 Wurtzite lattice structure

The Wurtzite is the most stable form in which III-Nitrides can be found, and it is also the most interesting from the engineering point of view, as we shall see in section 1.2.3. It is composed by the interpenetration of two Hexagonal Close Package (hcp) lattices, displaced

from each other along the *c* axis by a distance equal to 5/8 of the cell height. Nitrogen sits on one of the two sublattices, while the III material (Ga in GaN) sits on the other one.

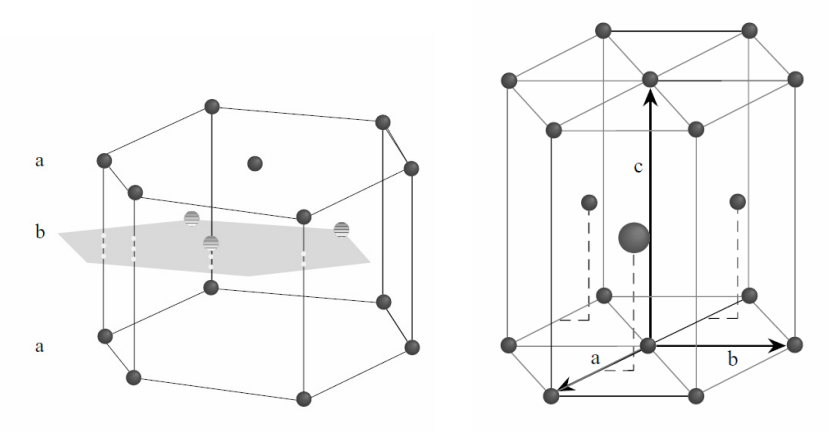

Fig. 1.3: (left) Interpenetration of two hexagonal lattices with a displacement and (right) arrangement of lattice points on a hcp lattice [9]

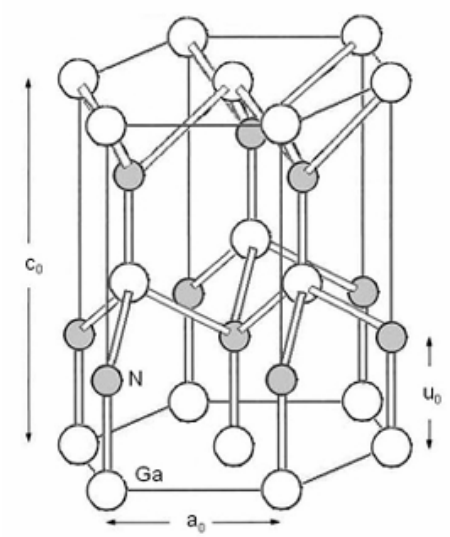

Fig. 1.4: The lattice unit cell for GaN in the Wurtzite form

The lattice vectors a_1, a_2, a_3 are denoted as *a*, *b*, *c* (Fig. 1.3). In an ideal structure, $a=b$ and c/a is approximately 1.633. However, this is not the case in actual III-N semiconductors like GaN, AlN and InN, as reported in Table 1.3, where the cation-anion bond length ratio along the [0001] axis *u* is also reported.

	a_0 [Å]	c_0 [Å]	c_0/a_0	u_0/c_0
GaN	3.1892	5.185	1.6258	0.377
AlN	3.1106	4.979	1.6008	0.3821
InN	3.538	5.703	1.6119	0.377

Table 1.3: Lattice constants for III-Nitrides in Wurtzite form [10]

1.2.3 The origin of polarization

One reason for the strong polarization along the c axis which characterizes III-Nitride materials is that the wurtzite crystal structure lacks inversion symmetry. This leads to a strongly polar structure, for the unit cell is terminated along the c axis with Gallium (or Aluminum, or Indium) on one side, and with Nitrogen on the other side. Moreover, the bond that lies along the c (0001) axis is rather ionic than covalent, for Nitrogen is the element with the highest electronegativity in group V. This is the reason for the intrinsic, or spontaneous polarization of III-Nitrides. It is called spontaneous because it only takes into account the volume density of the electric dipoles formed without strain.

	GaN	*AlN*	*InN*
P_{SP} (C m^{-2})	-0.029	-0.081	-0.032

Table 1.4: Parameters for the spontaneous polarization of III-Nitrides [11]

Piezoelectric effects were though considered the main responsible for the formation of sheet carrier densities in GaN devices [12]. All the binary III-Nitrides and their ternary and quaternary alloys have different lattice constants. This was not an obstacle in the design III-Nitride heterostructure systems, thanks to strained heteroepitaxy, by which a different material can be grown on top of another one (within a certain critical thickness) inducing a tensile or compressive strain on the top layer so that it can keep the same lattice constant of the substrate without giving rise to dislocations, which would happen if the top layer was relaxed. A piezoelectric polarization is induced therefore along the c axis in a strained layer of wurtzite-type III-N semiconductor, which can be calculated as [13]:

$$P_{PE} = 2\frac{a_L - a_S}{a_S}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \tag{1.3}$$

where e_{ij} are the piezoelectric constants, a_L and a_S are the lattice constants along the hexagonal edge of the top layer material and of the substrate, and C_{ij} are the elastic constants.

1.3 AlGaN/GaN HEMTs

1.3.1 Ga-polar and N-polar structures

III-Nitrides like GaN can be grown along different axes, with a different impact on the electric properties of the final structure. Different planes in the wurtzite structure have in fact different polar properties. The most common are summarized in Table 1.5.

Plane	*Feature*
(0001)	Polar
(11-20)	Semi-polar
(1-100)	Semi-polar
(10-1-3)	Non polar
(10-1-1)	Non polar
(11-2-2)	Non polar

Table 1.5: Polar, semi-polar, and non polar planes in the wurtzite crystal structure

The most favorable growth direction for III-Nitrides in electronics is (0001), for the polar charges accumulating at the interfaces can be used to engineer several device structures, as we shall see in section 1.3.2. However, semi-polar surfaces have been studied too and they are involved in optoelectronic applications. A comprehensive analysis of the development and perspectives of semi-polar and non polar surfaces is reported in [10].

We shall focus on the (0001) growth direction. A large part of the research activity both on electronic and optoelectronic GaN devices has been carried out on Ga-terminated layers, because of the much better stability of the growth, and remarkable results are reported in

literature for Ga-face systems. However, one of the next challenges will be to develop a comparably stable and good growth standard for N-polar devices too, thanks to growth techniques like molecular beam epitaxy (MBE): the availability of a reversely polarized material may push the potentialities and flexibility of the GaN-based electronic and optoelectronic systems even further.

1.3.2 Polarization-induced charges for device design

We shall now review the basic AlGaN/GaN HEMT structure and investigate the reason for the formation of a 2-Dimensional Electron Gas (2-DEG) for the Ga-polar case; then we will illustrate the most interesting features of a N-polar GaN HEMT.

In Fig. 1.5 the ball and stick representation model of Ga-face GaN and the associated crystal polarization is depicted. In the bulk material the net polarization is zero, for the $\pm Q_\pi$ charge at the top and bottom of each unit cell compensate each other. However, if the net dipole at the end of the GaN layer was not screened, an unsustainable dipole moment would form, as can be inferred from a few calculations.

Being the spontaneous polarization Q_π (previously indicated as P_{SP}) in GaN -0.029 C/m^2, the spontaneous polarization charge density will be:

$$\sigma_{SP,GaN} = \frac{P_{SP,GaN}}{q} = 1.81 \times 10^{13}\, cm^{-2} \tag{1.4}$$

The electric field is therefore:

$$F_\pi = \frac{Q_\pi}{\varepsilon} = \frac{q \cdot \sigma_{SP,GaN}}{\varepsilon} = 3.68 MV/cm \tag{1.5}$$

This dipole charge eventually results in a voltage across the material proportional to its thickness. Given a thickness d = 0.5 μm, that would be:

$$V_\pi = F_\pi \cdot d = 184V \tag{1.6}$$

A screening dipole appears therefore to be essential in order to sustain such voltage values.

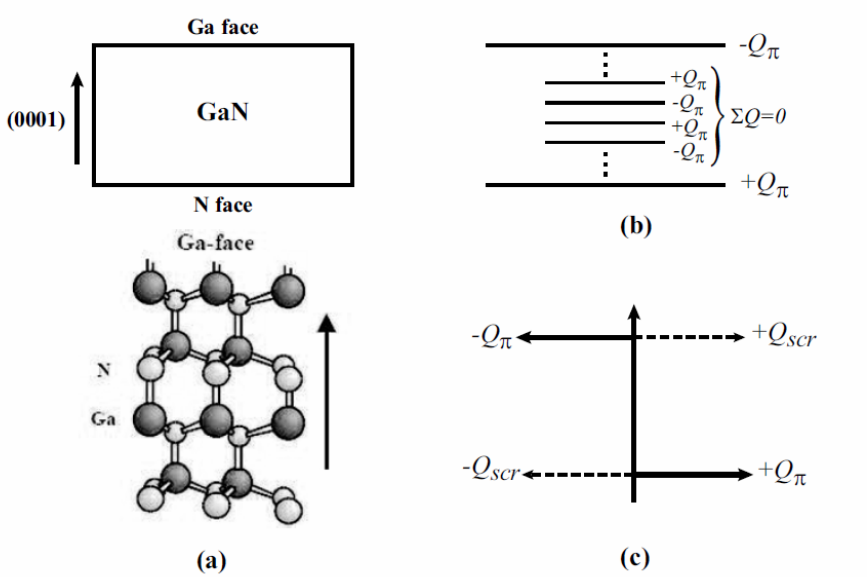

Fig. 1.5: (a) Ball and stick representation of a GaN wurtzite crystal structure. (b) Polarization charge model in a polar material. (c) Formation of screening charge to screen the polarization dipole. [14]

Let us follow the steps of the growth of a Ga-face AlGaN/GaN HEMTs. We shall assume in the first place that no surface states are present. We shall also assume that the background n-doping of GaN has a negligible effect compared to the electric field generated by the polarization charges. When a slightly n-doped GaN is grown, the band structure will keep its slope given by the electric field as in (1.3), so the valence band will cross the Fermi level after a certain thickness d_{cr}. When this occurs, holes begin to accumulate at the surface, while electrons are pushed towards the interface between GaN and the substrate, and so a screening dipole is eventually created (Fig. 1.6)

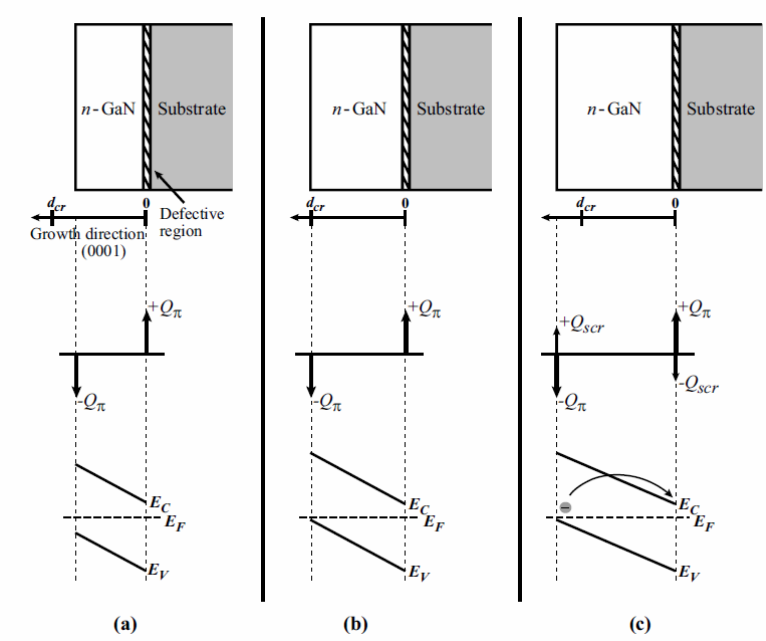

Fig. 1.6: Growth of an n-type GaN layer, with charge profile and band diagram (a) at the beginning of the growth. (b) at $d=d_{cr}$ (c) for $d>d_{cr}$. [9]

As the thickness of the material keeps increasing, the polarization dipole becomes more and more screened, until $Q_{scr} \rightarrow Q_\pi$ for d $\rightarrow \infty$. Actually, it has been demonstrated that a surface donor state exists, and that it is responsible for the formation of the 2-DEG [15-16]. The situation in this case is very similar: the difference is that the screening charge is not provided by holes, but by the ionized surface donors (Fig. 1.7).

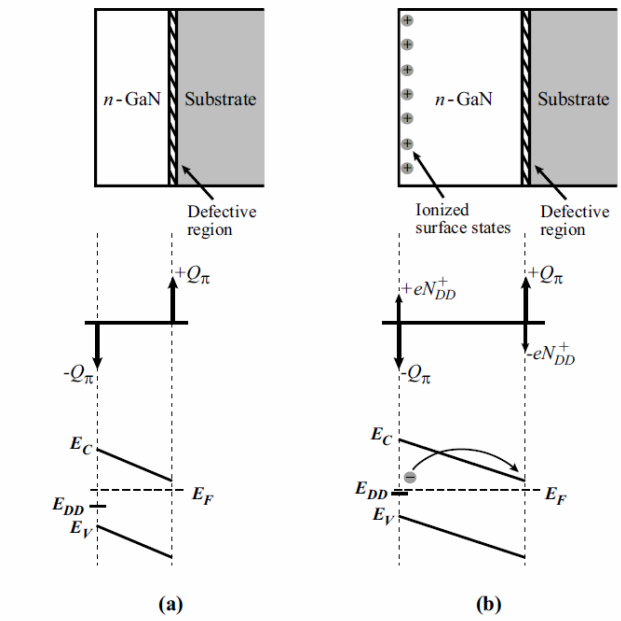

Fig. 1.7: Growth of an n-type GaN layer, with charge profile and band diagram (a) at the beginning of the growth. (b) when surface donor states ionize and screen polarization charge [9]

Now if an AlGaN layer is coherently grown on top of the GaN, it will be lattice-matched to it, and therefore will have a piezoelectric polarization component in addition to the spontaneous one. The bad diagram of the structure that is being created if the AlGaN layer is sufficiently thick is reported in Fig. 1.8. In this case, the surface potential happens to be pinned by the surface donors, and a distribution of electrons in the GaN close to the AlGaN/GaN interface is present. These electrons are confined in a triangular quantum well, therefore are allowed to move only in the plane perpendicular to the growth directions, forming a 2-Dimensional Electron Gas (2-DEG).

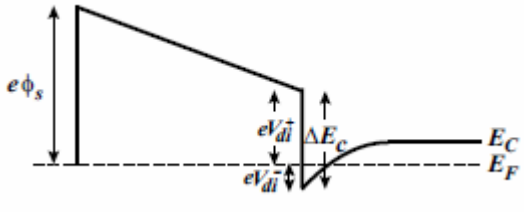

Fig. 1.8: AlGaN/GaN HEMT band diagram [9]

As the barrier thickness decreases though, the 2-DEG sheet density decreases too, until the point where the ionization of surface donors is no more sufficient to donate enough charge to the 2-DEG, for the underlying GaN layer becomes depleted. Typical Aluminum molefraction for state-of-the-art Ga-polar HFETs are between 22% and 35%.

N-polar GaN has gained attention for the potentialities offered by the reversed direction of polarization in order to design new structures, potentially superior to Ga-polar devices, even though the growth of N-terminated samples is more challenging. One advantage of N-polar HEMTs is the lower gate leakage: an AlGaN cap on top of the structure would prevent carriers from tunneling from the gate, providing a higher and more effective barrier [17] (Fig. 1.9).

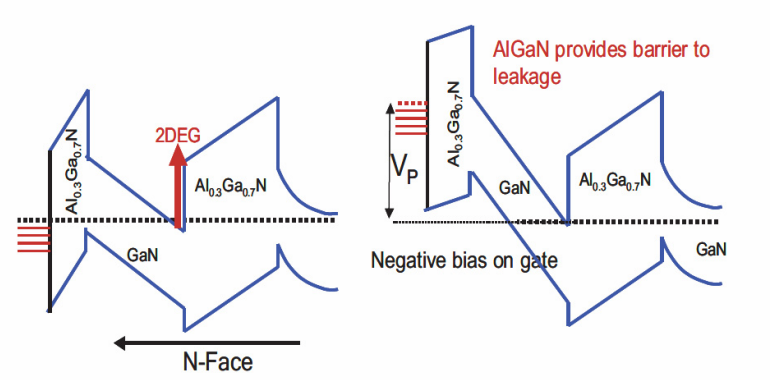

Fig. 1.9: N-polar AlGaN/GaN/AlGaN HEMT with no bias (left) and negative bias applied (right) [18]

Another application of N-polar GaN HEMTs is enhancement-mode devices. Such devices are important for high-voltage switching or digital electronics, and a way to fabricate them using Ga-polar materials is by a gate recess: by lowering the thickness of the AlGaN barrier, the pinning of the band at the surface forces the channel to get depleted. However, one disadvantage of this approach is the lack of control of the etching, and therefore of the threshold voltage. By using N-polar materials, a structure in which the access regions are etched away can be designed, being now the gate region depleted (Fig. 1.10).

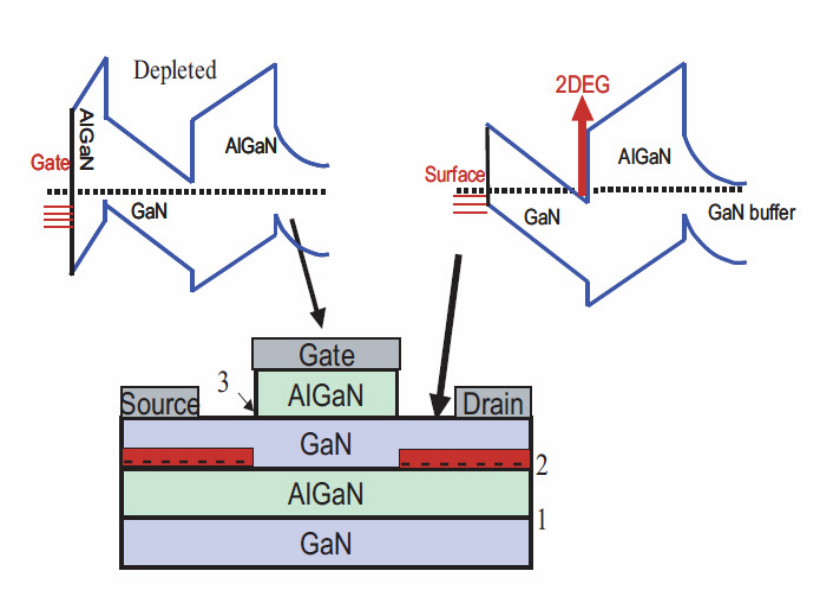

Fig. 1.10: N-polar enhancement-mode GaN HEMT [18]

1.4 Overview of the dissertation

In chapter 2 some of the most critical and addressed reliability issues of Gallium Nitride HEMTs are reported, including dc-to-RF dispersion, dc degradation, power degradation, and gate leakage. Solutions to such problems will be presented too.

In chapter 3 we investigate the correlation between dc and RF degradation of GaN HEMTs by means of measurements and stress tests. Details about the measurement setup will be provided. A study on the dependence of degradation mechanisms on the RF drive level is also reported.

In chapter 4 a study of the dc degradation of GaN HEMTs by means of stress tests and numerical simulations is reported. Additional AC simulation results are reported in order to verify the correlation between the transconductance and the cutoff frequency.

The work described in chapters 3 and 4 was carried out at the Department of Information Engineering of the University of Modena and Reggio Emilia, Modena, Italy.

In chapter 5 the current status of the research about p-channel conduction in GaN HEMTs is reviewed, and structures for the achieving of p-type conduction are proposed.

In chapter 6 the properties of high-k dielectric Al_2O_3 on GaN are studied, in order to verify the possibility of hole accumulation and to gain a better understanding of such structures.

The work described in chapter 5 and 6 was carried out at the Electrical and Computer Engineering Department of The Ohio State University, Columbus (Ohio), USA.

Chapter 2

Reliability of GaN HEMTs

2.1 Device degradation in GaN HEMTs

The degradation of an active device like an FET can be described in two ways. The first is by monitoring the variation of a certain parameter or figure of merit (like the drain current I_D, the gate current I_G, the transconductance g_m, or the RF output power) over time, in a ordinary working condition. The second is by waiting for a sudden catastrophic event (like a breakdown in a material layer) to occur. Both ways can provide information on the reliability of the device. Accelerated testing procedures, which are becoming more and more critical as the innovation of the field of Information and Communication Technology proceeds, are based on the second way. They make a wide use of statistics in order to estimate features like Mean Time to Failure (MTTF), Mean Time to First Failure (MTFF) or the FIT rate with accuracy and reproducibility, and therefore appear more market-oriented. The first approach is the one adopted for the studies carried out in this dissertation. In the next paragraphs, the main reliability issues of GaN HEMTs will be reviewed.

2.2 Frequency dispersion

Probably the best known and most addressed issue affecting GaN HEMTs is frequency dispersion (also referred to as dc-to-RF dispersion). Its main effect is a discrepancy between the expected value of the output RF power as predicted from static I-V curves, and actual measurements. It appears to be very critical for III-Nitrides: in the Gallium Arsenide (GaAs) system, such phenomenon has been observed and discussed [19], but the eventual effects on the device performance were not so pronounced. III-Nitrides instead have properties that play in favor of dispersion, among which are:

- A high surface charge density (~ 10^{13} cm^{-2})
- The lattice mismatch between III-Nitrides themselves and compared to the substrate
- The occurrence of defects such as threading dislocations due to the high growth temperatures (up to 1100°C for the MOCVD)

The most established believing is that dispersion is originated by typically either surface or bulk traps [20,21], even though a number of situations can be summarized as follows (Fig. 2.1):

1. Semiconductor/dielectric surface traps [22]
2. Barrier bulk traps [23]
3. Channel/barrier interface traps
4. Buffer bulk traps [21]
5. Substrate/buffer interface traps and/or in the nucleation layer [24]

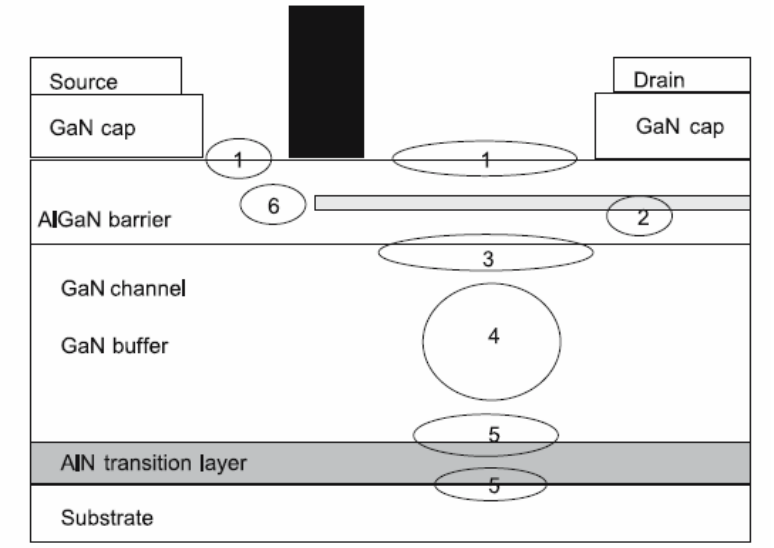

Fig. 2.1: Locations of traps in an AlGaN/GaN HEMT [8]

The effects of both surface [25-28] and bulk traps [24, 29-30] have been addressed in a high number of works. A modeling for the dispersion phenomena originating by cases 1 and 4 is reported in Fig. 2.2.

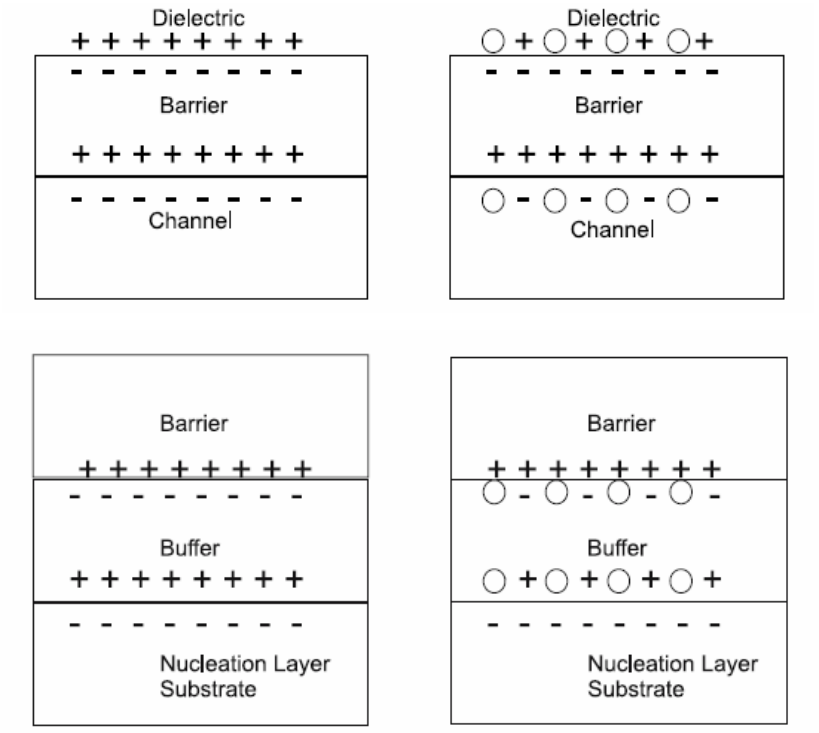

Fig. 2.2: The effects of traps at the dielectric/semiconductor interface (above) and in the buffer layer (below) [8]

If traps are present either on the surface or in the buffer layer, the time they get to reach steady-state after the bias of the device is changed may lead to serious limitations in their working frequency. A typical example of how traps act in this sense is the following. Consider a generic HEMT structure with no traps (Fig. 2.3). When a bias is applied, for instance from pinch-off to open channel, the device will respond quickly and the drain current transient will be very fast.

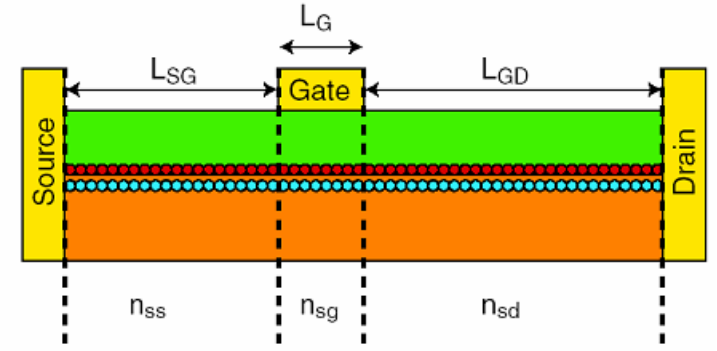

Fig. 2.3: Standard HEMT structure with no surface traps.

On the other hand, if surface traps are present (Fig. 2.4), the time response of the device will be characterized by a two-step transient, for the traps will take a certain time to extinguish their influence (Fig. 2.5 and 2.6).

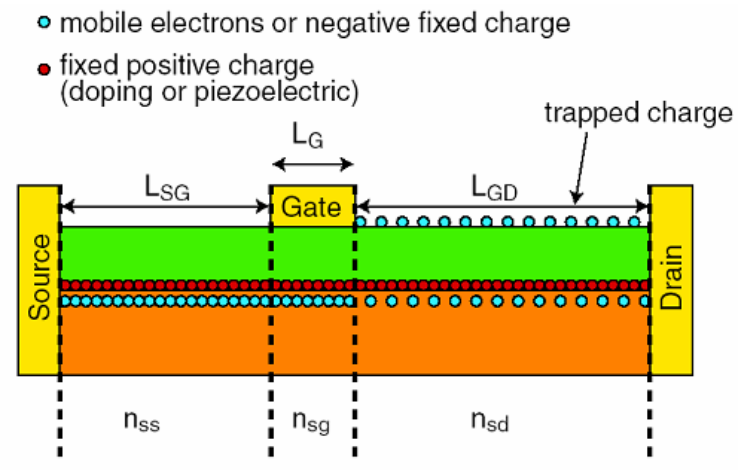

Fig. 2.4: Standard HEMT structure with surface traps.

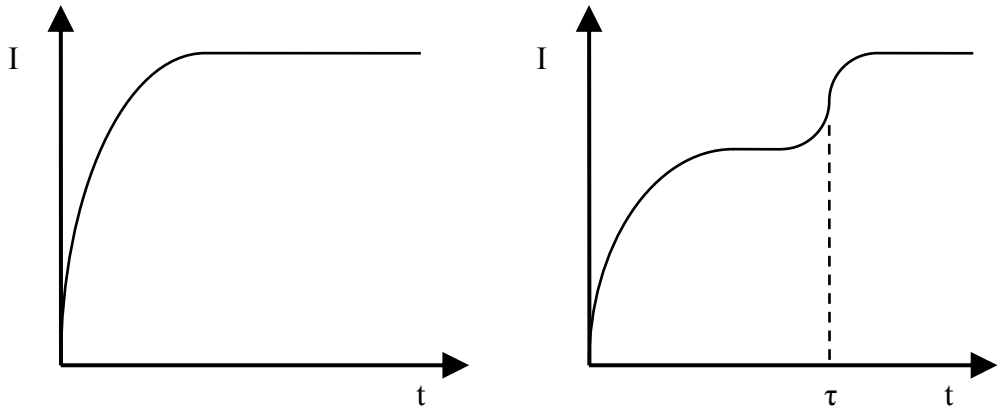

Fig. 2.5: Qualitative drain current time transients for a device without (left) and with traps (right).

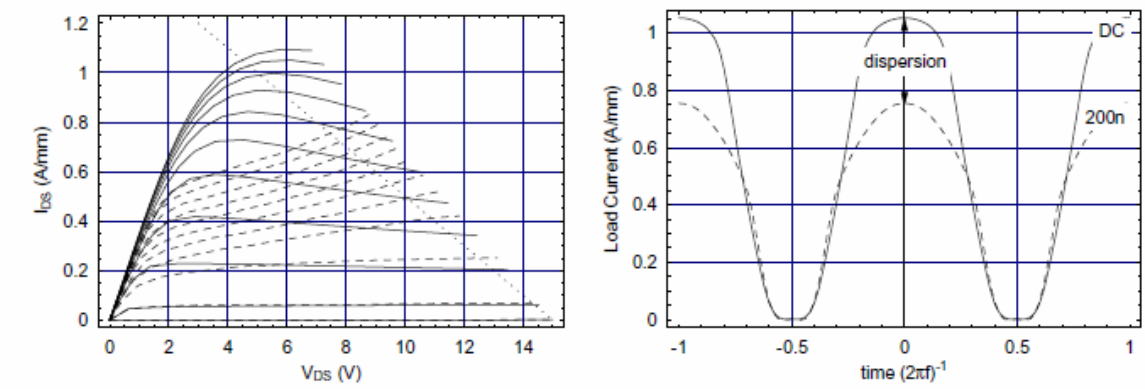

Fig. 2.6: Effect of dc-to-RF dispersion in an AlGaN/GaN HEMT. (left) dc (solid line) and 200ns (dashed line) pulsed IV characteristics. (right) Current obtained by driving the gate with a sine wave [31]

Among the technological solutions proposed to overcome such problems are surface passivation, field-plate structure, and gate recess technology.

2.2.1 Surface passivation

In the III-Nitride system there is no native oxide, like SiO_2 for Silicon. The most popular dielectric is Silicon Nitride (Si_3N_4). Its beneficial effects in preventing dispersion to occur were studied in many works [32,33]. Among the advantages achieved by the SiN passivation in GaN HEMTs are an increase of the output power [34], a reduction of the dc-to-RF dispersion [32], whereas inconveniences like an increase of the leakage have been observed [31].

2.2.2 Field-plate structures

One issue of GaN-based HEMTs is that they usually do not take advantage of the attractive breakdown properties of wide-bandgap materials, due to the significant electric field peaks occurring at the drain end of the gate contact. The function of the field-plate is to modify the electric field distribution along the structure, decreasing its peak and broadening it. In this way the high-bandgap properties of III-Nitrides can be exploited, leading to higher breakdown voltages, and eventually to higher RF power, helping preventing dispersion effects from occurring too. However, trade-offs have to be always taken into account anyway when dealing with these solutions. There are different variants of field-plate structures. The simplest is just an additional metal layer on top of the SiN passivation (Fig. 2.7).

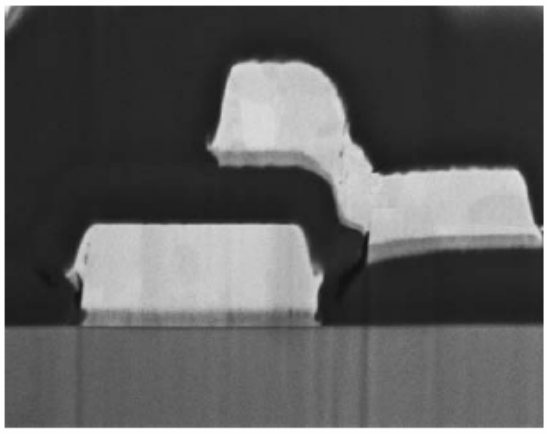

Fig. 2.7: Image of a gate structure with a field plate on top [8]

Another way of implementing a field-plate structure is by connecting it to one of the device terminals. In the first place, this terminal was the gate itself. This led to exceptional improvements in power performance and high-voltage operation (Fig. 2.8).

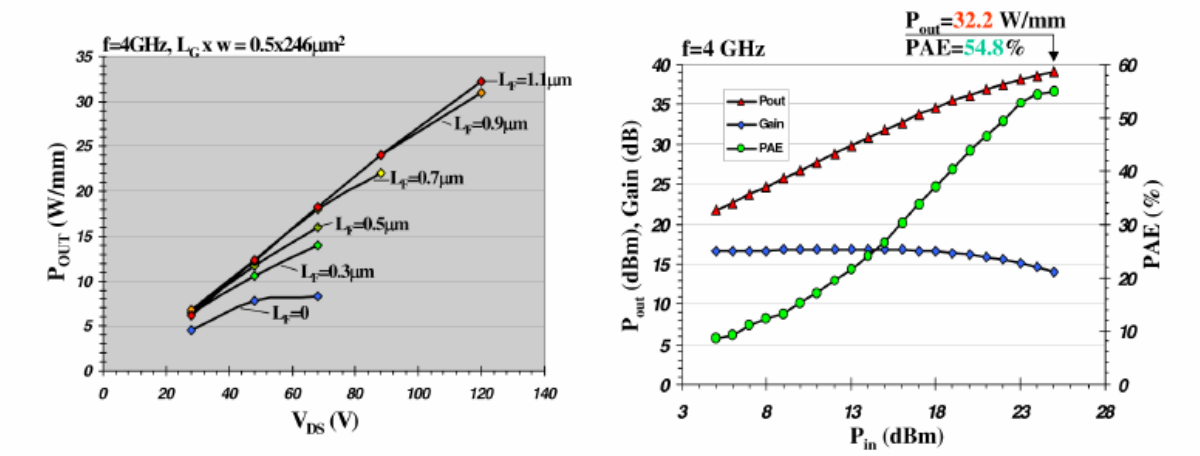

Fig. 2.8: Output power versus drain voltage for different field-plate lengths (left) and power performance of a GaN HEMT with a gate-connected field-plate (right) [35]

However, a major drawback of this configuration is the increase of the gate-drain capacitance C_{GD}, which eventually causes a decrease in the current-gain cut-off frequency f_T and in the power-gain cut-off frequency f_{max}. Things can be improved by choosing a source-connected field-plate configuration, in which the gate-source capacitance C_{GS} is increased, being disadvantages in this case absorbable by the tuning networks. Additional attractive techniques like multiple field-plates have also been proposed in order to achieve higher breakdown voltages [36].

2.2.3 Gate-recess technology

Since the effect of the surface traps on the channel is inversely proportional to the distance between them, one way to reduce dispersion effects is to grow very thick AlGaN or GaN caps to increase the surface-to-channel distance. In [37] a breakdown voltage of 90V was achieved in a GaN/AlGaN/GaN structure, as well as an output power density of 12W/mm and a PAE of 40.5% at 10GHz without surface passivation (Fig. 2.9).

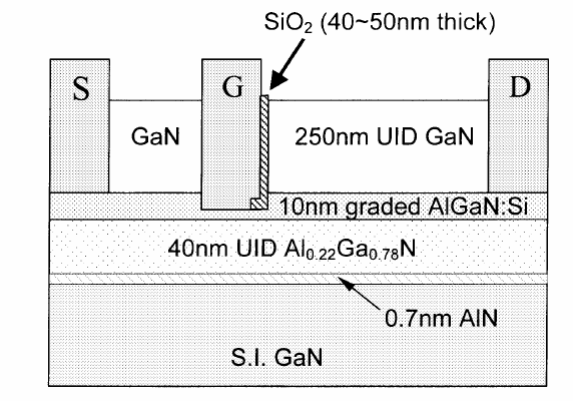

Fig. 2.9: GaN/AlGaN/GaN HEMT structure with thick caps to reduce dispersion [37]

2.3 DC degradation

DC degradation experiments can be carried out either at high temperature or at room temperature. In the first case they are typically aging tests, and are designed in order to extract information about figures of merit like mean time to failure (MTTF). DC stress experiments at room temperature have pointed out characteristic findings that include the reduction of the transconductance g_m, the change of Schottky barrier height, the reduction of the drain current I_{DSS}, and the increase of the access resistance.

Probably the most remarkable results in this field have been obtained by J. Del Alamo and his research group, having identified in the "inverse piezoelectric effect" one characteristic failure mechanism of III-N devices, and of AlGaN/GaN HEMTs in particular [38]. The application of a constant reverse bias to the gate of an AlGaN/GaN HEMT led to the abovementioned aging effects, the reason being in a defect formation in the AlGaN layer as a result of a high vertical field at the edge of the gate. The piezoelectricity of III-Nitrides is one of the reason of their ability to form heterojunctions suitable for making transistors. However, if the strain accumulated in the AlGaN layer due to the difference in the lattice constant with GaN leads to a charge accumulation (therefore to a potential), similarly the application of an external voltage may have the same reverse effect on the strain of the structure. If the total strain exceeds a critical value, strain can relax through defect formation, such as dislocations. Crystallographic defects bring along traps which may result in a reduction in the sheet carrier concentration in the channel. This phenomenon is most likely to take place right next to the gate edge, where the fields are highest.

Chapter 3

GaN HEMTs degradation mechanisms in dc and RF operation

3.1 Correlation between dc and RF degradation

In this section we will point out how experimental tests suggest that the mechanism inducing degradation during dc stress tests should be the same as the ones found to cause gate leakage increase during RF stress tests. Measurements and experiments were carried out at the Information Engineering Department within the University of Modena and Reggio Emilia, Modena, Italy. Otherwise specified, tested devices were all standard single-heterojunction $Al_{0.28}Ga_{0.72}N$/GaN HEMTs provided by Selex Sistemi Integrati (Rome, Italy). Tab. 3.1 summarizes their main features.

Growth technique	MOCVD
Substrate	SiC
AlGaN barrier thickness	25 nm
Gate length, L_G	0.25 µm
Total gate periphery, W_G	4 × 25/50/75 µm
Gate-drain spacing, L_{GD}	2.05 µm
Gate-source spacing, L_{GS}	1.4 µm
Passivation layer	SiN

Table 3.1: Features of the devices used in the stress tests and measurements

Typical dc and pulsed output I-V characteristics for fresh devices are reported in Figure 3.1. Maximum drain current for V_{GS}=+1V reaches up to 0.9 A/mm level while pinch-off voltage is approximately -5V. There is little difference between static and dynamic characteristics, suggesting that fresh device performances are not affected by trapping phenomena. Devices

also behave properly during RF operation at 2GHz. As shown in Figure 3.2, when biased at 25V and matched for maximum power, they would yield a 17.5dB small signal gain, and a 5.1 W/mm saturated output power with a 55% peak power added efficiency. The well stabilized technology process, the negligible current collapse observed during pulsed measurements, and their decent large signal performance, make these devices suitable for an analysis of their reliability both during dc and RF stress tests.

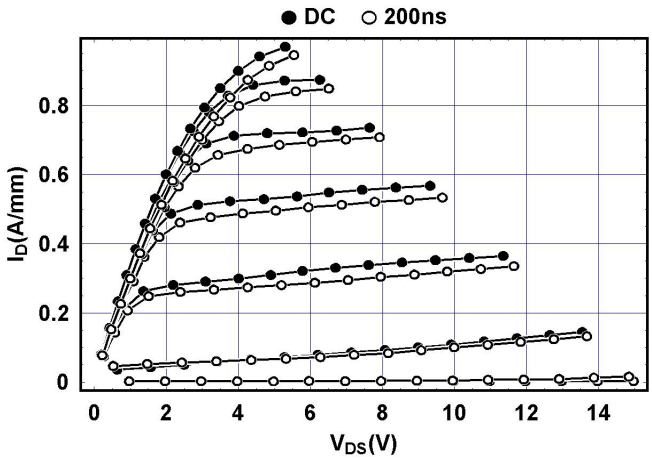

Fig. 3.1: Experimental dc (filled circles) and 200ns pulsed (empty circles) I-V characteristics for a typical fresh device. Gate terminal is pulsed from -6V up to +1V with a 1V step. Negligible current collapse is observed.

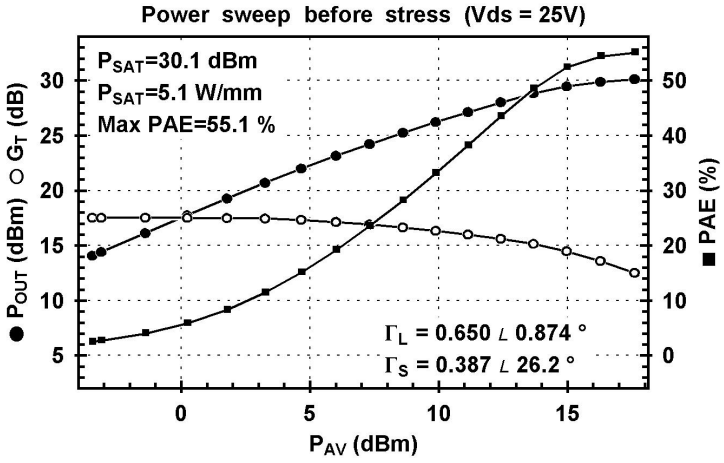

Fig. 3.2: RF power sweep at 2GHz for a typical fresh device. Output power densities measured are above 5W/mm, with peak power added efficiencies over 45-50%.

3.1.1 RF load-pull measurement setup

In Fig. 3.3 a scheme of the RF measurement setup is reported. The RF Power Amplifier provided a 2 GHz continuous wave signal, whereas the controlling/monitoring section

included a RF switch, a Vector Network Analyzer and dedicated software. The bias tees on the sides in Fig. 3.3 are connected to dc voltage supplies and multimeters.

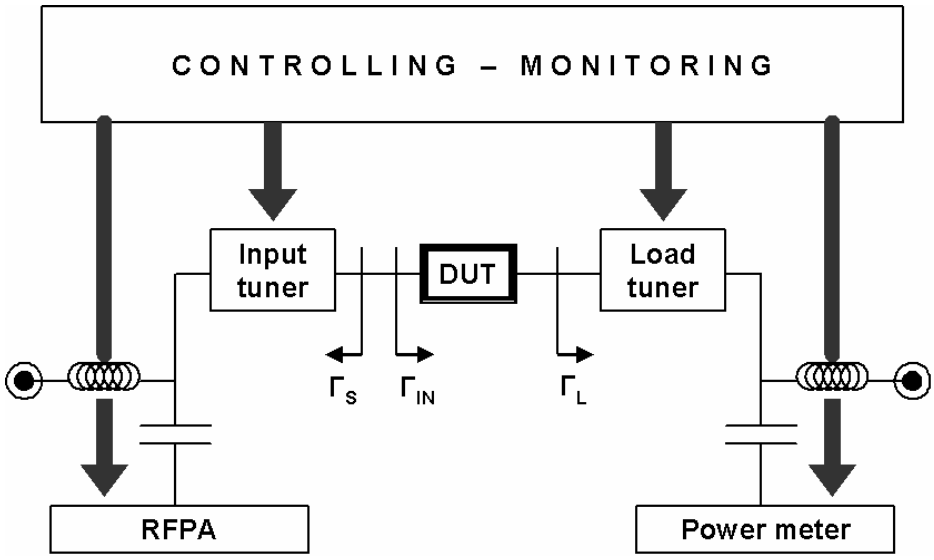

Fig. 3.3: RF measurement setup

As in any load- and source-pull system, tuners can provide the desired matching both for the input and the output port. The input tuner is needed to adjust the source impedance seen by the device under test (Γ_S) and bring it as close as possible to the conjugate of the input impedance of the device itself (Γ_{IN}), in order to maximize the power to the input. The load tuner is needed to adjust the load impedance seen by the DUT. In our measurements and stress tests, we always chose load-line match rather than conjugate match, in order to extract the maximum output power from the device. In Fig. 3.4 and 3.5 the RF probe station rack and a detail of the measurement site are reported.

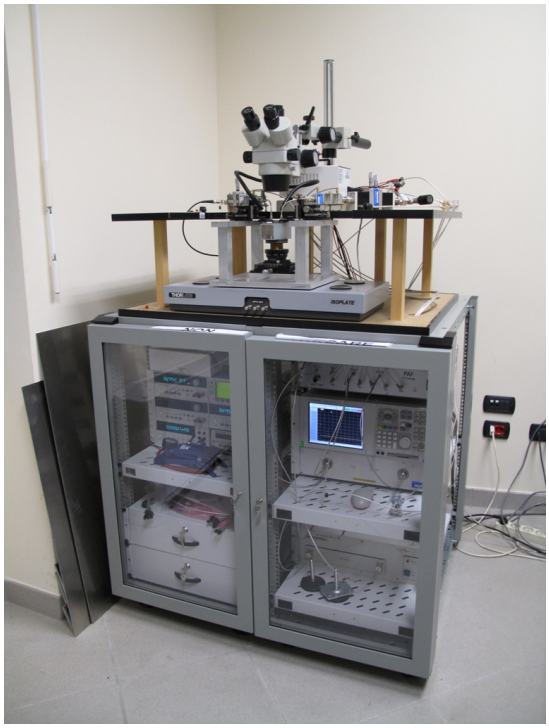

Fig. 3.4: The RF probe station used in the experiments carried out

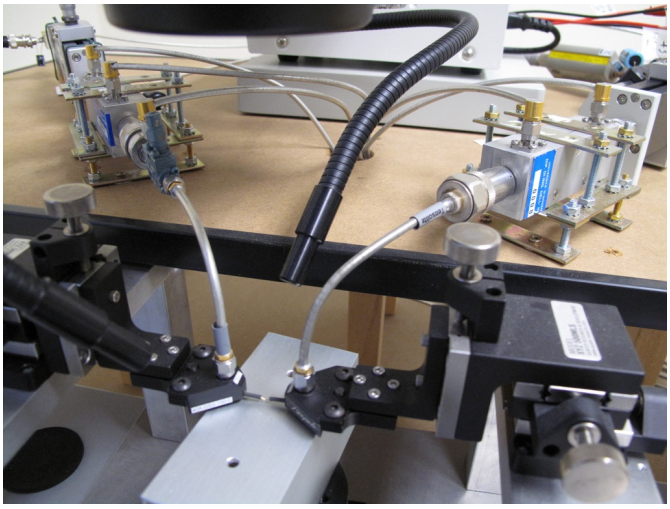

Fig. 3.5: Detail on the sample contact zone

3.1.2 DC reverse voltage stress tests

The dc stress the presented devices were subject to was applied in steps. Details on this experiment have been presented in [39] and will be summarized here. Devices were step-

stressed by applying a negative gate voltage of -5V/step for a total time of 2 min while drain and source were kept at 0V. After each step the following measurements were carried out:

- Dc and 200 ns-pulsed I-V characteristics
- Gate leakage current measurements at V_{DS}=0V and V_{GS}=-8V
- Current-DLTS measurements

A critical voltage of 25V was found for the onset of degradation (reproducible across the wafer) both in the gate leakage current and in the dc-to-RF dispersion, as can be seen from Fig. 3.6. Current-DLTS measurements revealed the presence of defects with an activation energy of 0.5 eV (Fig. 3.7)

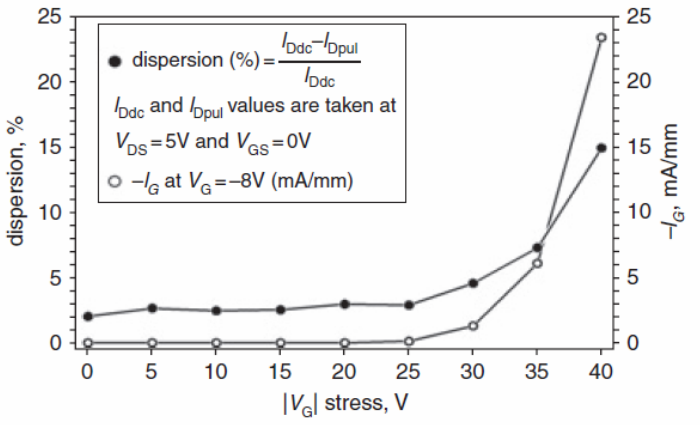

Fig. 3.6: Dispersion coefficient (filled circles) and reverse gate current (open circles) after each stress step [39]

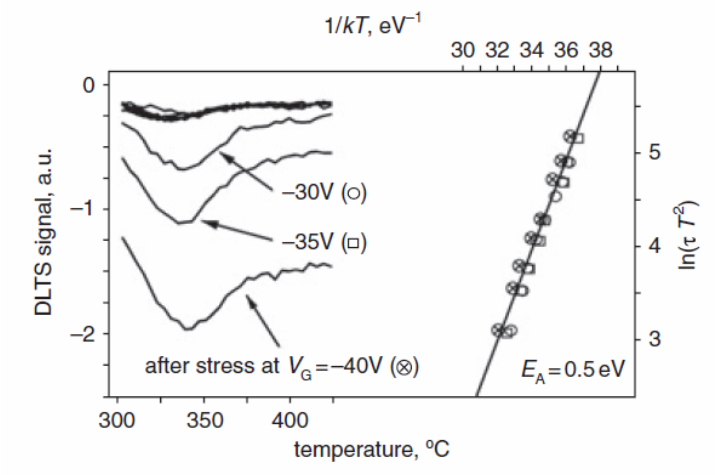

Fig. 3.7: I-DLTS signal and Arrhenius plot during the stress test [39]

Such results found an additional confirm in the study proposed in [40], according to which the observed device degradation can be effectively explained by means of an acceptor trap located 0.5 eV from the conduction band within the device AlGaN barrier, and the decrease in device performance can be related to the increase in trap concentration. These results will be recalled in Chapter 4 too, where a novel analysis on dc degradation mechanisms of GaN HEMTs will be proposed, following the results of that paper.

3.1.3 RF stress tests

In order to correlate the defect found during dc stress tests to the ones arising during RF operation, we carried out RF step stress tests at 2GHz on devices from the same wafer, either pushing them into compression or driving them at a certain output power back-off. Here we report results from different cases without going into the details of the dependence of degradation on the RF drive level: such issue will be addressed in paragraph 3.2.

A set of devices were stressed according to the following schedule:

- Class A operation
- CW signals at 2GHz / 3dB into compression
- V_{DS} increased by 5V every 30min, starting at 10V

Gate leakage was almost negligible (-60μA/mm at V_{DS}=0V, V_{GS}=-8V). Saturated current was about 0.7A/mm and no dispersion was present (Fig. 3.8). Devices were always matched for maximum power at each bias. As can be seen in Fig. 3.9, no significant degradation occurred up to a drain bias of 15V. Increasing the drain bias to 20V resulted in a sudden increase in the gate current after about 12 minutes of operation at 20V. At 25V we observed a slight degradation of the RF performances, about -0.1dBm in output power, and an increase in the reverse gate current. Finally, during the stress test at drain voltage of 30V we did observe a degradation of about 0.3dBm in terms of output power and an increase in gate reverse current from -3mA/mm to -5mA/mm.

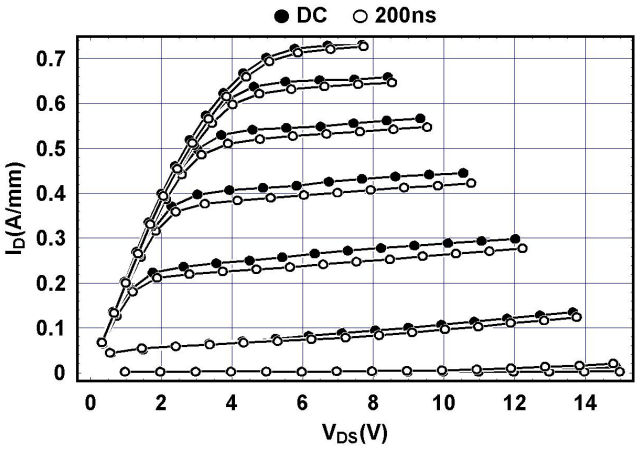

Fig. 3.8: dc and 200 ns-pulsed I-V characteristics of the fresh device. Vgs sweeps from -5V to +1V in 1V/step [41]

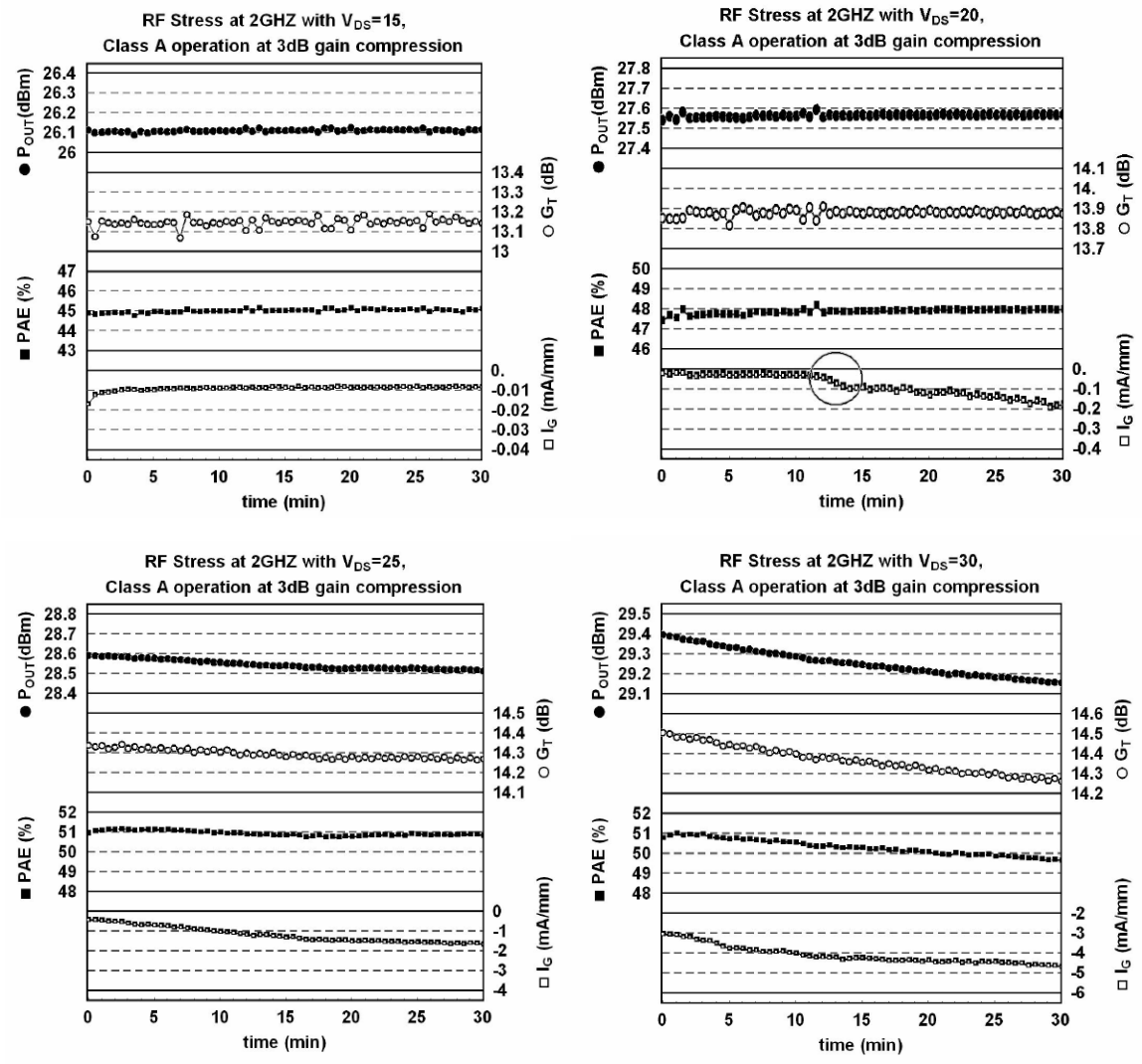

Fig. 3.9: RF stress test carried out up to 30V in Class A 3dB into compression [41]

At this point, dc and pulsed I-V measurements were carried out in order to compare the effects of the RF stress test on device dc and pulsed characteristics: the slight worsening of

the current-collapse is in accordance with the degradation of RF performance (Fig. 3.10). Current-DLTS measurements were also carried out in order to identify if any thermally activated process can be accounted for the observed performance degradation. Measurements were carried out by applying a voltage pulse with a peak value of -6V and a pulse width of 10ms to the gate of the device, while the drain current transient after switching the gate voltage to 0V was measured by I-DLTS technique. The measurements were carried out by biasing the device at V_{DS} values of 5V. As can be seen in Fig. 3.11, an activation energy of 0.5eV was extracted.

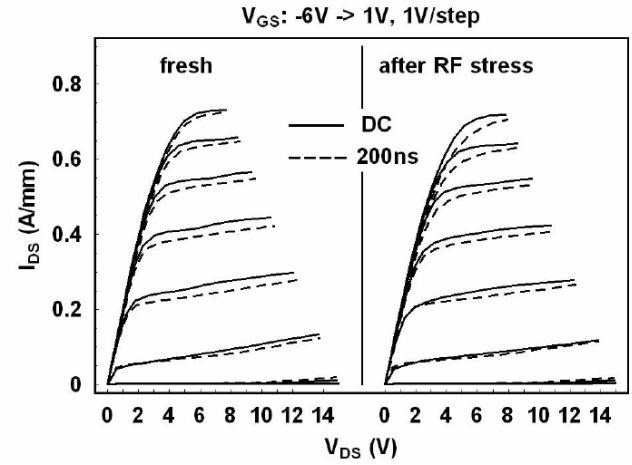

Fig. 3.10: DC (solid lines) and 200 ns-pulsed (dashed line) I-V characteristics measured before and after the RF stress [41]

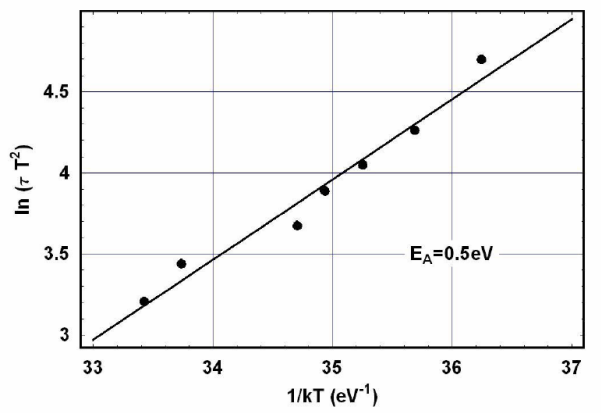

Fig. 3.11: Arrhenius Plot obtained from I-DLTS measurements on a sample after the RF stress test. An activation energy of 0.5eV is obtained [41]

3.2 Dependence of RF drive on degradation mechanisms

Several authors have studied the degradation mechanisms of GaN devices during RF stresses. However, GaN HEMTs have so far been tested mainly at RF drive levels suitable to push the device into compression [42-46]. In [47] two classes of devices were tested during RF stresses in different conditions: unpassivated ones were driven at a low-input power level, whereas passivated ones were driven 1 dB into compression. To the best of our knowledge though, no studies on identical GaN HEMTs stressed both at low and high input power have been reported so far. In [48], devices were tested at T_J=175°C, starting from V_{DS}=40V, I_{DQ}=100mA/mm, and increasing input power in compression from 20 to 26dBm for 5 hours in each stage: the RF stress eventually induced a trapping-related increase in the source resistance, most likely as a result of the creation of new traps, which seems to be strictly related to the presence of the RF signal. We will show that RF drive conditions can affect device robustness: testing devices into compression only may lead in fact to misleading conclusions.

3.2.1 Stress in back-off

Contrarily to conventional literature experiments, we carried out RF stresses on devices at an input power suitable to drive the device 8dB below power saturation. The stress schedule was the following:

- Class AB operation ($I_{D,Q}$ = 25% I_{DSS})
- Initial step-stress: $V_{DS,Q}$ = 15 V up to 30 V (step duration: 1h)
- Stress at constant $V_{DS,Q}$ = 30 V

Devices were always matched for maximum power at each bias. The common feature to all devices stressed at low input power was a severe and sudden degradation by all means, from the output power to the small-signal gain, to the gate leakage current. In Figures 3.12-3.13 and in Table 3.2 the I-V characteristics, power sweeps, and details about the measured degradation for fresh devices and after 6 hours of stress at 30V are reported.

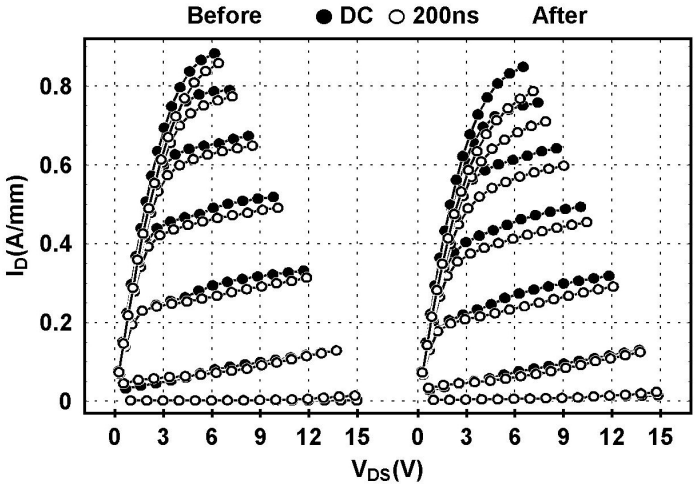

Fig. 3.12: Before-and-after dc and pulsed I-V characteristics for devices stressed in back-off. V_{GS} sweeps from –6V to 1V in 1V/step. Current collapse is evident.

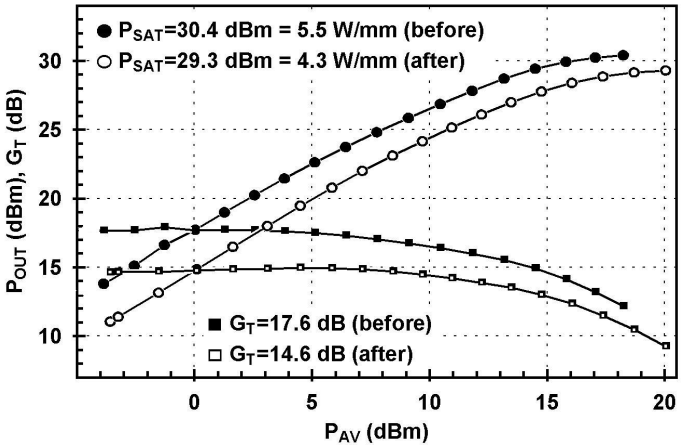

Fig. 3.13: Before-and-after output power and power gain sweeps for devices stressed in back-off

Dc-to-RF dispersion	4%	10%	+ 6 p.p.
P_{SAT}	30.4 dBm	29.3 dBm	– 1.1 dB
$\|I_{G,REV}\|$	0.03 mA/mm	3.4 mA/mm	> + 10^4 %
G_T	17.6 dB	14.6 dB	– 3 dB
PAE_{max}	56.9%	40.4%	– 16.5 p.p.

Tab. 3.2: Before-and-after parameters for the devices stressed in back-off

3.2.2 Stress in compression

An interesting result of our studies is that attention should be paid when carrying out RF stresses into compression, for results could be different according to the time schedule, as we will see. A first set of devices was stressed according to the same schedule introduced in Par. 3.2.1 for the back-off-stressed devices, being the difference in the driving power, now high enough to push the device 3dB into gain compression. Another set was stressed similarly, but keeping stress step duration much lower, only 5 minutes.

From the comparison between the two sets of devices stressed according to the same schedule (step duration 1h) it appears evident that the stress at high power seems to have little or no effect on the device performance: no significant decrease neither in the output saturated power nor in the small signal power gain is observed. The dc-to-RF dispersion does not increase significantly and the gate leakage seems not to be affected by the stress either. Fig. 3.14 shows these differences.

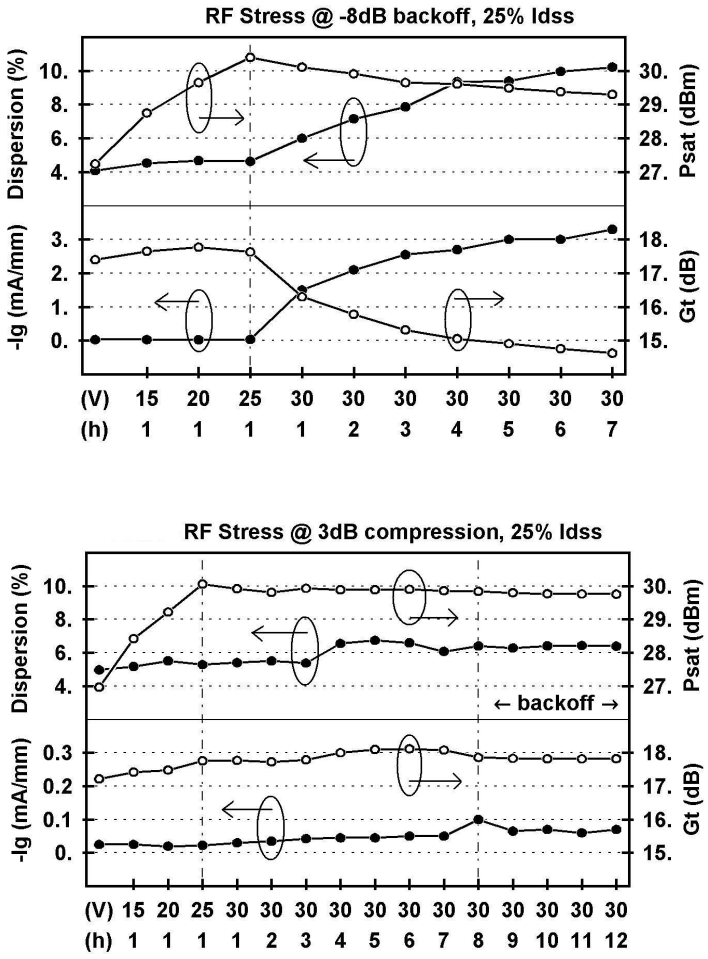

Fig. 3.14: Device parameters variation during RF stress at low power (above) and at high power (below).

As depicted in Fig. 3.14, the most interesting aspect in the stress carried out into compression is the apparent increase in the device robustness: even after being stressed in back-off for an additional time, the devices do not show any sign of degradation. However, this does not mean that the mechanisms triggered by the application of a high-power RF signal are likely to increase the device robustness: if the same compression RF stress is carried out by decreasing the step stress duration to 5 minutes, results are much different, and a severe degradation occurs, similar to the one observed in back-off stressed devices (in Fig. 3.15 the reverse gate current and the incremental variation of the output power after each step are shown).

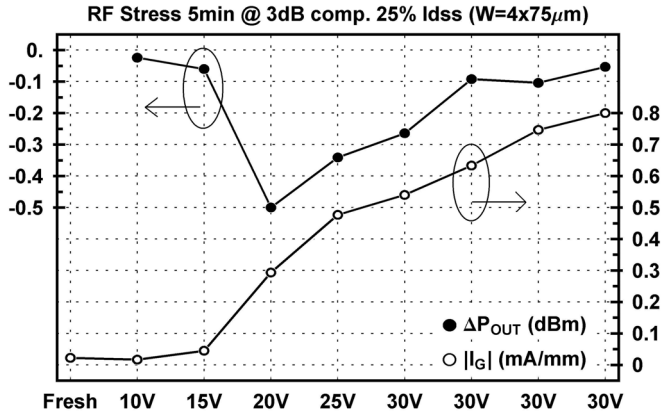

Fig. 3.15: Incremental variation of the output power after each stress step and reverse gate current for devices stressed into compression with a short step duration (5 minutes)

On some of the devices subjected to RF stress, current-DLTS measurements were also carried out in order to study the origin of the observed decrease in power performances: results confirmed the growth of a deep level with an activation energy of 0.5 eV as in the case of dc tests, see Figure 3.16. This suggests that the mechanism inducing the gate leakage increase during the RF tests should be the same already identified during the dc ones. However, the different behavior observed during back-off and compression stresses suggests that another physical mechanism is present, which may improve device robustness.

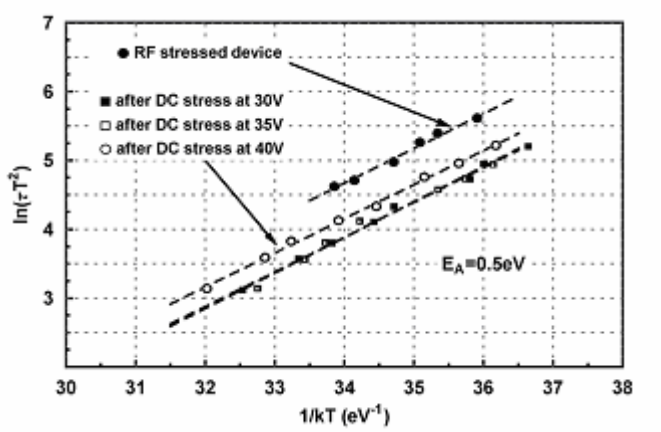

Fig. 3.16: Arrhenius plot derived from current DLTS measurements for devices dc-tested at various V_{DS}, and for RF-tested devices. Both dc and RF tests induce the formation of traps with an activation energy of 0.5eV

3.2.3 Two degradation mechanisms

The experimental results previously described as resulting from the competition of two coexisting degradation mechanisms will be now analyzed. We shall name these two mechanisms (a) and (b). Mechanism (a) arises from defects creation in the AlGaN barrier layer: this enhances dc-to-RF dispersion and increases gate current, through the generation of 0.5 eV deep levels, as described in the previous sections and observed by other authors [40, 49-54]. D. Marcon *et al.* [52,54] have shown that this degradation mode is both electric field and time triggered, which means that if larger bias is applied to the gate, the time required to activate the mechanism is shorter, and vice versa. However, experimental results tell that this is not the only type of failure present, otherwise devices stressed with longer stress step duration would have shown a more severe degradation, for the same electric field was applied for a longer time. The results introduced in Par. 3.2.2 show instead that devices driven into compression degrade much faster when the stress step duration is decreased down to 5 minutes. Therefore, a second mechanism (b) must be present in order to explain the experimental data.

An useful analysis to be carried out before speculating on the nature of mechanism (b) is to estimate the voltage swing and the dissipated power during operation both into compression and in back-off. The dc drain bias was the same in both cases, and was increased by 5V every 60 minutes. However, the maximum and minimum voltages reached during the two stress are significantly different, due to the different drive conditions. Although a correct

calculation of the voltage–current swing during RF measurements is difficult, approximations can be made in order to estimate the actual voltage swing. First, the load impedance can be extracted from the load-pull measurement data, being the reflection coefficient Γ_L known. The load impedance Z_L can then be calculated:

$$Z_L = Z_0 \cdot \frac{1+\Gamma_L}{1-\Gamma_L} = (R_L + jX_L) \tag{3.1}$$

Its equivalent parallel representation will simply have the form:

$$Z_{LP} = (R_{LP} + jX_{LP}) \tag{3.2}$$

Now, if we assume that:

- the reactive component of the load compensates the capacitive component at the device output
- all the harmonics are presented with a short circuit [55,56]

it can be demonstrated that the output RF signal will have a voltage amplitude given by

$$\Delta V = \sqrt{2R_{LP}P_{out}} \tag{3.3}$$

Thus, by calculating ΔV for each of the stress conditions it is possible to estimate the maximum and minimum drain voltage as $V_{DSmax}=V_{bias}+\Delta V$ and $V_{DSmin}=V_{bias}-\Delta V$, respectively. In Tab. 3.3 the maximum drain voltages reached during each of the step stress conditions and the device dissipated power are reported: as can be seen, devices stressed into compression reach larger instantaneous peak voltage levels, up to 54 V during the stress at V_{bias}=30 V, while devices stressed in back-off are subjected to lower voltage levels, i.e. 41 V during the stress at V_{bias}=30 V.

V_{bias}	V_{DSmax}	P_{diss}	V_{DSmax}	P_{diss}
	3dB comp.		-8dB back-off	
15 V	26 V	0.47 W	20 V	0.49 W
20 V	35 V	0.59 W	27 V	0.66 W
25 V	45 V	0.72 W	34 V	0.79 W
30 V	54 V	0.84 W	41 V	0.92 W

Table 3.3: Max. drain voltage and dissipated power for devices stressed into compression and back-off

Despite a significant difference in the devices peak voltages, power dissipation is quite similar for the devices stressed either into compression or in back-off: in back-off both input and output power are lower, but the efficiency is much lower too, so eventually the power dissipation is comparable to that in compression. As can be seen in Tab. 3.3, the dissipated power is very similar for the two sets of devices and is always within a 10% difference. We can therefore state that mechanism (b) is not thermally activated, since device junction temperatures will be similar for both the devices driven into compression and in back-off. In the end, we can propose the following explanation for the observed phenomena.

As we've already stated, two failure mechanisms (a) and (b) are present and partially competing. Mechanism (a) corresponds to the generation of defects, a rather slow process [52,54], which enhances electron injection through tunneling, increasing therefore the gate current and the drain current collapse, as observed during the dc stress test. Mechanism (b) is caused by (hot) electrons injection and trapping over the gate-drain region, a relatively fast mechanisms, which decreases the electric field at the drain edge of the gate terminal and, as a consequence, decreases the gate current. For the devices tested, the generation of defects (a) takes place for dc or average drain voltages larger than 20-25 V, and is mostly linked to the dc component, since it requires longer times compared to the RF signal. The high electric fields instantaneously reached into compression might not last long enough in order to activate (a) but they might be sufficiently long in order to inject hot electrons in the gate-drain access region [28,53] thus activating mechanism (b), which is relatively fast. Once electrons get trapped in pre-existing traps within the SiN layer or at the interface, they induce a decrease of the peak electric field at the gate edge. This explains the increase in robustness of devices during compression tests, due to the lowering of electric fields at the gate edge,

which shifts the onset of mechanism (a). On the contrary, testing in back-off does not significantly enhance mechanism (b), due to the lower peak V_{DS}.

In order to prove the consistency of our proposed explanation, we carried out other experiments. For devices stressed into compression with t_{step}=30min, we evaluated the trend of the drain access resistance by means of end-resistance measurements [57] at the end of each stress step. In Fig. 3.17 the access resistance is reported during the stress: as can be seen, it constantly increased from 1.7 Ω×mm to 2 Ω×mm after the last stress at 30V. These results agree with the injection of (hot) electrons in the gate-drain access region, that is, mechanism (b). It also corresponds to the mechanism of negative charge injection and trapping on pre-existing traps described in [53, 58-59]: a negative charge accumulates in the gate-drain access region, thus decreasing the 2DEG concentration in the HEMT channel increasing the access resistance values [28].

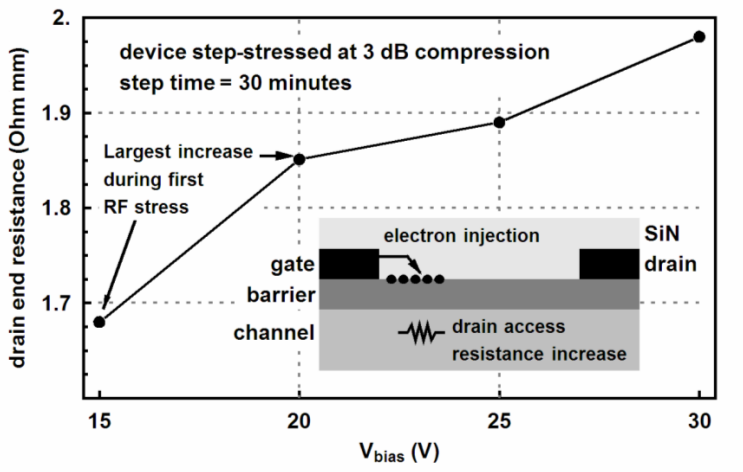

Fig. 3.17: Drain end-resistance at the end of each stress steps into compression. The injection of electrons in the gate-drain access region appears to be the reason for the increase in the access resistance.

Another experiment we carried out in order to verify our assumption was trying to induce both mechanisms (a) and (b) on a same device by alternating back-off and compression RF stress conditions. First, a pre-treatment was carried out by applying a step stress in back-off with short step duration up to a drain bias of 25V, in order to enhance degradation mechanism (a). Then, back-off and compression conditions were alternated at a drain bias of 30V. The schedule of the stress was the following:

- Pre-treatment: fast RF step-stress in back-off up to 25V
- RF stress in back-off at 30V for 30 minutes
- RF stress into compression at 30V for 5 minutes
- RF stress in back-off at 30V for 60 minutes
- RF stress into compression at 30V for 30 minutes

A summary of the trends of the device parameters after each step is reported in Fig. 3.18.

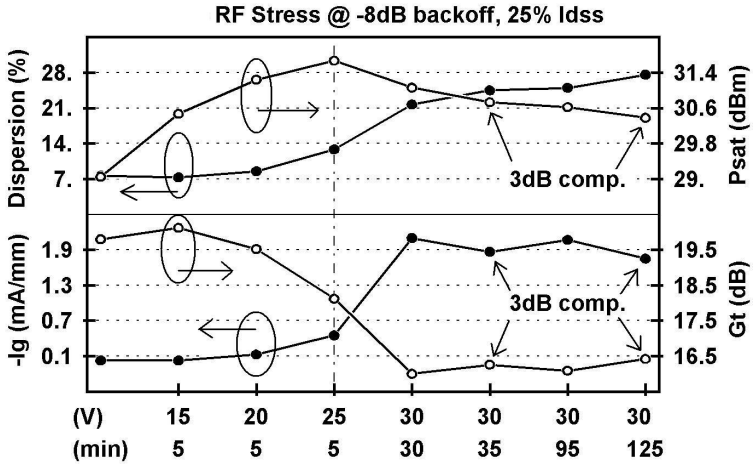

Fig. 3.18: Trend of device parameters after each step for the alternate-drive RF stress. Gate leakage and small-signal power gain improve after the stress steps into compression.

As can be seen, after the steps into compression, the small-signal power gain improves an the gate leakage current (measured at V_{DS}=0V and V_{GS}=-8V) decreases too. This clearly suggests that the two degradation mechanism are competing and can be alternatively dominant, depending on the device operating condition. We shall find proof of this by looking in detail at the gate current during the stress after the pre-treatment (Fig. 3.19).

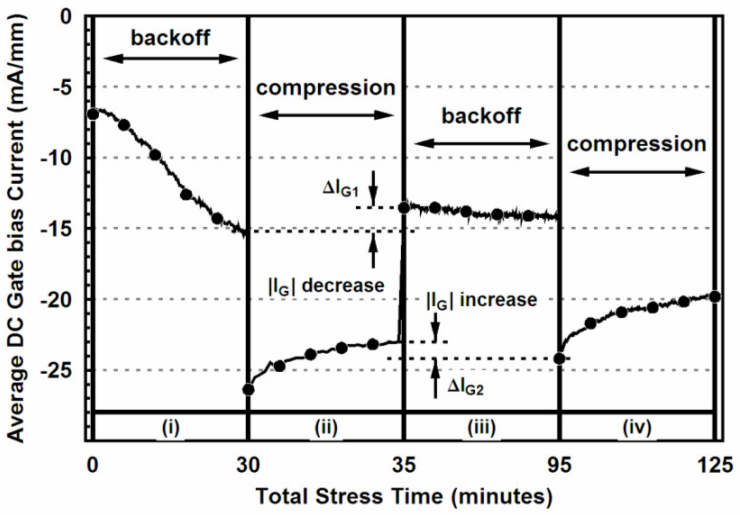

Fig. 3.19: Effect of alternated RF stress on device operation. Discontinuity between steps is due to the change in peak operating drain voltages when switching between back-off and compression (Tab. 3.3).

During the first 30 minutes in back-off, the average reverse gate current increases from 6.5mA/mm to 15mA/mm. This is consistent with the degradation related to mechanism (a) – the formation of defects at the drain-edge of the gate terminal. During the following step in compression (minutes 30–35), electron injection from the gate causes a decrease in the electric field value at the edge of the gate terminal, and the reverse gate current decreased from 26.4mA/mm to 23mA/mm. At the beginning of the next step in back-off (minute 35), the gate current is smaller than at the end of the previous step in back-off (ΔI_{G1} in Fig. 3.19) due to the lower electric field at the gate contact; the reverse gate current then starts to increase again due to the formation of new defects at the edge of the gate (from 13.4mA/mm to 14.1mA/mm). Finally, at the beginning of the last stress step into compression (minute 95), the reverse current is higher than at minute 35 (ΔI_{G2} in Fig. 3.19) because of the increase of trap state density during the previous RF stress in back-off operation; the reverse gate current then decreases again, from 24.2mA/mm to 19.8mA/mm.

A third experiment we carried out to verify our claims aimed to verify the correlation between the generation of defects (a) and the dc component of the voltage applied. As reported, for the devices tested, mechanism (a) takes place for dc or average drain voltages of 20-25 V and higher, and appears to be linked to the dc component, since it requires longer times compared to the RF signal. Fresh devices were subjected to pulsed gate stress: they were switched between on- and off-state by applying to the gate a square wave signal with a frequency span of 100Hz to 1MHz. A 550Ω load line was used, so that the off-state drain voltage could reach up to 60V – almost like during the RF stresses into compression – with

an on-state bias point in the linear region at a drain voltage of about 1V and a current not higher than 0.3A/mm (see Fig. 3.20). This is the reason why we call this type of experiment "pseudo-RF" stress.

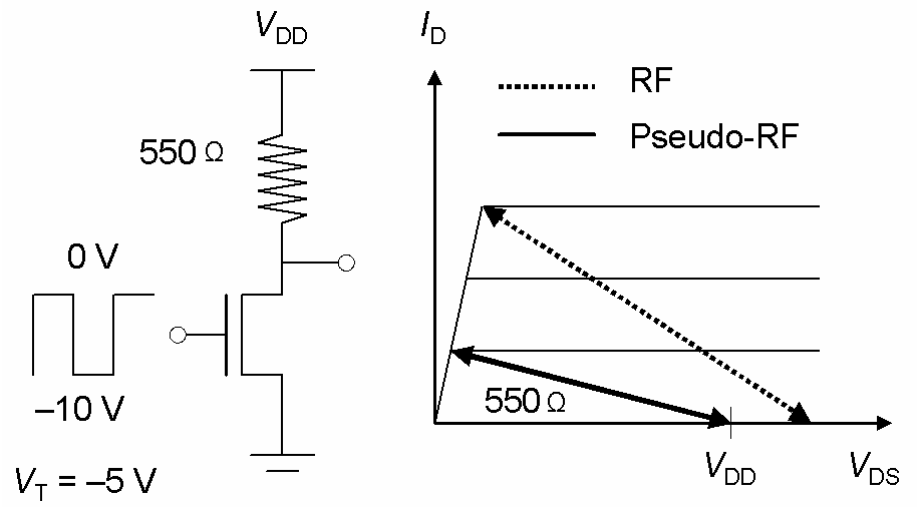

Fig. 3.20: Measurement setup for pseudo-RF stresses. A qualitative trajectory of the bias point is shown.

The frequency was initially 1MHz, and the off-state drain voltage was increased from 20V to 60V in 5V/step. The frequency was then reduced down to 1kHz and switched between 1kHz and 1MHz, with an eventual stress at 100Hz, for a total time of 22 hours. We monitored the reverse gate current, measured with a steady V_{GS}=–8V and V_{DS}=0V. As we expected, at lower frequencies – i.e., closer to dc – the gate leakage keeps increasing, whereas at higher frequencies, although it does not clearly decrease, it remains constant (see Fig. 3.21).

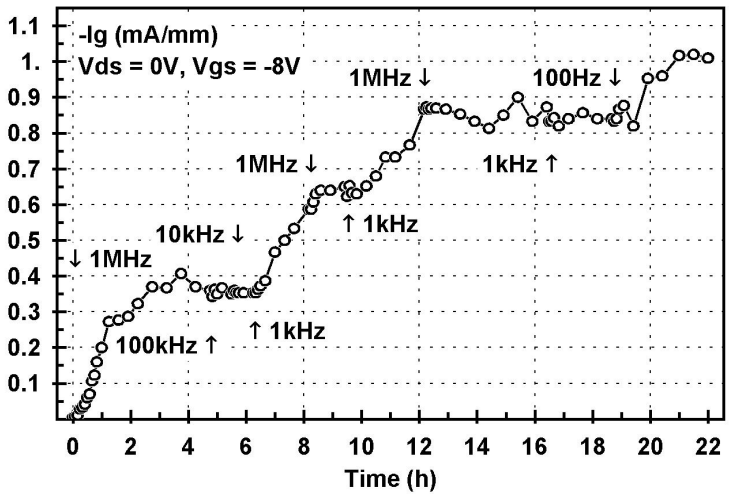

Fig. 3.21: Results of pseudo-RF stress campaign. In the first 45 min V_{DD} increased from 20V up to 60V.

In conclusion, we have shown that two degradation mechanisms are present and compete during RF stresses of GaN HEMTs: the effects of one or of the other can be emphasized by changing the RF stress power.

When the device is driven into compression, electron trapping in the gate-drain access region is enhanced due to the higher peak voltage, which supports fast trapping phenomena. Defects formation in the AlGaN barrier layer is accelerated by the electric field too, but it can not take place since the RF signal is too fast. The electron trapping enhanced during compression tests induces a sort of memory effect: the reduction in the electric field may increase device robustness and influence the results of subsequent tests or steps.

If the device is stressed in back-off, electron trapping is not efficient, since the peak voltage reached is much lower; when the quiescent V_{DS} value is increased, defects formation takes place before electron trapping has gone far enough to induce a significant charge trapping and affect therefore the electric field. Consequently, as the stress goes on, I_G increases sharply.

Chapter 4

A novel investigation on dc degradation mechanisms

4.1 Dc degradation and inverse piezoelectric effect

Among the most interesting physical properties of III-Nitrides there is piezoelectricity. As we have seen, this is a fundamental element for the engineering of material stacks and the design of devices, along with the intrinsic polar nature of such materials. However, this property itself has the drawback of making III-N devices very sensitive to the inverse piezoelectric effect (Par. 2.3): a high voltage applied to the device may lead to an additional strain of the layers, with possible consequences like the formation of traps or defects, or eventually the breakdown of the materials.
In this chapter we will study the effects of high reverse gate bias on GaN HEMTs by both experimental measures and numerical simulations to identify the degradation mechanisms occurring and estimate their effects on the device AC performance, too.

4.2 Study of dc degradation by means of numerical simulations

In one of our previous works a reverse gate-drain bias stress with the source terminal floating was found to cause both a decrease of the saturated drain current and an increase of the dc-to-RF dispersion [40]. In our case, the presence of a trapping region centered at the gate edge toward the drain contact with an acceptor trap level located 0.5 eV below the conduction band in the AlGaN barrier correctly predicted the experimentally observed degradation of both dynamic and static drain current levels (Fig. 4.1 and 4.2).

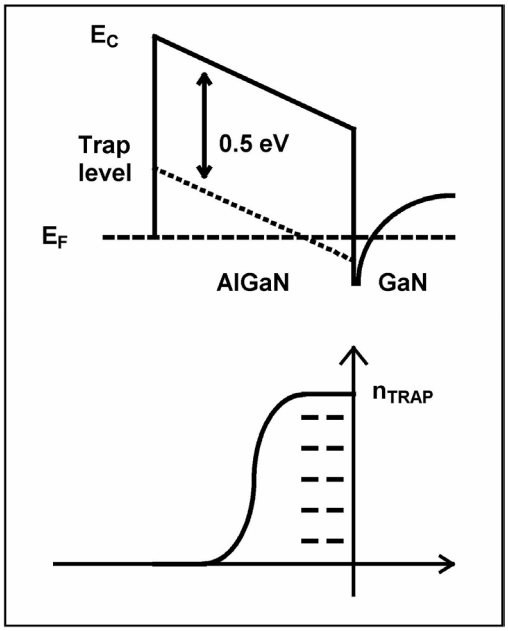

Fig. 4.1: Simplified band energy diagram of an AlGaN/GaN HEMT with an acceptor trap density located 0.5 eV below the conduction band edge (above) and concentration of the filled traps (below).

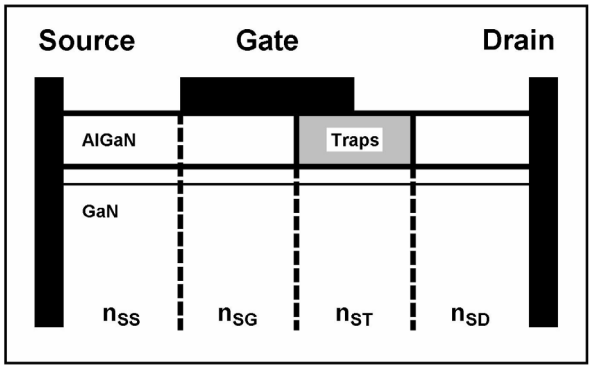

Fig. 4.2: Cross-section of a drain-degraded device structure showing in grey the defective region in the AlGaN barrier. The carrier sheet concentration n_{ST} is smaller than in the rest of the channel.

Our aim is to study the effects induced by the variation of the trapping region extension and of the trap concentration on the device dc characteristics, in particular on the saturated drain current I_{DSS}, the output conductance g_O, and the device transconductance g_m, in order to gain a better insight of the degradation mechanisms observed in [39] and [49].

4.2.1 Influence of trapping region on I-V curves

Dc stresses were carried out on 4×25μm-gate periphery devices of the ones introduced in Par. 3.1. The devices were step-stressed by applying a drain-gate voltage up to 35 V in 2.5 V/step with a step duration of 5 min, keeping the source terminal floating. At the end of each stress step, I_D–V_D and I_D–V_G characteristics were acquired in order to monitor the device degradation; the reverse gate current was monitored too. The saturated drain current I_{DSS},

evaluated at V_{GS}=0V and V_{DS}=8V, decreased by 15% at the end of the stress campaign, and the output conductance increased significantly (see Fig. 4.3). The peak of the device transconductance g_m also decreased by 21%, from 260 to 205 mS/mm (not shown). During the step stress carried out, the device experienced also an increase in the reverse gate current up to 15 mA/mm, as previously observed in [39] (not shown).

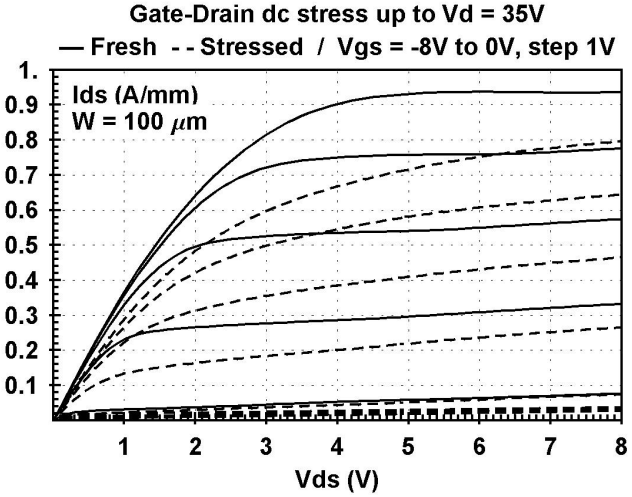

Fig. 4.3: I_D–V_D characteristics for a device stressed by applying a reverse gate-drain bias up to 35V, in step of 2.5V with a duration of 5 min. The source terminal was floating.

Two sets of structures were considered for numerical simulations. In the first one, the degraded region is centered at the gate edge and its overall extension spans in the source-drain direction from 40 to 100 nm in 20 nm/step. In the second set, the degraded region extends for 2/7 underneath the gate terminal and for the remaining 5/7 underneath the gate-drain access region, its overall extension varying from 70 to 175 nm in 35 nm/step (Fig. 4.4). The degraded region extends for the whole barrier thickness, in accordance with the results obtained in [40], with traps uniformly distributed throughout it. Total trap concentrations of 20, 50, 100, and 200 × 10^{18} cm^{-3} were considered. The I_D–V_D characteristics were simulated with the commercial DESSIS-ISE (Synopsis Inc.) simulator and a drift-diffusion model by biasing the device and solving then the currents under stationary conditions, so that all transients can be considered to have expired. As can be seen in Fig. 4.5, the introduction of a trap concentration at the edge of the gate contact leads to both a degradation of the saturated drain current I_{DSS} and to an increase in the output conductance g_O, as experimentally observed: it appears therefore as an appropriate model to describe the occurring degradation phenomena.

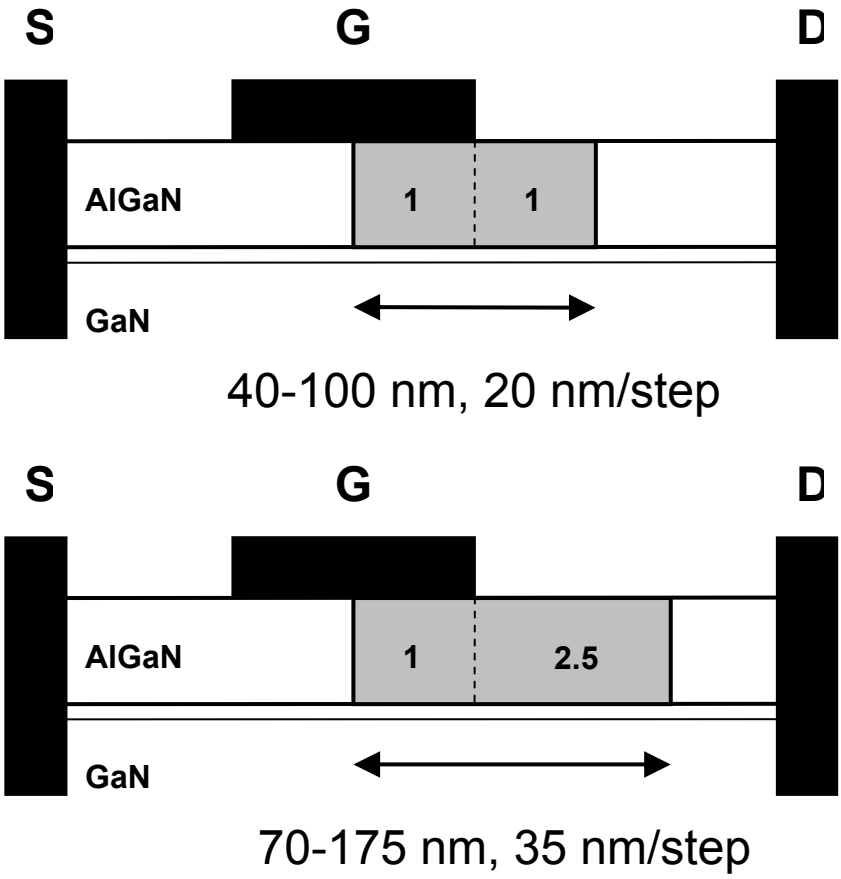

Fig. 4.4: The two sets of structures used for the numerical simulations, either with a "symmetrical" trapping region (above) or "asymmetrical" trapping region (below).

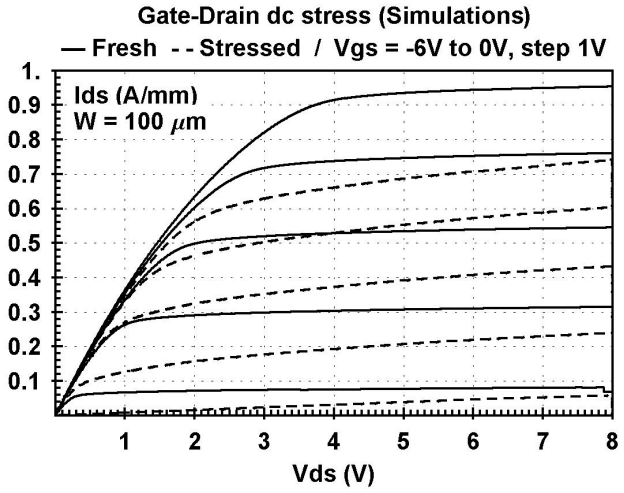

Fig. 4.5: I_D–V_D characteristics for the device structures simulated in the fresh condition and with 100 nm-long acceptor trap region in the AlGaN barrier layer, centered at the drain edge of the gate terminal. Trap concentration was 200×10^{18} cm^{-3}.

In the first set of structures (trapping region extension 40–100 nm), I_{DSS} degrades significantly at the increasing of the trap concentration, the decrease being proportional to the lateral extension of the trapping region. In the same way, the output conductance increases uniformly at the increasing of the trap concentration (Fig. 4.6). In Fig. 4.7 the same

results are shown for the second set of structures (trapping region extension 70–175 nm). The degradation of I_{DSS} is even more serious, whereas the output conductance tends to decrease for the longer degraded regions.

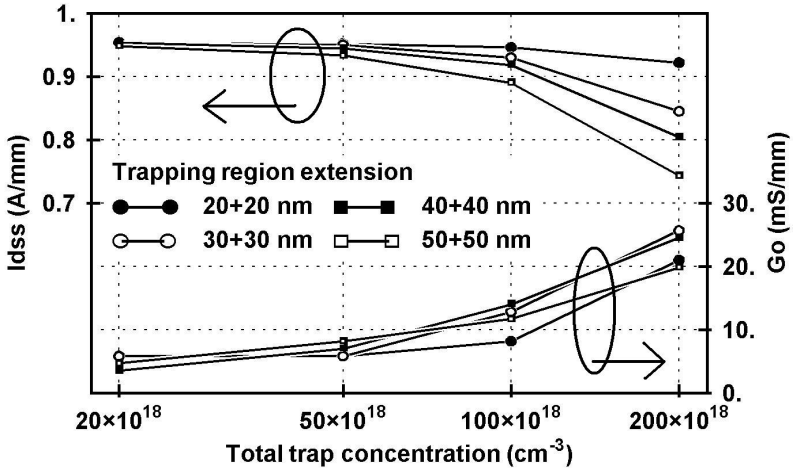

Fig. 4.6: I_{DSS} and output conductance values obtained by numerical simulations for different trap concentrations and trapping region extensions. The defective region is symmetrical.

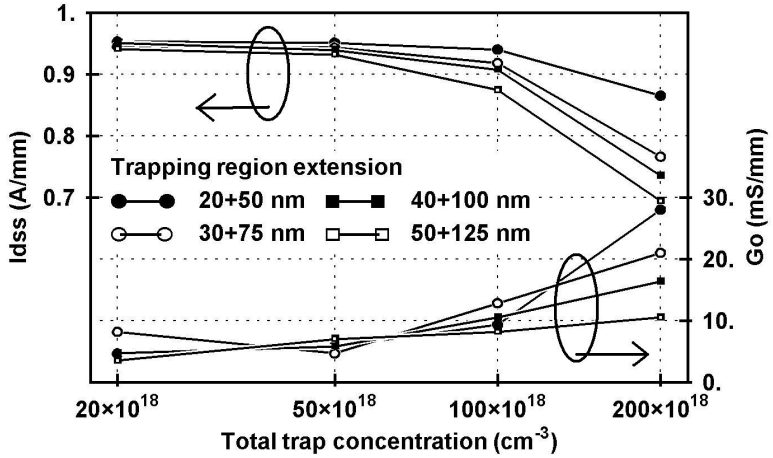

Fig. 4.7: I_{DSS} and output conductance values obtained by numerical simulations for different trap concentrations and trapping region extensions. The defective region is asymmetrical.

The reason for the decrease of I_{DSS} has been explained in [40]: The acceptor trap is located 0.5 eV from the conduction band: the trapping region extends for the whole AlGaN barrier thickness, so the traps closer to the AlGaN/GaN interface approach the Fermi level and a fraction of them are filled also in open-channel condition: a negative charge is therefore present in the barrier layer, close to the interface. Such negative charge decreases the effectiveness of the positive piezoelectric charge, inducing a reduction in the 2-DEG concentration. From the results obtained in [40], we can state that traps are filled only within very few nanometers from the interface: this statement is further confirmed by our

simulations, which show that a total trap concentration of 20–200 × 10^{18} cm^{-3} constitutes in the end an actual sheet charge density of 1.4–6.7 × 10^{12} cm^{-2}, compared to a 2-DEG sheet charge density in the channel of 12.4 × 10^{12} cm^{-2}. In Fig. 4.2 a cross-section of the device structure is reported: the value of the carrier sheet concentration in the channel under the trapping region (n_{ST}), is lower than in the other regions. On one hand, this limits the saturation current I_{DSS}, on the other hand an increase in the extension of the degraded region increases the channel resistivity anyway.

4.2.2 Output conductance and transconductance

The change in the output conductance can be explained as follows: The portion of the channel underneath the trapping region has a lower carrier concentration, acting therefore as a bottleneck for the flow of electrons. However, the same portion of the channel is subject to a high horizontal electric field at the drain end of the gate. At low V_{DS} such electric field is low, and electrons are provided with less energy, thus enhancing the bottleneck effect, leading to a significant current degradation compared to the fresh device. However, the electric field at the drain end of the gate increases with V_{DS}: if the degraded region is sufficiently short, electrons are provided with more energy and are significantly accelerated through the bottleneck, managing to pass through it, so the current increases. Our simulations show in fact that for a short degraded region the electric field peak at the drain end of the gate is much higher compared to a fresh device. Fig. 4.8 depicts the simulated electric field profiles in the channel for a fresh device and two with a trap concentration of 200 × 10^{18} cm^{-3} located in a degraded region either 70 or 175 nm long. As can be seen, if traps are present in a shorter degraded region the electric field peak is much higher and its distribution narrows: this enhances short-channel effects such as the increase in the output conductance g_O. Fig. 4.8 shows also that if the degraded region becomes longer, the electric field distribution broadens and its peak decreases, thus reducing short-channel effects and leading to a smaller output conductance: as a matter of fact, as the trapping region extension increases, the bottleneck region becomes longer too, so electrons require more energy (i.e., higher V_{DS}) to pass through it.

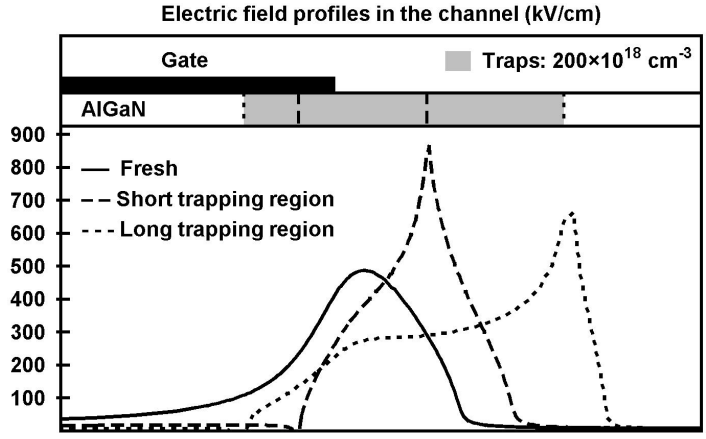

Fig. 4.8: Simulated electric field along the channel for a fresh device, and with a short or long defective region.

By simulating the I_D–V_G characteristics in the saturation region we extracted the peak device transconductance g_m for the different structures analyzed. The dependence of the transconductance on the extension of the degraded region and on the trap concentration showed a trend almost identical to the one found for the I_{DSS} current: a decrease in g_m is induced both by an increase in the trapping region extension or by an increase in the trap concentration. This happens for any of the degraded region extensions taken into account, as shown by Fig. 4.9 and 4.10.

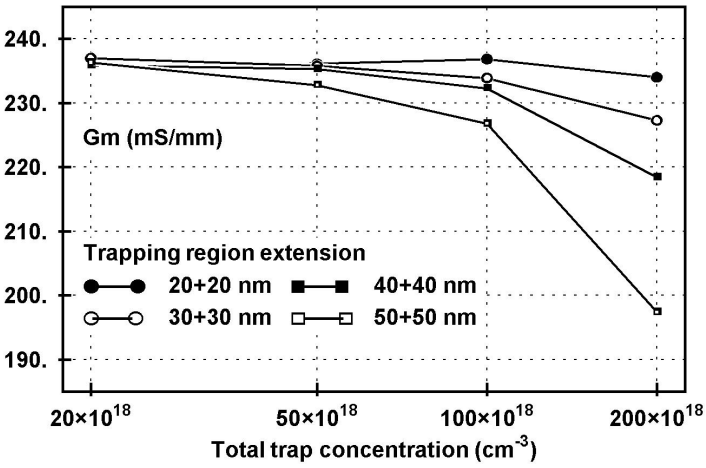

Fig. 4.9: Peak transconductance g_m values as obtained by numerical simulations. The defective region is symmetrical.

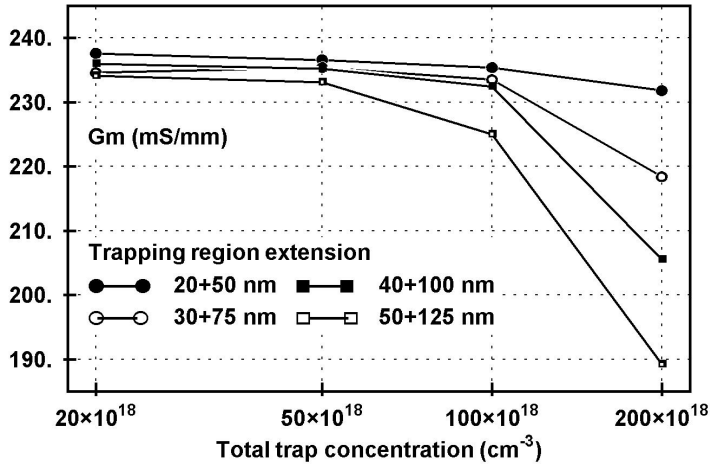

Fig. 4.10: Peak transconductance g_m values as obtained by numerical simulations. The defective region is asymmetrical.

Fig. 4.11 shows in more detail the case of the structure with a trapping region length of 140 nm: I_{DS} and g_m are reported versus V_{GS}, for a total trap concentration of 20×10^{18} cm^{-3} (almost identical to the fresh case) and 200×10^{18} cm^{-3} (V_{DS}=8V). Both I_{DS} and g_m decrease at the increasing of the trap concentration.

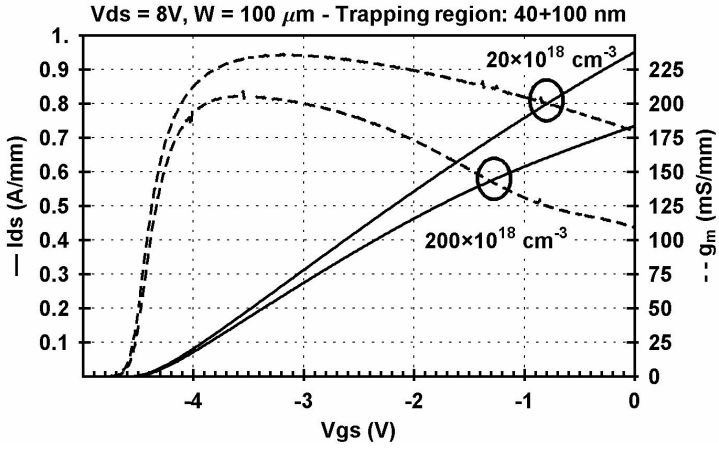

Fig. 4.11: I_{DS}–V_{GS} characteristics and g_m for two different trap concentration values (V_{DS}=8V).

4.2.3 Correlation with AC performance: scattering parameters

Additional simulations were carried out to correlate gm to the device AC performance. The scattering parameters were extracted in a common source configuration, and were then used to calculate the short circuit current gain h_{21}: the cutoff frequency f_T of the transistor was then extracted. This analysis was carried out for different trapping region lengths and different trap concentrations, both in the case of V_{GS}=0V and V_{GS}=–3V. It is reasonable to

expect the trends of g_m and f_T to match, according to a simple relation from the approximated AC model of an FET:

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{4.1}$$

From the results shown in Figures 4.12 and 4.13, we can state that this type of analysis appears suitable to study the AC performance of such devices. In fact, f_T at V_{GS}=0V is lower than at V_{GS}=–3V, reproducing the difference between the transconductance at the two bias points (approximately 15 to 20%). On the other hand, the dependence of f_T on the trapping region length and on the trap concentration follows exactly the trend of g_m.

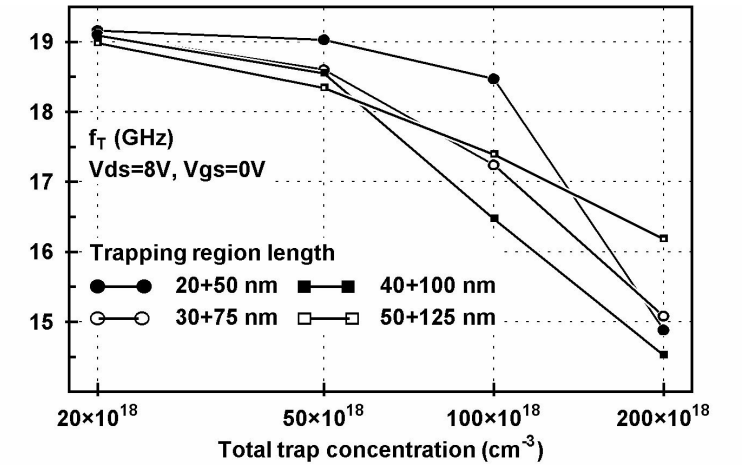

Fig. 4.12: Cutoff frequency f_T in open-channel condition for different structure variants.

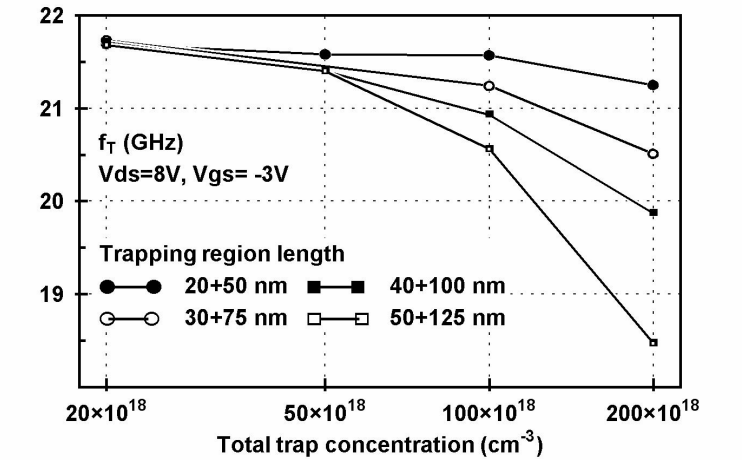

Fig. 4.13: Cutoff frequency f_T at V_{GS}=–3V (close to the g_m peak) for different structure variants.

4.3 Gate-source and gate-drain reverse bias stress and stress following

The analyses presented so far have pointed out the origin and the effects of the device degradation when the gate-drain junction is under dc reverse bias stress. However, no details were given about the dual case of a gate-source reverse bias stress: even though the physical effects on the device are the same, the device behavior may be substantially different, as we will see. In this paragraph, we will report on the difference between the consequences of gate-drain and gate-source reverse bias stress on the device, and will model the actual degraded region by means of numerical simulations in both cases.

4.3.1 Difference between gate-source and gate-drain stress and basic modeling

Stress conditions were identical as for the devices in the previous study: fresh devices were step-stressed by applying a reverse gate-drain voltage up to 35 V in 2.5 V/step with a step duration of 5 min with the source terminal floating. Another set of devices was stressed according to the same schedule on the gate-source side, keeping the drain terminal floating. At the end of each step, I_D–V_D and I_D–V_G characteristics were acquired and reverse gate current measurements were performed, in order to monitor the device degradation.
Both sets of devices showed an initial value of I_{DSS} of about 0.9 to 1 A/mm (measured at V_{GS} = 0 V and V_{DS} = 8 V), $V_{knee} \approx 3.5$ V, and negligible output conductance. In both cases, at the end of the stress campaign the saturated drain current decreased significantly (–15% for the drain-stressed and –18% for the source-stressed). Additional stress steps carried out at 35 V for both cases have shown that if the stress condition is maintained, the decrease in the saturated drain current tends to slow down, suggesting therefore a saturation of the I_{DSS}. The reverse gate current was evaluated on the stressed side of the device at V_G = –8 V with the stressed side terminal at 0 V and the other terminal floating: at the end of the stress campaign it had eventually increased up to 16 mA/mm (in Fig. 4.14 the trends of I_{DSS} and I_G are reported in detail). The peak transconductance has also degraded almost equally, from 260 to 190 mS/mm for the source-stressed case, and from 260 to 200 mS/mm for the drain-stressed case. In the latter though, a significant increase in the output conductance was observed compared to the former (see I_D–V_D characteristics reported in Fig. 4.15 and 4.16).

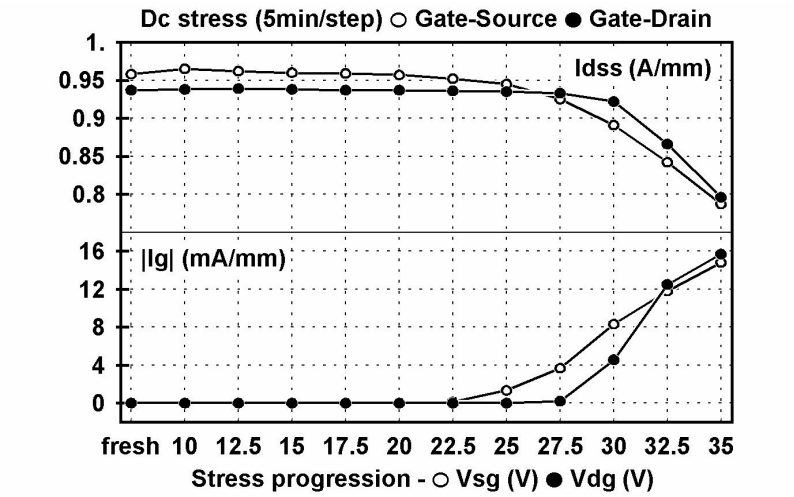

Fig. 4.14: Progression for a device stressed only on the gate-source side (drain floating, empty circles) or gate-drain side (source floating, filled circles).

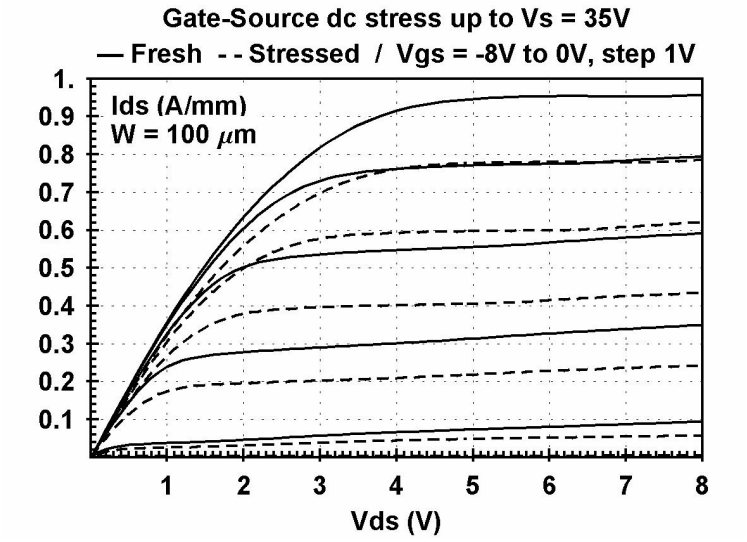

Fig. 4.15: I_D-V_D characteristics for a fresh device and after the last source-only stress step at V_{SG} = 35V.

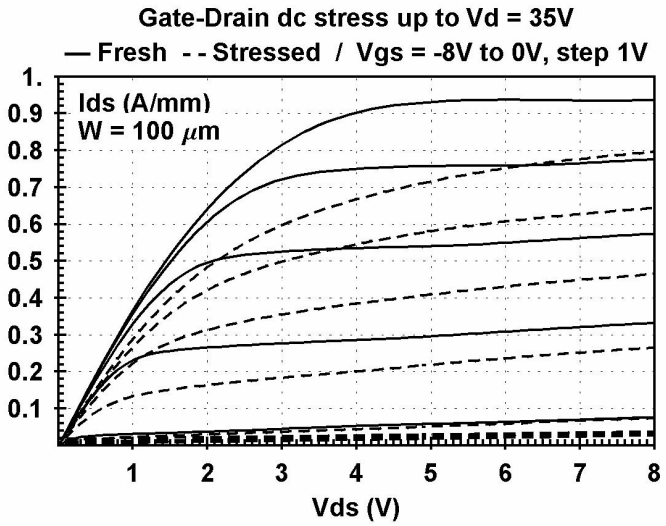

Fig. 4.16: I_D-V_D characteristics for a fresh device and after the last drain-only stress step at V_{DG} = 35 V.

The difference in the output conductance can be explained as follows. The portion of the channel under the trapping region has a lower carrier concentration, representing therefore a bottleneck for the flow of electrons. Let us consider the case of a degraded region located at the drain end of the gate first. At low V_{DS}, with a low electric field, electrons are provided with little energy, thus enhancing the bottleneck effect and leading to a significant decrease in the drain current compared to the fresh device. However, simulations carried out on a drain-degraded structure biased in the saturation region at V_{GS} = 0 V yielded a higher electric field peak at the trapping region edge compared to the fresh structure. This can enhance short-channel effects such as the increase in the output conductance g_O: since the electric field at the drain end of the gate increases with V_{DS}, as the bias increases electrons are provided with more energy and are significantly accelerated through the bottleneck, managing to pass through it, so the current increases: this can explain the increase in the output conductance, in accordance with the literature.

On the other hand, if the trapping region is located under the source end of the gate, the electric field to which the channel bottleneck is subject is not high enough to provide electrons with an amount of energy sufficient to let them fully overcome its degrading effect: in this case, any increase in V_{DS} beyond V_{knee} does not yield any significant further increase in the drain current, which soon saturates.

The role of traps can be furthermore corroborated by recovery measurements carried out 2 hours after the end of the stress campaign: devices subjected to a 40-min 35 V step showed a recovery in the drain current of about 3% compared to the last stress step.

The explanation of the occurring phenomena can also be inferred just by considering a simple model of the device after the generation of defects subsequent to the stress. A short part of the channel gets depleted by the presence of the traps, therefore the device can be modeled as two devices in series, one with a longer channel and a higher 2-DEG concentration, and the other with a short channel and a lower n_S. In Fig. 4.17 the model is presented for the drain-stressed case: the "drain" transistor has a lower current and a lower channel length, which leads to a high output conductance, whereas the "source" transistor has a high current and no output conductance. The voltage drop is mainly across the drain transistor, which acts ad a bottleneck and sets the ultimate shape of the global I-V characteristic.

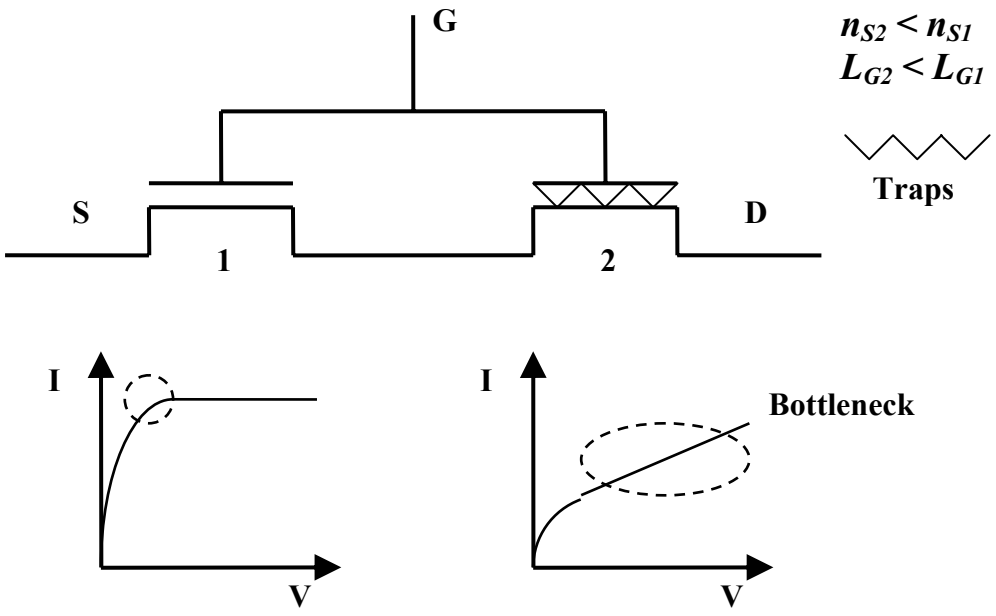

Fig. 4.17: Model for drain-stressed devices.

Similarly, in Fig. 4.18 the same model is proposed for the source-stressed case: this time the source transistor has a lower current and a lower channel length, which leads to a high output conductance, whereas the drain transistor has a high current and no output conductance. The voltage drop is again mainly across the drain transistor, so the source transistor sets the ultimate shape of the global I-V characteristic, with a constant lower current.

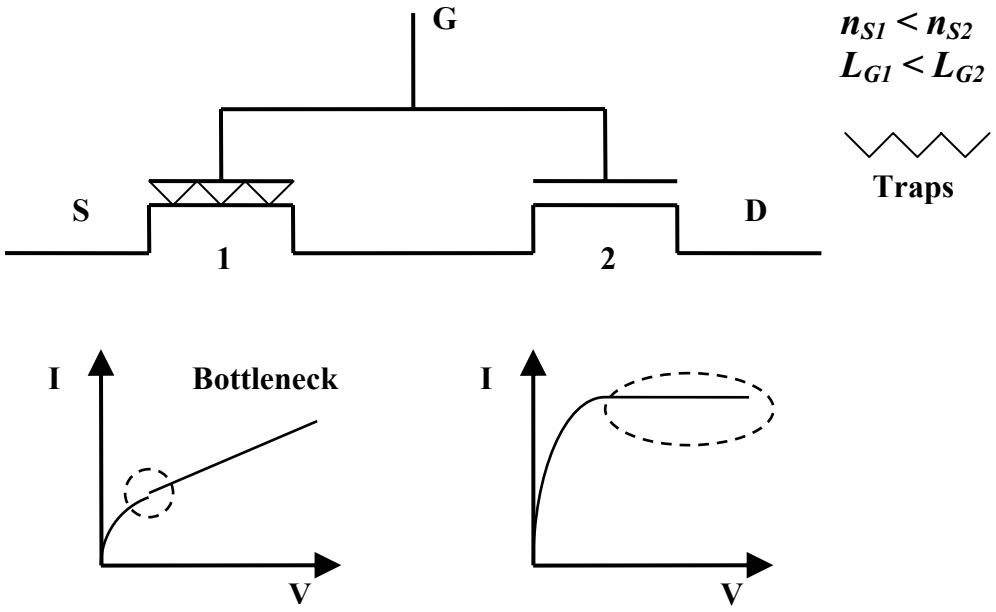

Fig. 4.18: Model for source-stressed devices.

4.3.2 Stress following

In order to investigate the physical mechanism causing the observed degradation phenomena, we carried out 2-D numerical simulations using the commercial DESSIS-ISE (Synopsis Inc.) simulator. A trapping region was placed under the gate terminal edge, either on the drain or source side, similar to what we did in Par. 4.2. Again, acceptor-like traps were located at 0.5 eV below the conduction band edge. The two parameters we changed in order to fit the experimental drain current degradation were the lateral extension of said region and the trap concentration.

In the first place, the source-stressed structure was simulated. A good fitting was obtained for the fresh case (Fig. 4.19). Then, a trapping region was introduced at the source end of the gate to try and fit the device characteristics as acquired after the stress steps at 32.5 V and 35 V. As can be seen from Fig. 4.20, a good fitting was obtained after V_{SG} = 32.5 V by introducing a trapping region with a length of 580 nm (80 nm under the gate, 500 nm under the source access region) and an acceptor trap concentration of 60×10^{18} cm^{-3}. The significant length of such degraded region (about 16% of the source–drain spacing) was necessary to fit the increase in the on-resistance from 2.8 to 3 Ωmm. Then, since the on-resistance stayed almost unchanged after the following step at V_{SG} = 35 V, only the trap concentration was increased. As shown in Fig. 4.21, a value of 93×10^{18} cm^{-3} was sufficient

to follow the degradation and obtain a good fitting also after V_{SG} = 35 V, always with an almost negligible output conductance, as experimentally observed.

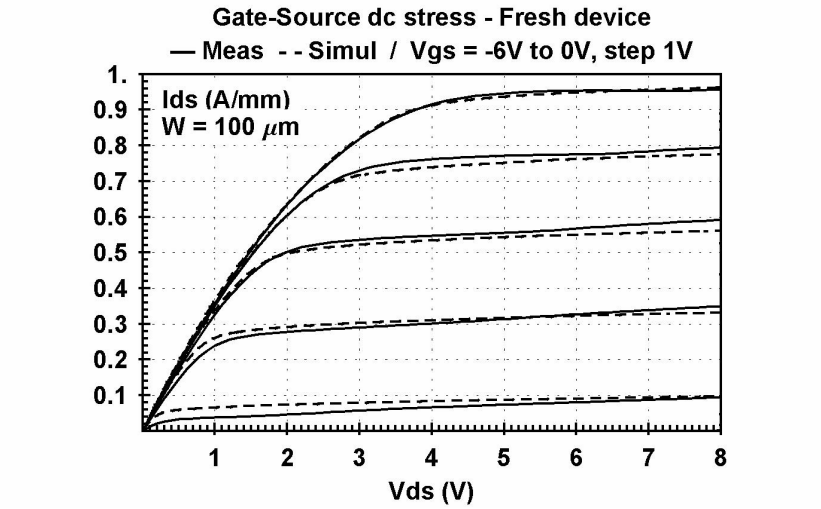

Fig. 4.19: Experimental and simulated I_D-V_D characteristics for the fresh source-stressed structure

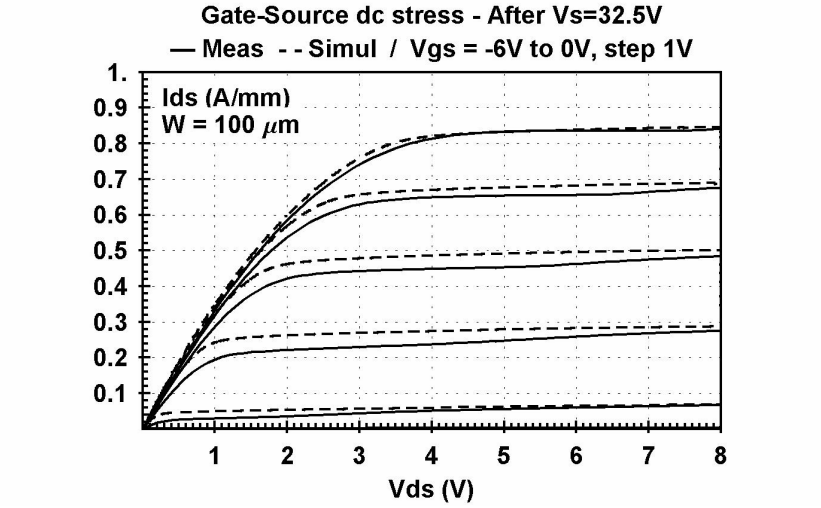

Fig. 4.20: Experimental and simulated I_D-V_D characteristics for the source-stressed structure after the stress step at V_{SG} = 32.5 V. Simulated trap concentration is 60×10^{18} cm^{-3}

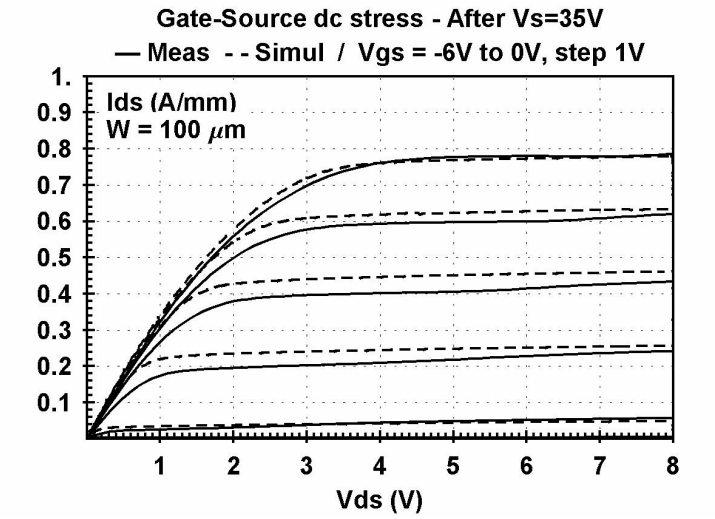

Fig. 4.21: Experimental and simulated I_D-V_D characteristics for the source-stressed structure after the last stress step at V_{SG} = 35 V. Simulated trap concentration is 93×10^{18} cm^{-3}

Since the drain-stressed devices were subjected to the same stress schedule and the final degradation of the I_{DSS} was almost the same, we simulated a drain-stressed structure with a trapping region of the same length as before (80 nm under the gate, 500 nm under the drain access region). Again, simulations fitted very well for the fresh structure (Fig. 4.22). Degraded characteristics after V_{DG} = 32.5 V fitted well by introducing a trap concentration of 88×10^{18} cm^{-3} (see Fig. 4.23): both the dc drain current degradation and the increase in the output conductance are reproduced by the simulations. As regards fitting after V_{DG} = 35 V though, the decrease of the I_{DSS} was properly matched by introducing a trap concentration of 130×10^{18} cm^{-3}, but the worsening in the on-resistance and in the output conductance were only qualitatively fitted (Fig. 4.24).

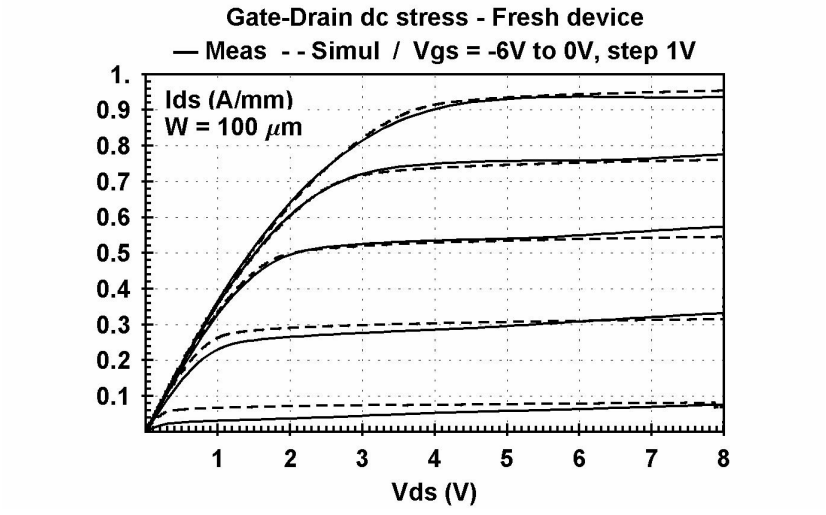

Fig. 4.22: Experimental and simulated I_D-V_D characteristics for the fresh drain-stressed structure

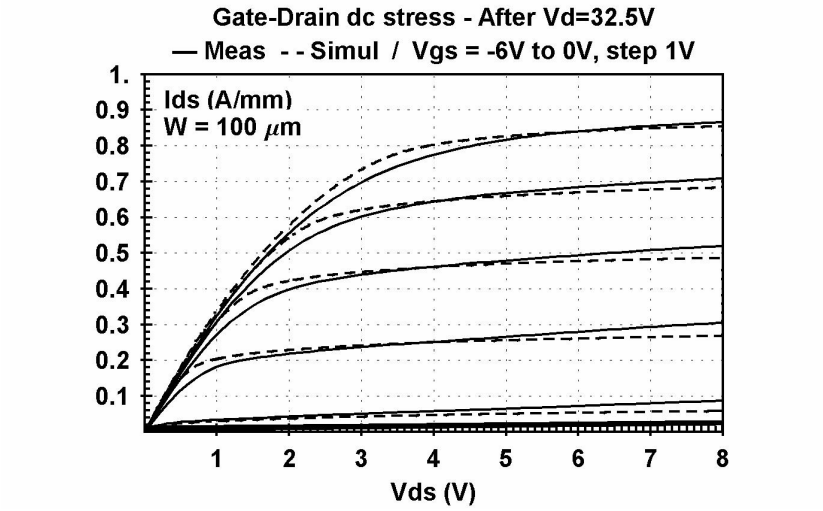

Fig. 4.23: Experimental and simulated I_D-V_D characteristics for the drain-stressed structure after the stress step at V_{DG} = 32.5 V. Simulated trap concentration is 88×10^{18} cm^{-3}.

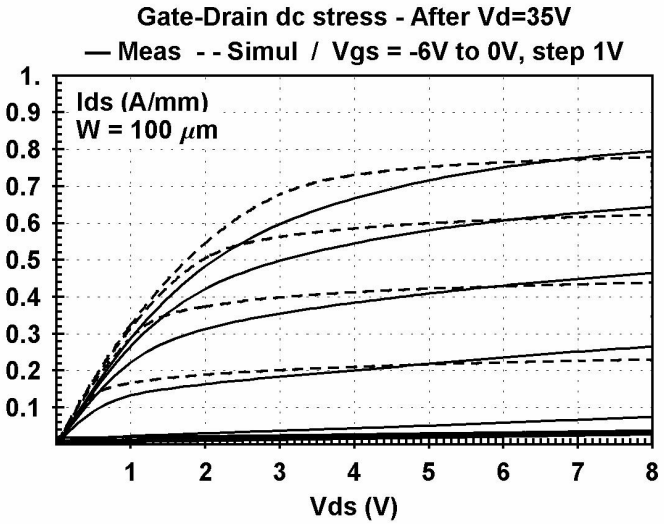

Fig. 4.24: Experimental and simulated I_D-V_D characteristics for the drain-stressed structure after the last stress step at V_{DG} = 35 V. Simulated trap concentration is 130×10^{18} cm^{-3}.

The higher difficulty in fitting the characteristics of the drain-stressed devices is probably due to the different pace of degradation. Device parameters were monitored during the stress: in all cases it was possible to identify a point in time during the dc stress when the reverse gate current would suddenly become noisy and start increasing incessantly, soon giving rise to a visible device degradation. This event occurred at about 20 V for the source-stressed devices, with a significant degradation starting being visible at about 25 to 27.5 V. It occurred at higher voltage for the drain-stressed devices (22.5 to 25 V), with a significant degradation starting being visible at about 30 to 32.5 V. This could be due to the higher gate–drain spacing having delayed the onset of breakdown, which therefore occurred at

higher voltage: hence, it appears not unlikely that some mechanism has been triggered in the gate-drain stressed devices that has emphasized the drain current degradation to a point where the only account for traps in the AlGaN as we supposed here could be not sufficient to explain the device degradation, even though key aspects like the decrease of I_{DSS} and the increase of g_O are indeed reproduced, as shown in a more detailed comparison in Fig. 4.25.

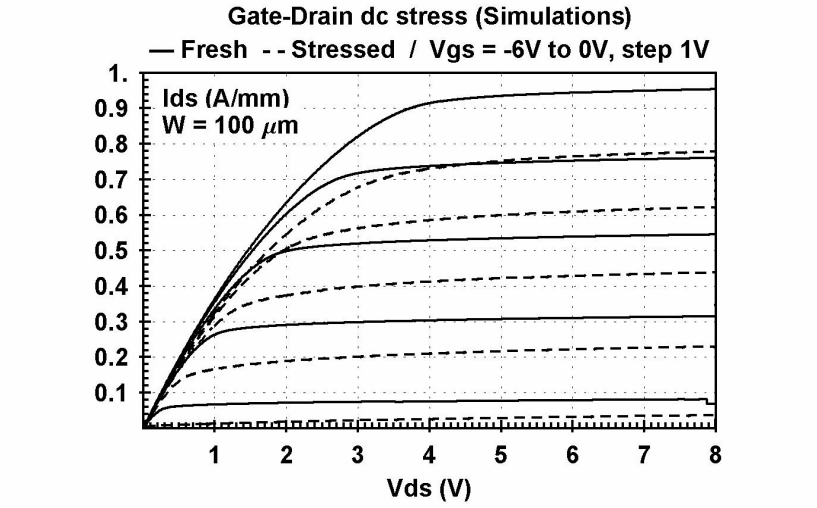

Fig. 4.25: Simulated I_D-V_D characteristics for the drain-stressed structure both fresh and after the last stress step at V_{DG} = 35 V (trap concentration is 130×10^{18} cm^{-3}).

Chapter 5

Innovative applications of GaN: structures for hole conduction

On of the many challenges that can be outlined for gallium nitride, and the whole III-N system in general, is to break the barrier of the unipolar conduction. III-Nitrides have so far demonstrated excellent performances in a wide variety of applications, though by exploiting electron conduction only. The possibility to extend the acquired knowledge of GaN electronics to p-type conduction III-Nitrides may eventually lead in the future to a combination of both n-type and p-type GaN-based transistors, in a likely C-HEMT technology that would push the performances of logic circuits even further as far as operation temperature and switching frequency are concerned.
In this chapter, the known issues and limitations of III-Nitrides for hole conductions will be reported, followed by the road-map that eventually led to the fabrication of devices that showed signs of hole accumulation.

5.1 Known issues of III-Nitrides for hole conduction

Observation of 2-DHG or p-type conduction in GaN is hard to achieve, due to limitations that have been identified and faced throughout the years. Here are the most significant.

5.1.1 Lack of shallow acceptors

A serious obstacle to hole accumulation in GaN and AlGaN is the lack of a sufficiently shallow acceptor species in order to obtain a high concentration of holes. Silicon is an excellent n-dopant, for it is truly a shallow donor and sits just 5 meV below the GaN conduction band. It happens to be a very effective donor for AlGaN too, with activation energies ranging from 17 to 100 meV [60]. However, it is not so straightforward to find an

equally effective p-dopant for GaN: the most known ones are berillium (250 meV), carbon (230 meV) and magnesium (220 meV) [61].

Material	*Doping*	*Element*	*Energy*
GaN	n	Si	E_C – 0.005 eV
GaN	p	Be	E_V + 0.25 eV
GaN	p	C	E_V + 0.23 eV
GaN	**p**	**Mg**	**E_V + 0.22 eV**
$Al_{0.18}Ga_{0.72}N$	n	Si	E_C – 0.054 eV
$Al_{0.6}Ga_{0.4}N$	n	Si	E_C – 0.090 eV
AlGaN	**p**	**Mg**	**E_V + 0.4 eV**

Table 5.1: Doping species for GaN and AlGaN

As can be seen, there is no easy choice for p-doping in III-Nitrides. However, the best chances seem to be more likely to achieve by the use of magnesium at high concentration in GaN, rather than AlGaN or other materials.

5.1.2 Ohmic contacts

The techniques developed to obtain good ohmic contacts on n-type GaN are by now at an advanced stage so that resistivity values of less than 1Ω·mm are not prohibitive. Among the most reported ohmic stacks there are Ti/Al/Pt/Au [62] (with Pt acting as a diffusion barrier for Au penetration), Ti/Al/Ti/Au [63] and Ti/Al/Ni/Au [64]. All the contacts are meant to be alloyed at temperatures of 830-850°C.

An increasing number of studies of p-type ohmic contacts on GaN has been reported, for the role they play in optoelectronic devices. However, for the purpose of this dissertation we shall focus only on their electric properties. The main electronic application of p-type contacts on GaN is the base of npn-GaN HBTs. However, it should be noted that, due to the properties of GaN and to the difficulty in obtaining a high hole concentration, contact resistance values are typically two orders of magnitude higher than that for n-type contacts; moreover, as-deposited metal stacks are usually rectifying. In some cases, even after annealing, contacts do not show a purely ohmic behaviour anyway (Ni/Pt/Au stack [65]).

Several studies were reported on the properties of the Ni/Au metal stack on p-GaN [66-68], which appears to be an interesting candidate for making ohmic contacts on Mg-doped GaN.

5.1.3 Polarity inversion

In [69], V. Ramachandran et al. found that exposing the surface of Wurtzite 0001-GaN to 1 monolayer of Mg or more during growth would have a surfactant effects and, more importantly, would cause the polarity of the material to switch from Ga-polar to N-polar (Fig. 5.1)

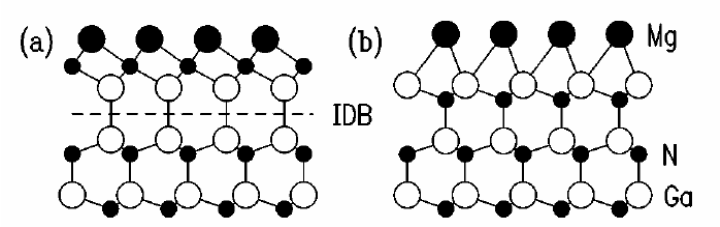

Fig. 5.1: (a) Model of an inversion domain boundary induced by Mg. (b) Non-inverted structure [69]

Similar results were obtained by L. T. Romano et al. in [70], were instabilities with respect to polarity inversion were observed. The issue of polarity inversion affects of course not only GaN, but other III-Nitrides. AlGaN in particular, was found by H. K. Cho and others to be affected by the doping with Mg by means of dislocation density, inversion domain boundaries, and shape of defects [71]. Such issues were found to be dependent both on the Mg concentration and on the Al content [72]. Countermeasures can be taken to avoid polarity inversion: D. S. Green et al. have reported that the presence of a Ga wetting layer would inhibit the nucleation of N-face GaN, even though it required time to develop [73]. In the end, if a Ga-polar structure is needed, the risk of polarity inversion shall be taken into account. However, the studies reporting polarity inversion of p-GaN have remarked that no second inversion from N-face to Ga-face was ever observed, nor to our knowledge N-face GaN has ever been reported to have inverted to Ga-face during growth because of exposure to magnesium. Therefore, if a Ga-face structure is needed, attention must be paid in order to avoid polarity inversion; alternatively, the use of N-face structures shall can be considered in order to avoid such risk.

5.2 2-dimensional hole gas (2-DHG): a recent challenge

Several works have reported theorethical calculations and numerical simulations predicting the feasibility of a 2-DHG in III-Nitrides. In 2000, M. S. Shur et al. reported on the possibility to obtain a 2-DHG in an AlGaN/GaN structure by exploiting the piezoelectric and pyroelectric charges, up to a concentration higher than 10^{13} cm^{-2} [74-75]. Whereas the results in these studies are addressed towards a potential reduction of the base spreading resistance in AlGaN/GaN-based Heterostructure Bipolar Transistors, the potentialities of an undoped p-channel structure were still investigated in the following years, for the most known element acting as a p-dopant for III-Nitrides, magnesium, has a high activation energy not only in GaN and AlGaN, but also in InGaN [76]. However, experimental results have rarely brought confirm to such theories. In 2004, T. Zimmermann et al. proposed a GaN/InGaN/GaN structure with a theoretical 2-DHG concentration of 7×10^{11} cm^{-2} calculated by numerical simulations [77]. Measures at low temperature (in order to exclude that the channel was related to acceptor doping) suggested the presence of a 2-DHG with a sheet charge density of 10^{11} cm^{-2}.

An interesting contribution to the field arose from the study of N-face GaN/AlGaN/GaN FETs by S. Rajan [18]. The purpose of the study was to investigate the properties and potentialities of N-face GaN for n-channel devices. However, it was found that devices were affected by dispersion, and that according to the Schrödinger-Poisson simulator, there was a high population of holes at the lower AlGaN/GaN interface (Fig. 5.2).

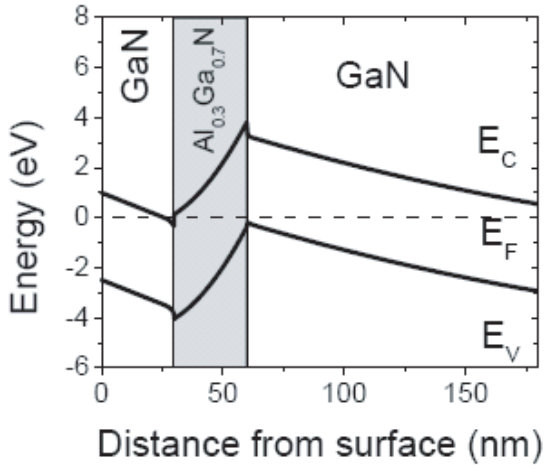

Fig. 5.2: Simulated band diagram of an N-face GaN/AlGaN/GaN HEMT [18]

The nature of this positive charge was investigated by capacitance DLTS measurements by A. Chini and Y. Fu [78], which revealed the presence of a donor-like hole trap state at the GaN/AlGaN interface with negative polarization charge that would behave electrostatically similarly to holes in steady state conditions but causes current collapse and gate lag under pulsed excitation. The concept of such a structure was then exploited by A. Nakajima et al. in [79], where a 2-DHG with a sheet concentration of 10^{13} cm^{-2} was demonstrated in Ga-polar pn junction diodes. In this case the AlGaN was undoped, being the device not intended for enhancing electron conduction (Fig. 5.3).

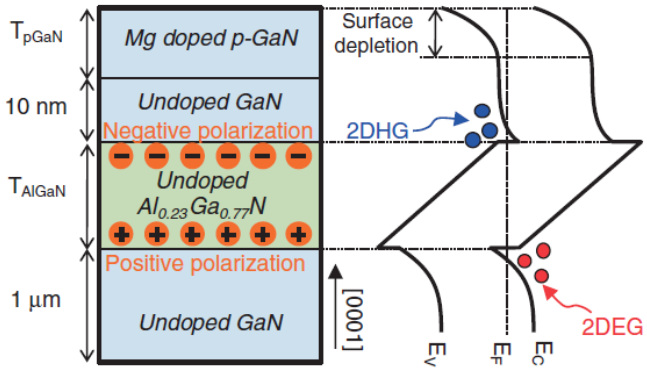

Fig. 5.3: Layer structure and band diagram of a Ga-face GaN/AlGaN/GaN diode [79]

However, in order to apply such findings to a more HEMT-oriented layer structure and process and achieve a p-type channel, some changes to a structure like the one presented in [79] would be necessary. Due to the necessity to perform an annealing to the ohmic contacts, one first requirement would be to eliminate the 2-DEG at the lower AlGaN/GaN interface. This could be achieved by the use of magnesium as p-dopant in the AlGaN layer. In Fig. 5.4 a band structure for a p-GaN/GaN/p-$Al_{0.3}Ga_{0.7}N$/GaN is reported. P-doping concentration is 5×10^{19} cm^{-3}. It was obtained by numerical simulation using BandEng, a one-dimensional Schrödinger-Poisson solver developed by Michael Grundmann [80].

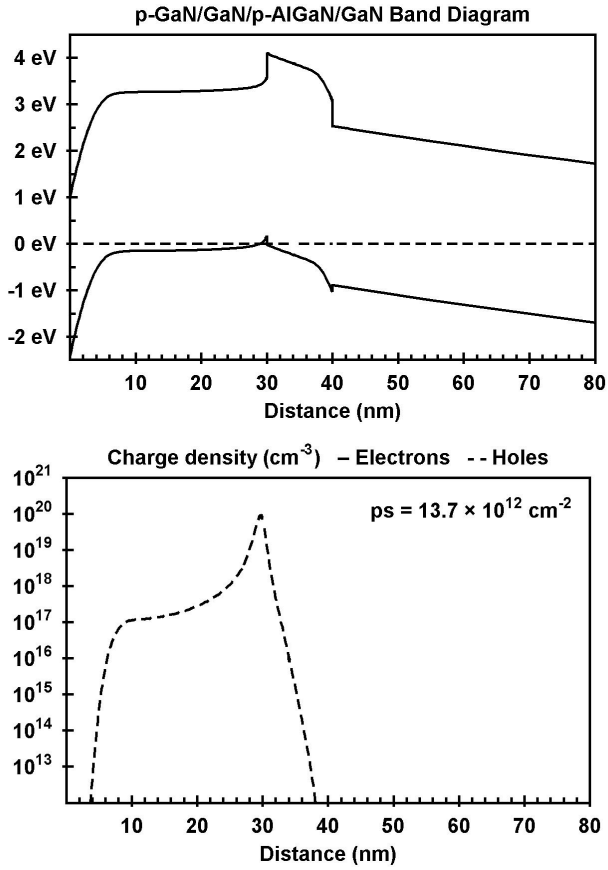

Fig. 5.4: Band diagram and charge distribution of a Ga-face p-GaN/GaN/p-AlGaN/GaN HEMT.

However, a big challenge for such a structure comes from the risk of polarity inversion, being the doping considerably high and present both in GaN and AlGaN. Therefore, according to our experience, it was eventually decided to concentrate on a novel challenge: to develop a new kind of structure which, to the best of our knowledge, has never been investigated in the perspective of the formation of a 2-DHG.

5.3 N-polar GaN/InGaN/GaN p-channel devices

In order to avoid the risk of polarity inversion, a new structure was designed and studied. It is a N-polar GaN/InGaN/GaN stack, in which p-doping is exploited to avoid the formation of a parasitic 2-DEG and to help creating a better ohmic contact.

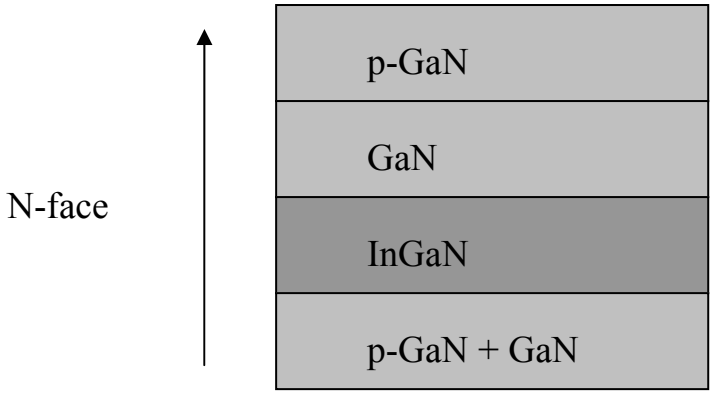

Fig. 5.5: Layer structure of the N-face GaN/InGaN/GaN HEMT

The design criteria in order to have a hole gas at the upper GaN/InGaN interface were mainly focused on three variables to play with, given all other parameters are equal:

- The thickness of the upper GaN layer
- The thickness of the InGaN layer
- The In molefraction in the InGaN

i) <u>Increasing the thickness of the upper GaN layer</u>

As can be seen in Fig. 5.6, given that the metal-semiconductor barrier height Φb is constant and so is the net polarization charge σ_P at the interface, increasing the upper GaN layer thickness leads to an increase in the hole sheet concentration p_S, for ΔF decreases. However, this eventually leads to no further increase in the hole gas concentration, as the band bending slows down due to the constraint imposed by Φb, therefore we can state that an optimum value can be found for the GaN thickness. The p-type doping in GaN is omitted for simplicity (Fig. 5.6).

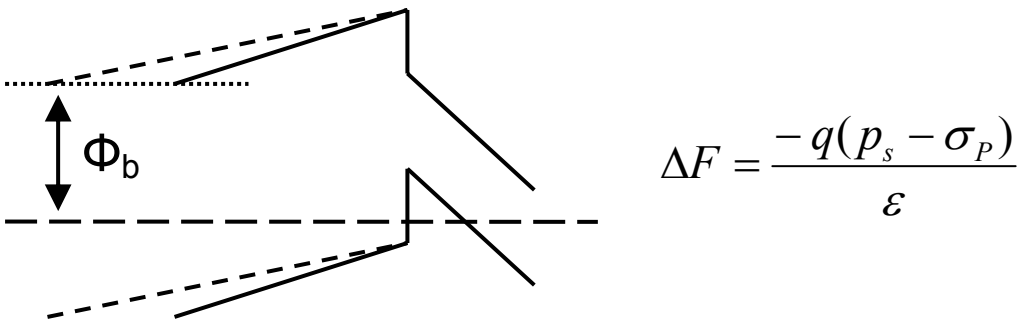

Fig. 5.6: Effect of the increasing of the upper GaN layer on the hole sheet concentration.

ii) Increasing the thickness of the InGaN layer

In Fig. 5.7 the lower interface between InGaN and GaN is reported. A uniform unintentionally doped GaN layer is assumed. Given the In molefraction, as the InGaN thickness is increased, the valence band is pushed above the Fermi level, and holes shall begin to accumulate. Again, p-type doping is omitted in the figure for simplicity.

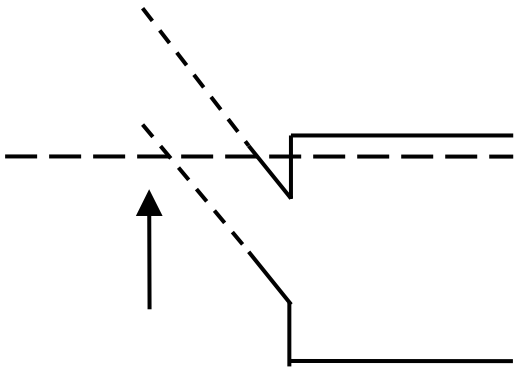

Fig. 5.7: Increasing of the InGaN layer thickness shall eventually lead to hole accumulation.

iii) Increasing the In molefraction in the InGaN layer

Given the InGaN layer thickness, a higher fraction of indium can help obtaining a hole gas, as shown qualitatively in Fig. 5.8 (p-type doping is again omitted for simplicity).

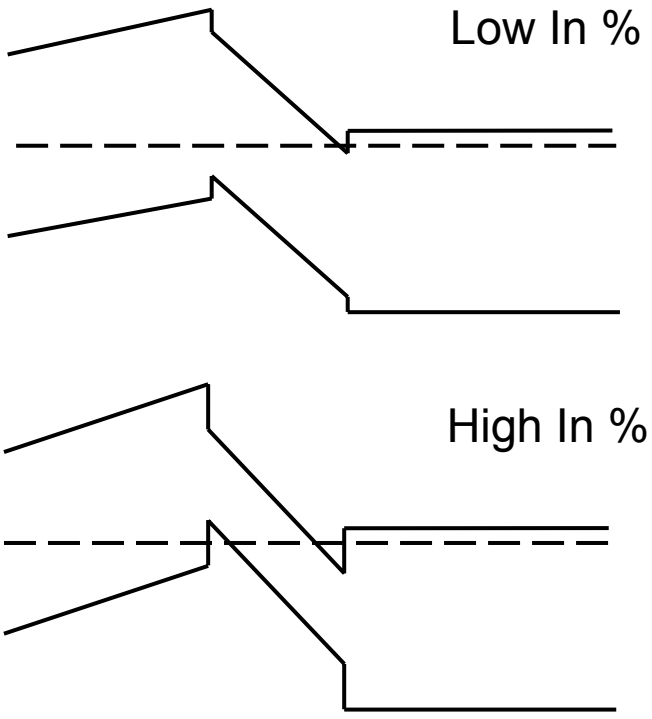

Fig. 5.8: Increasing the InGaN In molefraction shall eventually lead to hole accumulation.

Of course, factors ii) and iii) are not independent and a trade-off must be find in order to avoid the risk of relaxation of the material. The structure eventually designed is reported in Fig. 5.9. In Tab. 5.2 the simulated tolerance values for In molefraction and InGaN thickness are reported too.

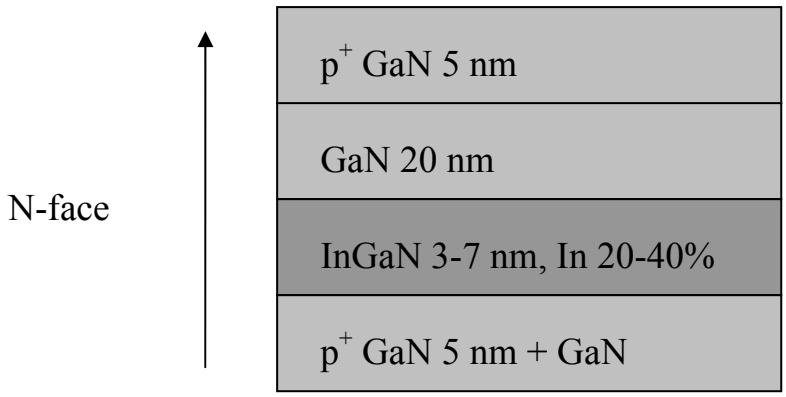

Fig. 5.9: Layer structure of the grown N-face GaN/InGaN/GaN HEMT.

InGaN	In 20%	In 25%	In 30%	In 35%	In 40%
3 nm	Good	Good	Good	Good	Good
4 nm	Good	Good	Good	Good	Good
5 nm	Good	Good	Good	Good	**Fair**
6 nm	Good	Good	Good	**Fair**	**Bad**
7 nm	Good	Good	**Fair**	**Bad**	**Bad**

Table 5.2: Qualitative tolerance for the InGaN layer in order to have a hole gas

As can be seen, the allowed wide tolerance makes this structure attractive, for even consistent deviation from the assigned values during the growth may not result in a failure.

The designed structure was grown by Plasma Assisted Molecular Beam Epitaxy (PAMBE) on C-face SiC. The epilayer eventually consisted of an undoped 310-nm GaN buffer, followed by a 5-nm p^+ GaN layer (in order to avoid the formation of a 2-DEG at the interface), a 6-nm $In_{0.2}Ga_{0.8}N$ layer, then a 12.5-nm undoped GaN layer followed by a 5-nm p^+ GaN cap in order to favor the ohmic nature of the contacts. In Fig. 5.10 a simulated band diagram and charge concentration for the actual grown structure are reported.

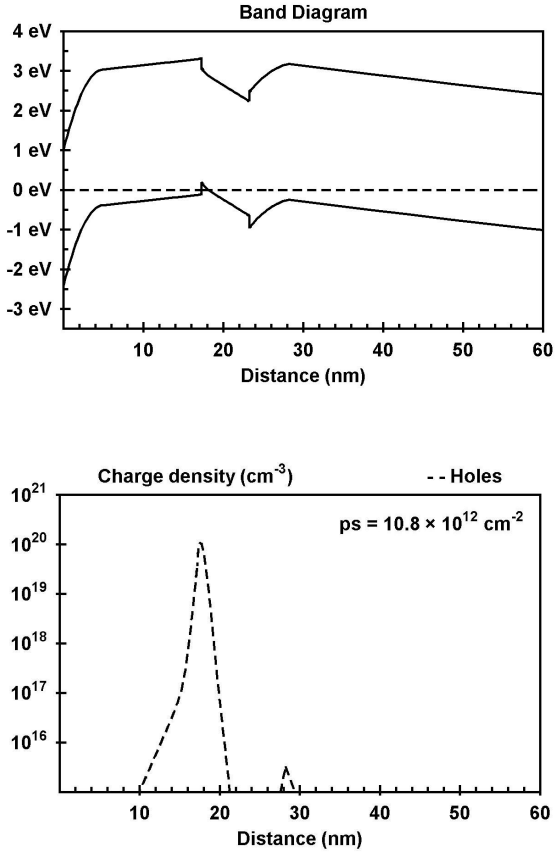

Fig. 5.10: Simulated band diagram and charge concentration for the grown structure

The ohmic metal deposition took place through a metal-first process. Ni/Au (25/100 nm) contacts were first deposited by e-beam evaporation, and then defined by optical contact lithography and metal wet etching. The reasons for avoiding lift-off were on one hand a better definition of the contacts on p-type materials, and on the other hand to protect the surface of the epilayer: being the structure N-face, it would have been etched by the MF-219 developer. Device mesa isolation was formed by Cl-based ICP/RIE etching: the etching depth was about 250 nm. Source-drain spacing varied from 2 to 4.5 μm.

The buffer leakage appeared to be acceptably low, ranging between 1–2 μA/mm at 50V. However, the testing of the sample brought less results than expected, being affected mainly by the non-ohmic characteristic of the contacts. Not even subsequent annealing sessions up to 500°C could improve such behavior (Fig. 5.11).

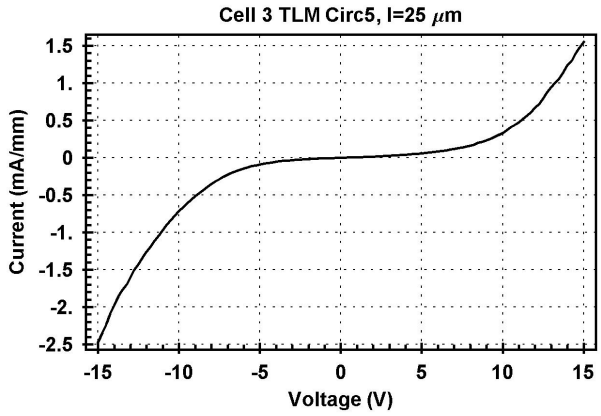

Fig. 5.11: I-V characteristic of a couple of TLM contacts (spacing 25 μm)

This issue of course affected most of the usual procedures to characterize the sample, like the Hall measurements to find the sheet carrier and the mobility, and the TLM measurements to calculate the sheet resistance – even though prior to the mesa isolation a sheet resistance of approximately 1.67 kΩ/sq was extracted. Therefore, in order to verify the presence of a hole gas, we carried out the gate lithography process step, in order to etch a recess in the gate zone rather than evaporating gate metal. To do this, since N-face GaN etches in developer, germanium was used as a sacrificial layer to prevent the etching of the epitaxial layer during development. Ge was then etched away by H_2O_2, which does not etch GaN. The gate recess was etched by Cl-based ICP/RIE: the etching depth was about 5 nm, just like the p^+ GaN cap thickness. From numerical simulations, the effect of the gate recess should be a decrease of the 2-DHG concentration by 70-80%. As can be seen in Fig. 5.13, this is confirmed by the decrease of the current approximately by the same value.

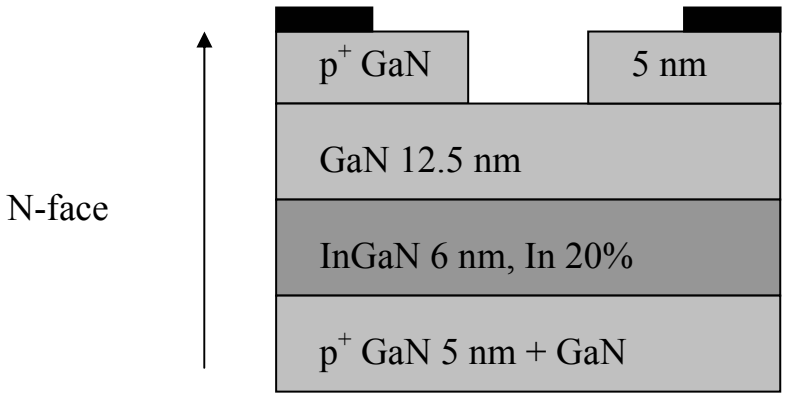

Fig. 5.12: Structure with the gate recess

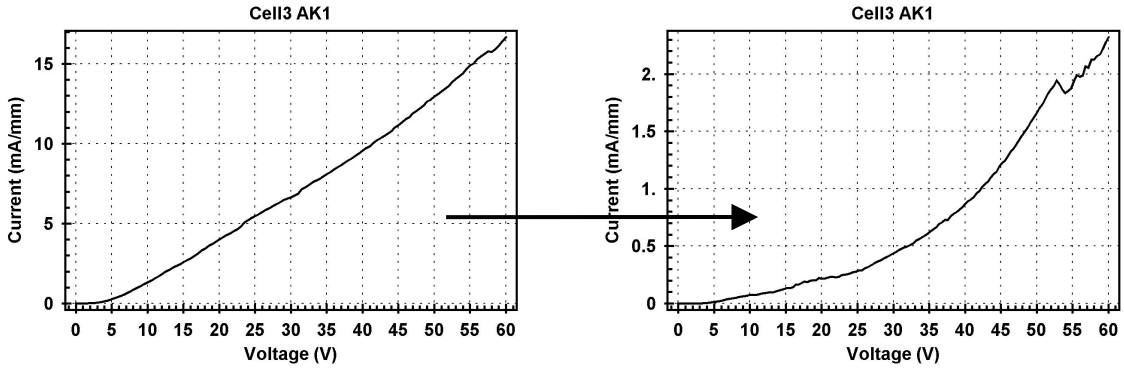

Fig. 5.13: Ids-Vds characteristics of a device before (left) and after (right) gate recess

This appears to be a key result in order to try to prove the presence of a 2-DHG. Not only, in fact, the presence of a hole gas is contemplated by the simulations (and band engineering and doping have been designed on purpose), but experimental results show that the simulation tool is reliable. If the current measured was due to the buffer leakage, in fact, the removal of the top p-GaN layer would have no effects on it: the fact that it decreases tells that there is a carrier concentration at one of the interfaces between GaN and InGaN. Furthermore, the effect of the removal of the top p-GaN layer is to push the band diagram down, so if the current was due to electrons, it should increase, not decrease.

5.4 Conclusions and future work

A novel N-polar GaN/InGaN/GaN structure for the study of p-type conduction in III-Nitrides was presented. Although the results were severely affected by the difficulty in obtaining ohmic contacts, signs of p-type conduction were found. This can be an encouraging step forward in the study of p-type conduction in III-Nitrides, especially in N-polar devices. Future work on this topic may include the improving of the process in order to achieve better ohmic contacts and the optimization of the process, even with *ad hoc* lithography masks, compared to the ones commonly used for traditional HEMTs.

Chapter 6

Al_2O_3 as gate dielectric on GaN

6.1 Introduction

The performance and reliability of GaN high-electron mobility transistors is indeed limited by the gate leakage current. Its decreases the breakdown voltage and affects the RF performance causing the power-added efficiency to drop severely. One way to try and suppress it is to exploit structures like Metal-Insulator-Semiconductor HEMTs (MISHEMTs) or Metal-Oxide-Semiconductor HEMTs (MOSHEMTs). A consistent variety of oxides have been considered and studied for this purpose: SiO_2 [81-83], Si_3N_4 [84-85], HfO_2 [86-88], Al_2O_3 [89-91]. However, the properties of such materials and their interface properties in the III-Nitride systems are still under investigation. In this chapter we will focus our attention on Al_2O_3, which appears already as a leading candidate for the replacement of SiO_2 in future-generation Si digital ICs. Aluminum oxide has a high potential in suppressing the gate leakage in GaN HEMTs: it has a large bandgap (9 eV), a high dielectric constant (about 9 to 10 times ε_0), and high breakdown field. One of the most used techniques of deposition of Al_2O_3 has become atomic layer deposition (ALD), due to its low-defect density, high uniformity, and the possibility to tune the deposition thickness very precisely. That is also the deposition technique used in the samples we report about in this chapter.

Our study focuses on two different aspects of Al_2O_3 on GaN. On one hand, we will study the possibility to obtain hole accumulation in GaN with the help of a metal/Al_2O_3/p-GaN capacitor structure, both for the Ga-polar and the N-polar case. On the other hand, an analysis of the properties of metal/Al_2O_3/n-GaN diodes will be presented, and a technique to estimate the metal-oxide barrier from the tunneling currents analysis will be presented.

6.2 Al_2O_3 on p-GaN: MIS diodes

The samples used in this experiment were grown using a Veeco RF-plasma molecular beam epitaxy system on semi-insulating GaN templates on sapphire (Ga-polar) or on free-standing GaN (N-polar). The epitaxial layer consisted of 200 nm unintentionally doped GaN on substrate followed by 100 nm Magnesium-doped GaN (Fig. 6.1). The oxide layers were deposited in a Picosun atomic layer deposition (ALD) system, using trimethylaluminum (TMA) and H_2O as precursors.

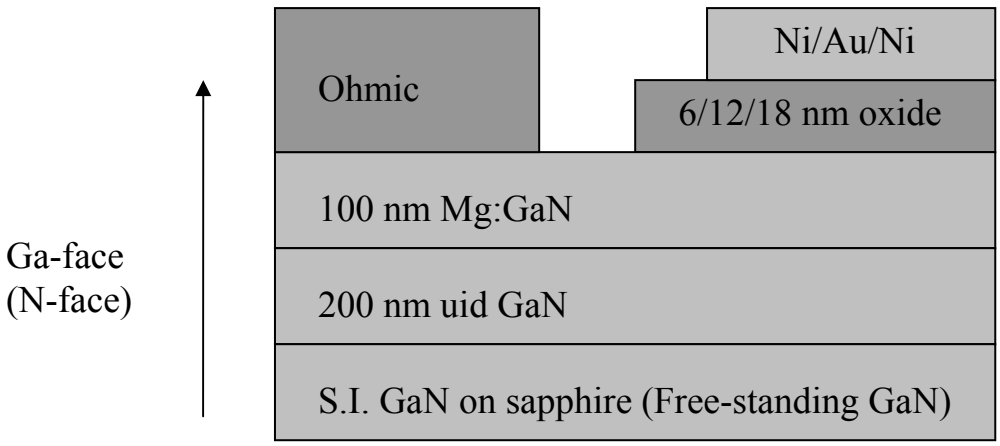

Fig. 6.1: Structure layer of the grown p-GaN samples

After a removal of the excess gallium droplets on the surface, three different thicknesses – 6 nm, 12 nm, and 18 nm – of oxide were deposited at 300˚C on three different pieces cleaved out of the same sample. All six samples (3 Ga-polar, 3 N-polar) were then annealed at 600˚C in forming gas for 1 min. The gate pads were defined by optical contact lithography. Features of large contacts were also defined in the photo resist. Buffered Oxide Etch (BOE) 10:1 was used to remove locally the oxide layer in these large features in order to get ohmic contacts. A Ni/Au/Ni stack was e-beam evaporated and a post metallization annealing was finally performed on all six samples at 400 ˚C in forming gas for 5 min.

6.2.1 Al_2O_3 on Ga-face p-GaN

C-V measurements were performed using an Agilent B1500 semiconductor device analyzer equipped with medium power source/monitor units (MPSMUs) and multi frequency capacitance measurement unit (MFCMU). The results showed a C-V profile with no signs of

hole accumulation for all the three oxide thicknesses. The voltage range over which such measurements could be considered reliable was also limited by the onset of the flow of the gate current, both in direct and in reverse bias. In Fig. 6.2 a C-V profile for the 6-nm oxide sample is reported.

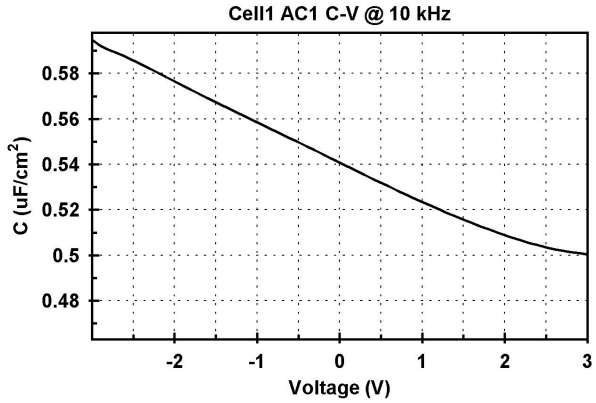

Fig. 6.2: C-V profile for the 6-nm oxide samples

The doping density extracted from the C-V measurement was 10^{20} cm^{-3} for Mg in the GaN. However, the fact that the thickness extracted from the C-V measurements is consistently about 9 nm higher than the oxide thickness appears as a clear indicator that, contrarily to the expectations, the GaN must be depleted. This eventually happens to be consistent with an inversion of the polarity of GaN due to the high doping concentration (Fig. 6.3).

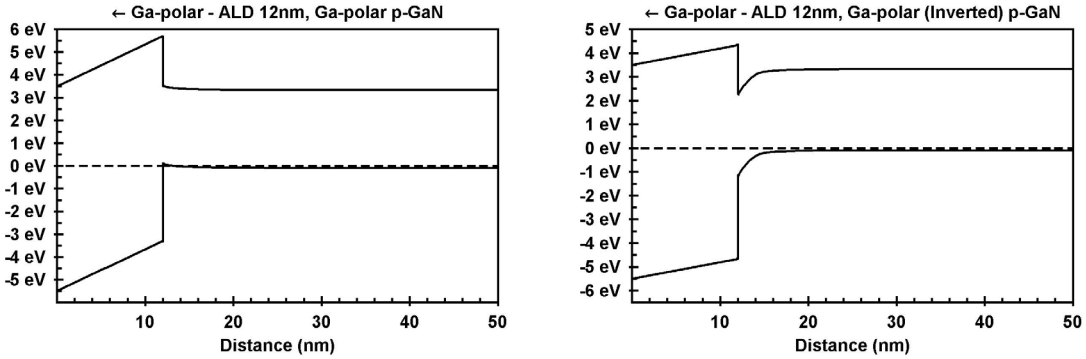

Fig. 6.3: Simulated band diagram for Ga-polar (left) and inverted Ga-polar GaN (right).

The excess of about 9 nm for all the devices can be therefore explained by taking into account the depletion region width in the GaN and the Debye length: considering an effective hole concentration $p = 4.7 \times 10^{17}$ cm^{-3} (from the doping density of 10^{20} cm^{-3}) we have:

$$L_D = \sqrt{\frac{k_B T \varepsilon_0 \varepsilon_r}{q^2 p}} = 5.2nm$$

$$x_A = 9nm - L_D = 3.8nm \tag{6.1}$$

which is consistent with an approximate built-in voltage of 1 – 1.3 V, according to the simulations carried out for the inverted p-GaN case (Fig. 6.3).

So, in the end, even though not a sufficient amount of information could be collected by the experimental results, we can state that the presence of a positive charge at the interface between Al_2O_3 and GaN is the reason for the absence of hole accumulation. One explanation for the origin of such charge could be the polarity inversion of GaN: as reported in [92], an AlO_x transition layer has been proven to be an effective mean for GaN polarity inversion. Another possible origin of such charge could be *fixed* charge, attributed to energy states between the conduction band minima of Al_2O_3 and GaN: as reported in [93], independently of the bias applied, the Fermi level would not be able to modulate these states, and they will therefore behave like "fixed" charges. However, in order to gain a better understanding of the exact phenomena taking place at the interface, further studies shall be carried out.

6.2.2 Al_2O_3 on N-face p-GaN

As reported in Chapter 1, N-polar stacks represent a very interesting opportunity to engineer new types of devices and increase the possibilities of application of III-Nitrides. However, the quality of the material and of the tuning of the growth conditions is a serious issue that has somewhat limited the spread of this new technology so far.

On one hand the measurements carried out on the N-face p-GaN samples showed currents approximately two orders of magnitude lower than in the Ga-polar case; on the other hand, the C-V profile showed an extremely low capacitance, approximately 10-20 times lower than expected. This was believed to be due to a very high resistivity of the sample, and was verified by confronting the capacitance measured in the same conditions on different pads with different areas: in the case of a very resistive substrate, the measured capacitance would be likely to be only the one correspondent to a thin layer on the edge of the pad, due to current crowding effects. In this situation, the capacitance per unit area would not be

constant over different areas, but would be decreasing with the increasing of the total area. Assuming a circular pad with radius R, let r be the radius of the internal pad area not measured, and L the difference between them.

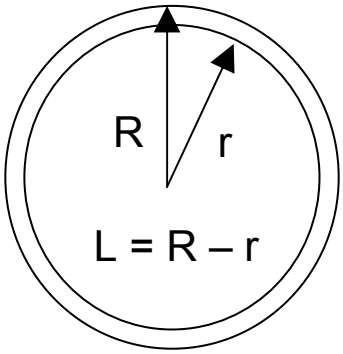

Fig. 6.4: Effective measured area.

Therefore we have

$$A_{eff} = \pi R^2 - \pi r^2 = \pi\left(R^2 - r^2\right) \tag{6.2a}$$

$$\frac{C}{A} = \frac{C}{A_{eff}}\left(1 - \left(1 - \frac{L}{R}\right)^2\right) \tag{6.2b}$$

which represents the following trend:

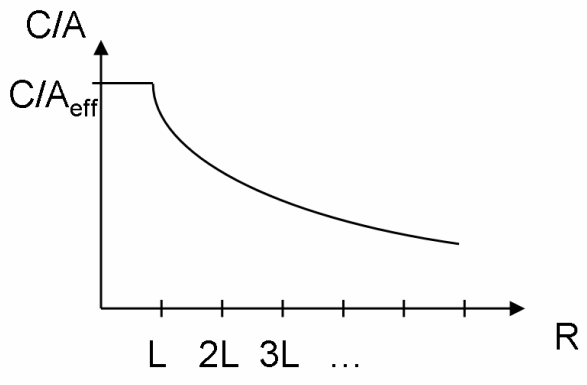

Fig. 6.5: Trend of C/A versus the radius.

Capacitance measurements were carried out on different gate pads with different areas. Though the pads were not circular, their area could be expressed through an equivalent radius Req of 21, 31, and 135 μm, respectively. As can be seen in Fig. 6.6, the trend of the

curve is the same as the one depicted in Fig. 6.5, and this was found in all the N-polar samples.

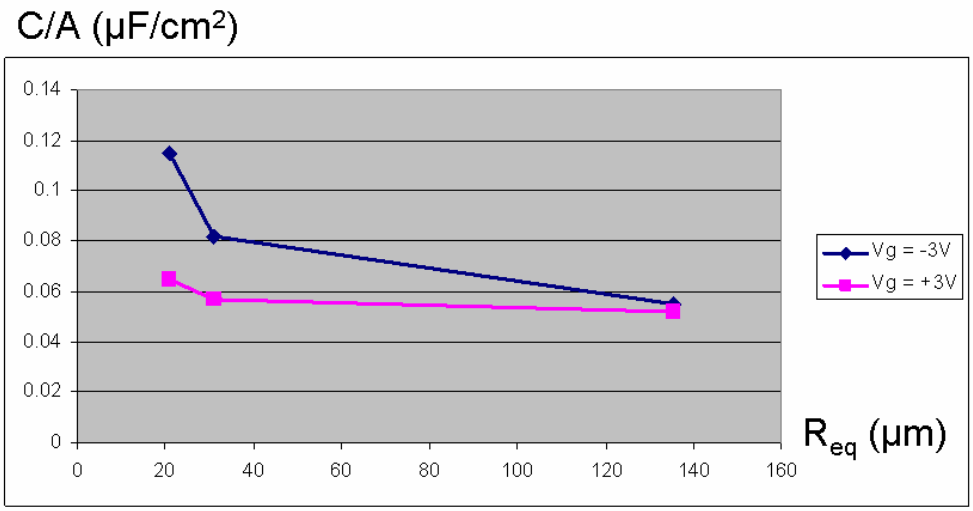

Fig. 6.6: Actual trend of C/A versus the equivalent radius of different gate pads.

The reason for the higher resistivity of N-polar samples could be either an intrinsic worse quality of the epilayer due to the criticalness of the growth of N-face stacks, or to a much less concentration of Magnesium, or both. However, a fitting of the curve in order to try and estimate the parameter L (and therefore the value of the capacitance without the current crowding effect) was not straightforward, for the capacitance at negative bias showed a strong frequency dependence, and L itself appeared to be not constant from pad to pad.

In conclusion, even though the accumulation of holes appears likely to be demonstrated in Al_2O_3/p-GaN stacks according to numerical simulations, particular attention must be paid to the growth condition of GaN, in order to avoid polarity inversion and to keep the interface as ideal as possible. New techniques as Al deposition right after growth before subsequent oxide deposition are currently under investigation.

6.3 Al_2O_3 on Ga-face n-GaN and metal-oxide barrier estimation

For these experiments, samples similar to the ones discussed in Par. 6.2 were used, being the only difference the doping species for the GaN, which is n-type. In Fig. 6.7 the stack grown and processed and an atomic force microscope scan of the as-grown surface is shown [93].

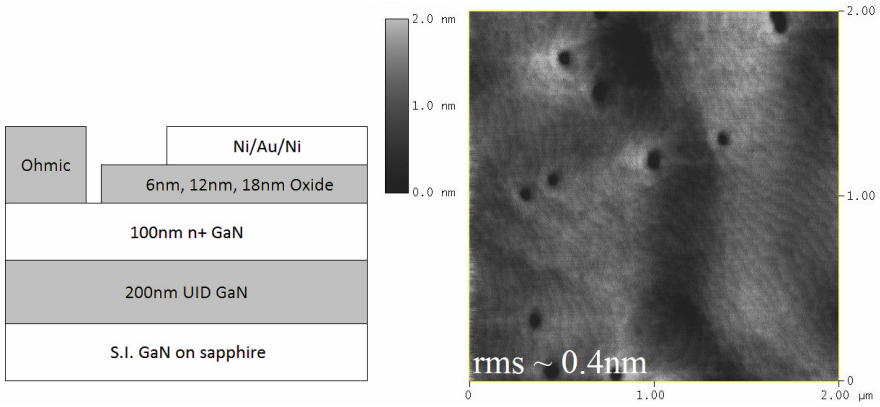

Fig. 6.7: MIS structure and AFM image of the as grown surface [93]

Fig. 6.8 shows the current-voltage measurements for the 6-nm samples in direct bias. A voltage at which the slope of the logarithmic I-V curve clearly changes can be noticed: from the second-order derivative of the curve (shown in the inset), such voltage is calculated to be 3.45 V.

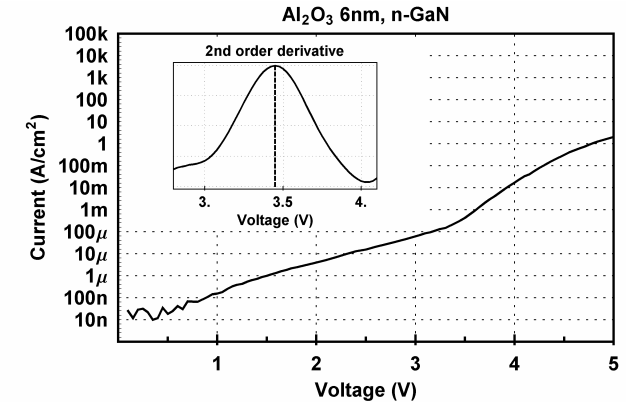

Fig. 6.8: Current-voltage characteristic for the 6-nm samples. Inset: 2nd-order derivative.

In Fig. 6.9 the simulated band diagram for the 6-nm samples is reported both at zero bias (V_G=0), and for V_G=V_{SW}, at which the potential barrier seen by electrons in the 2-dimensional electron gas (2-DEG) in the GaN switches from trapezoidal to triangular. The conduction band offset between Al_2O_3 and GaN was assumed to be 2.13 eV [93]. Simulations were carried out using BandEng [80]. Since the flat-band voltage for the 6-nm samples was found to be 0.8 V [93], 2-DEG starts forming soon, and in the end V_{SW} will simply be equal to Φ_B/q (being Φ_B the barrier height at the Ni/Al_2O_3 interface).

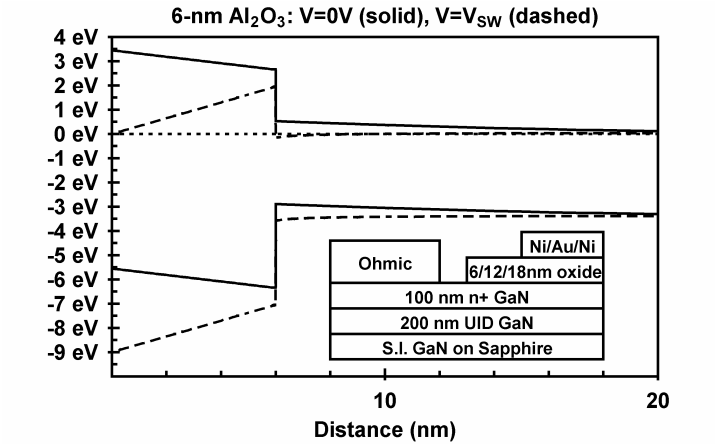

Fig. 6.9: Simulated band diagram of the 6-nm sample both at zero bias and at $V=V_{SW}$

Assuming conduction to be due to tunneling mechanisms only, the voltage $V_G=V_{SW}$ should represent therefore the onset of Fowler-Nordheim (triangular barrier) tunneling regime for the electrons in the 2-DEG. Further analyses of the experimental I-V characteristics actually show that the current above 3.45 V is due to Fowler-Nordheim tunneling, whereas the current below 3.45 V is not (Fig. 6.10). The current in the Fowler-Nordheim tunneling regime is given by:

$$J_{FN} = A \cdot F_{OX}^2 \cdot \exp\left(-\frac{4}{3\hbar q F_{OX}} \sqrt{2m^* \Phi_{Barr}^3} \right) \tag{6.3}$$

where m* is the tunneling effective mass, Φ_{Barr} is the barrier seen by the tunneling electrons (ΔE_C in our case), F_{OX} is the electric field in the oxide, and A is a parameter that depends on Φ_{Barr} and on the tunneling mass. Such behavior is confirmed by the straight line in the FN plot for V_G higher than 3.45 V in Fig. 6.10, whereas the same plot for V_G below 3.45 V (in the inset) shows a clear non-FN behavior.

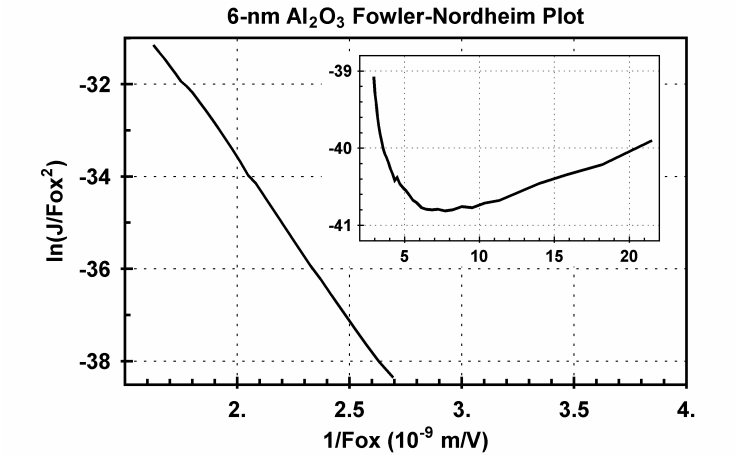

Fig. 6.10: Fowler-Nordheim plot above 3.45 V in the 6-nm samples. Inset: FN plot below 3.45 V.

Therefore, since it has been verified that V_{SW}=3.45 V represents the onset of Fowler-Nordheim tunneling regime, the barrier height Φ_B between Ni and Al_2O_3 is simply found to be equal to 3.45 eV: this value matches previous reports [94] and can be easily inferred by the logarithmic I-V curve itself, for at 3.45 V its slope increases (Fig. 6.8).

Energy band diagram analysis was then used in order to find the electric field in the oxide given the gate voltage for all the samples. Neglecting the distance between the Fermi level and the conduction band edge in the GaN, we obtain the approximate expression:

$$-qV_G + \Phi_B + qF_{OX}t_{OX} - \Delta E_C = 0 \tag{6.4}$$

where V_G is the voltage applied to the gate, Φ_B is the barrier height at the Ni/Al_2O_3 interface (3.45 eV), F_{OX} is the electric field in the oxide, t_{OX} is the oxide thickness, and ΔE_C is the conduction band offset at the Al_2O_3/GaN interface (2.13 eV).

The currents observed in the 12-nm and 18-nm samples were due entirely to Fowler-Nordheim tunneling. The reason for this is the much thicker oxide: a voltage higher than Φ_B/q is required to induce a field in the oxide high enough to trigger a measurable tunneling current, so when the device eventually turns on (i.e., when the current becomes higher than the noise floor of our instruments), the Fowler-Nordheim regime has already been entered. As from Eq. 6.4, Fig. 6.11 shows the current vs. field characteristics of the 6-, 12-, and 18-nm samples. As can be seen, the current in Fowler-Nordheim regime is the same for all the thicknesses, with the 6-nm samples showing the switch from non-FN to Fowler-Nordheim

regime at 3.5 MV/cm, which is simply equal to $\Delta E_C/q$ (2.13 V) divided by the oxide thickness (6 nm).

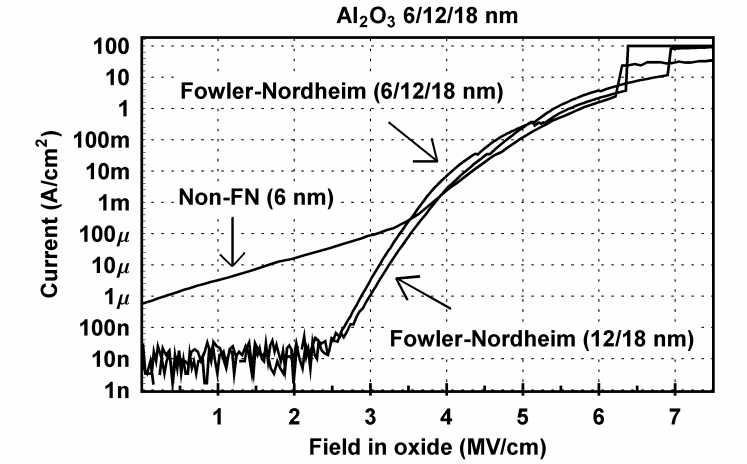

Fig. 6.11: Current density as a function of the field in the oxide for the three samples

Experimental current-voltage curves in FN tunneling regime were fitted according to the Fowler-Nordheim theory (with Φ_{Barr} in Eq. 6.3 being the ΔE_C at the Al_2O_3/GaN interface). An effective tunneling mass of $m_T^* = 0.152\ m_0$ was extracted from the Fowler-Nordheim plots, which is in agreement with [95].

Breakdown measurements for Al_2O_3 were also carried out in forward bias. As from Eq. 6.5, Al_2O_3 eventually showed a breakdown field of 6–7 MV/cm (Fig. 6.11). This value is in accordance with other works in literature [96-97].

Bibliography

[1] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "*GaN-based RF Power Devices and Amplifiers*", Proceedings of the IEEE **96**(2), 287 (2008).

[2] E. Johnson, "*Physical limitations on frequency and power parameters of transistors*", RCA Rev. **26**, 163 (1965).

[3] Y.-F. Wu, "*AlGaN/GaN Microwave Power High-Mobility Transistors*", Ph.D. Dissertation, University of California Santa Barbara, 1997.

[4] B. J. Baliga, "*Power semiconductor device figure of merit for high-frequency applications*", IEEE Electron Device Lett. **10**(10), 455 (1989).

[5] J. Edgar, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 1.2, pp. 7–21.

[6] J. Wu, W. Walukiewicz, K. Yu, J. Ager, E. Haller, H. Lu, W. Schaff, "*Small band gap bowing in $In_{1-x}Ga_xN$ alloys*", Appl. Phys. Lett. **80**, 4741 (2002).

[7] B. Foutz, S. O'Leary, M. Shur, L. Eastman, "*Transient electron transport in wurtzite GaN, InN, and AlN*", J. Appl. Phys. **85**, 7727 (1999).

[8] R. Quay, "*Gallium Nitride Electronics*", Springer-Verlag, 2008.

[9] U. K. Mishra and J. Singh, "*Semiconductor Device Physics and Design*", Springer-Verlag, 2008.

[10] T. Paskova, "*Nitride Materials and Devices with Nonpolar Surfaces: Development and Prospects*", in Nitrides with Nonpolar Surfaces, edited by T. Paskova, Wiley-VCH, 2008.

[11] F. Bernardini, V. Fiorentini, D. Vanderbilt, "*Spontaneous polarization and piezoelectric constants of III-V nitrides",* Phys. Rev. B **56**, R10024 (1997).

[12] E. Yu, G. Sullivan, P. Asbeck, C. Wang, D. Qiao, S. Lau, "*Measurement of piezoelectrically induced charge in GaN/AlGaN heterostructure field-effect transistors*", Appl. Phys. Lett. **71**, 2794 (1997).

[13] O. Ambacher, B. Foutz, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, A. Sierakowski, R. Dimitrov, A. Mitchell, M. Stutzmann, "*Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures*", J. Appl. Phys. **87**, 334 (2000).

[14] Murphy et al., MRS Internet J. Nitride Semicond. Res. 4S1, G8.4(1999).

[15] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "*Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field-effect transistors*", Appl. Phys. Lett. **77**, 250 (2000).

[16] R. Vetury, N. Zhang, S. Keller, and U. K. Mishra, "*The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs*", IEEE Trans. Electron Devices **48**(3), 560, (2001).

[17] S. Rajan, A. Chini, M. Wong, J. S. Speck, and U. K. Mishra, "*N-polar GaN/AlGaN/GaN High Electron Mobility Transistors*", J. of Appl. Phys. **102**, 044501 (2007).

[18] S. Rajan, "*Advanced Polarization Engineering for GaN-based Transistors*", Ph.D. Dissertation, University of California Santa Barbara, 2006.

[19] J. Brinkhoff, A. Parker, in Workshop Applied Radio Science, Hobart, 2004, pp. 1–8.

[20] M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia, "*Current-voltage characteristic collapse in AlGaN/GaN heterostructure insulated gate field effect transistors at high drain bias*", Electronics Lett., **30**(25), 2175 (1994).

[21] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "*Trapping effects and microwave power performance in AlGaN/GaN HEMTs*", IEEE Trans. Electron Devices **48**, 465 (2001).

[22] J. Bernat, P. Javorka, A. Fox, M. Marso, H. Lueth, P. Kordos, "*Effect of surface passivation on performance of AlGaN/GaN/Si HEMTs*", Solid-State Electron. **47**, 2097 (2003).

[23] H. Kim, R. Thompson, V. Tilak, T. Prunty, J. Shealy, L. Eastman, "*Effects of SiN passivation and high-electric field on AlGaN-GaN HFET degradation*", IEEE Electron Device Lett. **24**(7), 421 (2003).

[24] G. Meneghesso, A. Chini, E. Zanoni, M. Manfredi, M. Pavesi, B. Boudart, C. Gaquiere, in IEDM Technical Digest, San Francisco, 2000, pp. 389–392.

[25] S. Binari, P. Klein, T. Kazior, in IEEE International Microwave Symposium Digest, Seattle, 2002, pp. 1823–1826.

[26] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. Mishra, C. Canali, E. Zanoni, "*Surface-related drain current dispersion effects in AlGaN-GaN HEMTs*", IEEE Trans. Electron Devices **51**(10), 1554 (2004).

[27] S. Bradley, A. Young, L. Brillson, M. Murphy, W. Schaff, L. Eastman, "*Influence of AlGaN deep level defects on AlGaN/GaN 2-DEG carrier confinement*", IEEE Trans. Electron Devices **48**(3), 412 (2001).

[28] M. Neuburger, J. Allgaier, T. Zimmermann, I. Daumiller, M. Kunze, R. Birkhahn, D. W. Gotthold, E. Kohn, "*Analysis of surface charging effects in passivated AlGaN-GaN FETs using a MOS test electrode*", IEEE Electron Device Lett. **25**(5), 253 (2004).

[29] P. Klein, S. Binari, K. Ikosso-Anastasiou, A. Wickenden, D. Koleske, R. Henry, D. Katzer, " *Investigation of traps producing current collapse in AlGaN/GaN high electron mobility transistors*", Electronics Lett. **37**(10), 661 (2001).

[30] J. Torvik, J. Pankove, B.V. Zeghbroeck, "*Comparison of GaN and 6H-SiC p-i-n photodetectors with excellent ultraviolet sensitivity and selectivity*", IEEE Trans. Electron Devices **46**(7), 1326 (1999).

[31] A. Chini, "*Fabrication, Characterization and Reliability of AlGaN/GaN HEMTs for Power Microwave Applications*", Ph.D. Dissertation, University of Padova, Italy, 2002.

[32] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "*The Effect of Surface Passivation on the Microwave Characteristics of Undoped AlGaN/GaN HEMTs*", IEEE Electron Device Lett. **21**(6), 268 (2000).

[33] Y.-F. Wu, N. Zhang, J. Xu, M. L. Jian, and M. L. Carthy, U.S. Patent 6 586 781, Jul. 1, 2003, filed in January 29, 2001, grated in.

[34] V. Tilak, B. Green, H. Kim, R. Dimitrov, J. Smart, W. Schaff, J. Shealy, L. Eastman, in Proceedings of the International Symposium Compound Semiconductors, Monterey, 2000, pp. 357–363.

[35] Y.-F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "*30-W/mm GaN HEMTs by field plate optimization*", IEEE Electron Device Lett. **25**(3), 117 (2004).

[36] Y. Huili Xing Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "*High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates*", IEEE Electron Device Lett. **25**(4), 161 (2004).

[37] L. Shen, R. Coffie, D. Buttari, S. Heikman, A. Chakraborty, A. Chini, S. Keller, S. P. DenBaars, and U. K. Mishra, "*High-Power Polarization-Engineered GaN/AlGaN/GaN HEMTs Without Surface Passivation*", IEEE Electron Device Lett. **25**(1), 7 (2004).

[38] J. Joh, J. A. del Alamo. "*Mechanisms for Electrical Degradation of GaN High-Electron Mobility Transistors*", IEEE IEDM Tech. Dig. 2006, pp. 1-4.

[39] A. Chini, M. Esposto, G. Meneghesso, E. Zanoni, "*Evaluation of GaN HEMT degradation by means of pulsed I-V, leakage and DLTS measurements*", IET Electronics Lett. **45**(8), 426 (2009).

[40] A. Chini, V. Di Lecce, M. Esposto, G. Meneghesso, and E. Zanoni, "*Evaluation and Numerical Simulations of GaN HEMTs Electrical Degradation*", IEEE Electron Device Lett. **30**(10), 1021 (2009).

[41] A. Chini, V. Di Lecce, M. Esposto, G. Meneghesso, and E. Zanoni, "*RF Degradation of GaN HEMTs and its correlation with DC stress and I-DLTS measurements*", European Microwave Week—EuMW 2009, Rome (Italy), Sep. 2009.

[42] T. Kikkawa, T. Maniwa, H. Hayashi, M. Kanamura, S. Yokokawa, M. Nishi, N. Adachi, M. Yokoyama, Y. Tateno, and K. Josh, "*An Over 200-W Output Power GaN HEMT Push-Pull Amplifier with High Reliability*", IEEE MTT-S International Microwave Symposium Digest, Fort Worth TX, USA, 2004, pp. 1347–1350.

[43] C. Lee, L. Witkowski, M. Muir, H. Q. Tserng, P. Saunier, H. Wang, J. Yang, and M. A. Khan, "*Reliability Evaluation of AlGaN/GaN HEMTs grown on SiC Substrate*", in Proc. IEEE Lester Eastman Conference on High Performance Devices, Newark DE, USA, 2002, pp. 463–442.

[44] A. M. Conway, M. Chen, P. Hashimoto, P. J. Willadsen, and M. Micovic, "*Failure Mechanisms in GaN HFETs under Accelerated RF Stress*", in CS-MANTECH Conf. *Proc.*, Austin TX, 2007, pp. 99–102.

[45] C. Lee, L. Witkowski, H. Q. Tserng, P. Saunier, R. Birkhahn, Dan Olson, Don Olson, G. Munns, S. Guo, and B. Albert, "*Effects of AlGaN/GaN HEMT structure on RF reliability*", IET Electronics Lett. **41**(3), 155 (2005).

[46] A. P. Zhang, E. B. Kaminsky, A. F. Allen, J. W. Hedrick, A. Vertiatchikh, and L. F. Eastman, "*Stability of AlGaN/GaN high-power HEMTs under DC and RF stresses*", IET Electronics Lett. **40**(19), 1229 (2004).

[47] P. Valizadeh, D. Pavlidis, "*Effects of RF and DC Stresses on AlGaN-GaN MODFETs: A Low-Frequency Noise-Based Investigation*", IEEE Trans. Device Mater. Rel. **5**(3), 555 (2005).

[48] J. Joh and J. A. del Alamo, "*RF power degradation of GaN High Electron Mobility Transistors*", IEEE IEDM Tech. Dig. 2010, pp. 468-471.

[49] E. Zanoni, F. Danesin, M. Meneghini, A. Cetronio, C. Lanzieri, M. Peroni and G. Meneghesso, "*Localized damage in AlGaN/GaN HEMTs induced by reverse bias testing*", IEEE Electron Device Lett. **30**(5), 427 (2009).

[50] P. Makaram, J. Joh, J. A. del Alamo, T. Palacios, and C. V. Thompson, "*Evolution of structural defects associated with electrical degradation in AlGaN/GaN high electron mobility transistors*", Appl. Phys. Lett. **96**, 233509 (2010).

[51] Joh Jungwoo, J. A. del Alamo, "*Impact of Electrical Degradation on Trapping characteristics of GaN High Electron Mobility Transistors*", IEEE IEDM Tech. Dig. 2008.

[52] D. Marcon, T. Kauerauf, J. Das, M. Van Hove, P. Srivastava, K. Cheng, M. Leys, R. Mertens, S. Decoutere, G. Meneghesso, E. Zanoni, and G. Borghs, "*A comprehensive reliability investigation of the voltage-, temperature- and device geometry dependence of the gate degradation on state-of-the-art GaN-on-Si HEMTs*", IEEE IEDM Tech. Dig. 2010, pp. 472-475.

[53] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, E. Zanoni, "*Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives*" IEEE Trans. Device Mater. Rel. **8**(2), 332 (2008).

[54] D. Marcon, A. Lorenz, J. Derluyn, J. Das, F. Medjdoub, K. Cheng, S. Degroote, M. Leys, R. Mertens, M. Germain, and G. Borghs, "*GaN-on-Si HEMT stress under high electric field condition*" Phys. Status Solidi C **6**, S1024 (2009).

[55] S. C. Cripps, "*RF Power Amplifiers for Wireless Communications*", Norwood, MA: Artech House, 1999, pp. 50-51.

[56] A. Chini, D. Buttari, R. Coffie, L. Shen, S. Heikman, A. Chakraborty, S. Keller, and U. K. Mishra, "*Power and Linearity Characteristics of Field-Plated Recessed-Gate AlGaN-GaN HEMTs*", IEEE Electron Device Lett. **25**(5), 229 (2004).

[57] K. Lee, M. S. Shur, A. J. Valois, G. Y. Robinson, X. C. Zhu, and A. Van Der Ziel, "*A New Technique for Characterization of the "End" Resistance in Modulation-Doped FET's*", IEEE Trans. on Electron Devices **31**(10), 1394 (1984).

[58] S. Demirtas and J. A. del Alamo, "*Critical voltage for electrical reliability of GaN high electron mobility transistors on Si substrate*", Reliability of Compound Semiconductors Digest (ROCS), pp. 53-56, 2009.

[59] S. Demirtas and J. A. del Alamo, "*Effect of Trapping on the Critical Voltage for Degradation in GaN High Electron Mobility Transistors*", IEEE International Reliability Physics Symposium (IRPS), pp. 134-138, May 2010.

[60] J. Orton, C. Foxon, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 8.4, pp. 294–299.

[61] J. Orton, C. Foxon, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 8.5, pp. 300–305.

[62] C. Lee and H. Kao, "*Long-term thermal stability of Ti/Al/Pt/Au Ohmic contacts to n-type GaN*", Appl. Phys. Lett. **76**, 2364 (2000).

[63] R. Thompson, T. Prunty, V. Kaper, J. Shealy, "*Performance of the AlGaN HEMT structure with a gate extension*", IEEE Trans. Electron Devices **51**(2), 292 (2004).

[64] W. Hanson, R. Borges, J. Brown, J. Cook, T. Gehrke, J. Johnson, K. Linthicum, S. Peters, E. Piner, P. Rajagopal, J. Robert, S. Singhal, R. Therrien, and A. Vescan, "Development of a GaN transistor process for linear power applications", 2004 International Conference on Compound Semiconductor Manufacturing Technology (GaAs MANTECH), Miami, 2004, pp.107-110.

[65] F. Ren, J. Han, R. Hickman, J.V. Hove, P. Chow, J. Klaasen, J. LaRoche, K. Jung, H. Cho, X. Cao, S. Donovan, R. Kopf, R. Wilson, A. Baca, R. Shul, L. Zhang, C. Willison, C. Abernathy, and S. Pearton, "*GaN/AlGaN HBT fabrication*", Solid-State Electron. **44**, 239 (2000).

[66] J. Kim, J. Je, J. Lee, Y. Park, T. Kim, I. Jung, B. Lee, and J. Lee, "*Microstructural and electrical investigation of Ni/Au ohmic contact on p-type GaN*", J. Electron. Mater. **30**, L8 (2001).

[67] B. Shelton, D. Lambert, J. Huang, M. Wong, U. Chowdhury, T. Zhu, H. Kwon, Z. Weber, M. Benarama, M. Feng, and R. Dupuis, "*Selective area growth and characterization of AlGaN/GaN heterojunction bipolar transistors by metalorganic*

chemical vapor deposition", IEEE Trans. Electron Devices **48**(3), 490 (2001).

[68] J. Sheu, Y. Su, G. Chi, P. Koh, M. Jou, C. Chang, C. Liu, and W. Hung, "*High-transparency Ni/Au ohmic contact to p-type GaN*", Appl. Phys. Lett. **74**, 2340 (1999).

[69] V. Ramachandran, R. M. Feenstra, W. L. Sarney, L. Salamanca-Riba, J. E. Northrup, L. T. Romano, and D. W. Greve, "*Inversion of wurtzite GaN(0001) by exposure to magnesium*", Appl. Phys. Lett. **75**, 808 (1999).

[70] L. T. Romano, J. E. Northrup, A. J. Ptak and T. H. Myers, "*Faceted inversion domain boundary in GaN films doped with Mg*", Appl. Phys. Lett. **77**, 2479 (2000).

[71] H. K. Choa, J. Y. Lee, S. R. Jeon, and G. M. Yang, "*Influence of Mg doping on structural defects in AlGaN layers grown by metalorganic chemical vapor deposition*", Appl. Phys. Lett. **79**, 3788 (2001).

[72] H. K. Choa, B. H. Kong, Z. Ren, J. Han, and S.-R. Jeon, "*Inversion domain boundaries and phase separation in p-AlGaN layers with high Al contents*", Appl. Phys. Lett. **88**, 231905 (2006).

[73] D. S. Green, E. Haus, F. Wu, L. Chen, U. K. Mishra, and J. S. Speck, "*Polarity control during molecular beam epitaxy growth of Mg-doped GaN*", J. Vac. Sci. Technol. B **21**(4), 1084 (2003).

[74] M. S. Shur, A. D. Bykhovski, and R. Gaska, "*Two-dimensional hole gas induced by piezoelectric and pyroelectric charges*", Solid-State Electronics **44**, 205 (2000).

[75] M. S. Shur, A. D. Bykhovski, R. Gaska, J. W. Yang, G. Simin, and M. A. Khan, "*Accumulation hole layer in p-GaN/AlGaN heterostructures*", Appl. Phys. Lett. **76**, 3061 (2000).

[76] K. Kumakura, T. Makimoto, and N. Kobayashi, "*Activation energy and electrical activity of Mg in Mg-doped $In_xGa_{1-x}N(x < 0.2)$*" Jpn. J. Appl. Phys., pt. 2, **39**(4B), L337 (2000).

[77] T. Zimmermann, M. Neuburger, M. Kunze, I. Daumiller, A. Denisenko, A. Dadgar, A. Krost, and E. Kohn, "*P-Channel InGaN-HFET Structure Based on Polarization Doping*", IEEE Electron Device Lett. **25**(7), 450 (2004).

[78] A. Chini, Y. Fu, S. Rajan, J. S. Speck, and U. K. Mishra, "*An Experimental Method to Identify Bulk and Surface Traps in GaN HEMTs*", in 32nd International Symposium on Compound Semiconductors (ISCS), Europa-Park Rust, Germany, 2005.

[79] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. Sankara Narayanan, "*High Density Two-Dimensional Hole Gas Induced by Negative Polarization at GaN/AlGaN Heterointerface*", Appl. Phys. Express **3**, 121004 (2010).

[80] Michael Grundmann. BandEng. http://my.ece.ucsb.edu/mgrundmann/bandeng/.

[81] G. Simin, X. Hu, N. Ilinskaya, A. Kumar, A. Koudymov, J. Zhang, M. Asif Khan, R. Gaska, and M. S. Shur, "*7.5 kW/mm^2 current switch using AlGaN/GaN metal-oxide-*

semiconductor heterostructure field effect transistors on SiC substrates", IET Electronics Lett. **36**(24), 2043 (2000).

[82] A. Koudymov, X. Hu, K. Simin, G. Simin, M. Ali, J. Yang, and M. Asif Khan, "*Low-loss high power RF switching using multifinger AlGaN/GaN MOSHFETs*", IEEE Electron Device Lett. **23**(8), 449 (2002).

[83] G. Simin, A. Koudymov, H. Fatima, J. Zhang, J. Yang, M. Asif Khan, X. Hu, A. Tarakji, R. Gaska, M. S. Shur, "*SiO_2/AlGaN/InGaN/GaN MOSDHFETs*", IEEE Electron Device Lett. **23**(8), 458 (2002).

[84] G. Simin, X. Hu, N. Ilinskaya, J. Zhang, A. Tarakji, A. Kumar, J. Yang, M. Asif Khan, R. Gaska, and M. S. Shur, "*Large periphery high-power AlGaN/GaN metal-oxide-semiconductor heterostructure field effect transistors on SiC with oxide-bridging*", IEEE Electron Device Lett. **22**(2), 53 (2001).

[85] X. Hu, A. Koudymov, G. Simon, J. Yang, M. Asif Khan, A. Tarakji, M. S. Shur, and R. Gaska, "*Si3N4/AlGaN/GaN–metal–insulator–semiconductor heterostructure field–effect transistors*", Appl. Phys. Lett. **79**, 2832 (2000).

[86] X. Xin, J. Shi, L. Liu, J. Edwards, K. Swaminathan, M. Pabisz, M. Murphy, L. F. Eastman, and M. Pophristic, "*Demonstration of Low-Leakage-Current Low-On-Resistance 600-V 5.5-A GaN/AlGaN HEMT*", IEEE Electron Device Lett. **30**(10), 1027 (2009).

[87] J. Shi, L. F. Eastman, X. Xin, and M. Pophristic, "*High performance AlGaN/GaN power switch with HfO_2 insulation*", Appl. Phys. Lett. **95**, 042103 (2009).

[88] J. Shi and L. F. Eastman, "*Correlation Between AlGaN/GaN MISHFET Performance and HfO_2 Insulation Layer Quality*", IEEE Electron Device Lett. **32**(3), 312 (2011).

[89] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, "*GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al_2O_3 as gate dielectric*", Appl. Phys. Lett. **86**, 063501 (2005).

[90] D Gregušová, R Stoklas, K Čičo, T Lalinský and P Kordoš, "*AlGaN/GaN metal–oxide–semiconductor heterostructure field-effect transistors with 4 nm thick Al_2O_3 gate oxide*", Semicond. Sci. Technol. **22**, 947 (2007).

[91] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, and V. Sahmuganathan, "*Improved two-dimensional electron gas transport characteristics in AlGaN/GaN metal-insulator-semiconductor high electron mobility transistor with atomic layer-deposited Al_2O_3 as gate insulator*", Appl. Phys. Lett. **95**, 223501 (2009).

[92] M. H. Wong, F. Wu, J. S. Speck, and U. K. Mishra, "*Polarity inversion of N-face GaN using an aluminum oxide interlayer*", J. Appl. Phys. **108**, 123710 (2010).

[93] M. Esposto, S. Krishnamoorthy, D. N. Nath, S. Bajaj, T.-H. Hung, and S. Rajan, "*Electrical properties of atomic layer deposited aluminum oxide on gallium nitride*", Appl. Phys. Lett. **99**, 133503 (2011).

[94] V.V. Afanas'ev, M. Houssa, A. Stesmans, and M.M. Heyns: "*Band alignments in metal–oxide–silicon structures with atomic-layer deposited Al_2O_3 and ZrO_2*", Appl. Phys. Lett. **91**(5), 3079 (2002).

[95] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, D. Jena, "*Barrier Height, Interface Charge and Tunneling Effective Mass in ALD AI203/AIN/GaN HEMTs*", 69th Annual Device Research Conference Proceedings, IEEE, pp. 121-122 (2011).

[96] H. C. Lin, P. D. Ye, and G. D. Wilk, "*Leakage current and breakdown electric-field studies on ultrathin atomic-layer-deposited Al_2O_3 on GaAs*", Appl. Phys. Lett. **87**, 182904 (2005).

[97] H. Bartzsch, D. Glöß, B. Böcher, P. Frach, and K. Goedicke, "*Properties of SiO_2 and Al_2O_3 films for electrical insulation applications deposited by reactive pulse magnetron sputtering*", Surface and Coatings Technology **174–175**, 774 (2003).