Reliability Physics of Ferroelectric/Negative Capacitance Transistors for Memory/Logic Applications: An Integrated Perspective

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ABSTRACT

Despite the remarkable development in ferroelectric HfO_2-based FETs, key reliability challenges (e.g. endurance) may still limit their widespread adoption in memory and logic applications. In this paper, we present a simple theoretical framework – based on the Landau theory of phase transition – to design both ferroelectric FETs (FeFETs) and negative capacitance transistors (NCFETs) and investigate their reliability issues. For FeFETs, we analyze the role of interface and bulk traps on memory window closure to quantify endurance under different operating conditions. For NCFETs, we discuss the beneficial role of NC effect in reducing (or even eliminating) the persistent reliability issue of negative bias temperature instability (NBTI) that has plagued MOSFETs for decades. Both devices could also suffer from the Hot Atom Damage (HAD), i.e., switching-induced bond dissociation during transient overshoot. We conclude by discussing how other reliability issues (e.g. TDDB, HCD, etc.) may also have to be reinterpreted for FE/NCFETs.

KEYWORDS

Ferroelectric HfO_2; Ferroelectric FETs; Negative Capacitance FETs; Endurance; NBTI; Reliability.

1. INTRODUCTION

Employing a ferroelectric (FE) layer in the gate stack of a metal-oxide-semiconductor field-effect transistor (MOSFET) significantly enhances the functionality of the device by enabling simultaneous data storage and logic operation [1] on the one hand, and, steep-slope operation for ultra-low power consumption on the other [2]. The ferroelectric transistor that uses the polarization charge to store data for memory application, combined with the logic functionality intrinsic to the MOSFET operation, is called FeFET, whereas the device that exploits the so-called "negative capacitance" (NC) effect to achieve voltage amplification (and thus sub-thermionic switching) is called NCFET [1].

While the first demonstration of a FeFET dates back to the 1960s [3], the concept of NCFET has been proposed relatively recently in 2008 [2] with the first demonstration following immediately thereafter [4]. Despite decades-long refinements, the persistent challenges associated with process integration beyond the 130nm node, retention loss [5], and per-bit cost of perovskite ferroelectrics (e.g. PZT, BaTiO, etc.)-based memories/devices [6] have limited their practical use only to niche applications [6]–[9]. In this context, the prospects of FeFETs and NCFETs changed dramatically by the discovery of ferroelectric properties in crystalline HfO_2 and ZrO_2 in 2011 [10], [11], which was thereafter exploited to realize scaled FeFETs [12]–[14] as well as NCFETs [15]–[17].

While there is a worldwide effort focused on the performance metrics of ferroelectric HfO_2-based FeFET and NCFETs (i.e,, subthreshold slope, negative-DIBL, switching speed, power consumption, scalability, and process compatibility with complementary metal-oxide-semiconductor technology, CMOS), the corresponding reliability issues (i.e., the capability of these devices to maintain their performance metrics within the specified margin over a prescribed period of operation) remain relatively unexplored or not fully solved [1], [9]. Despite the novelty of both technologies (the first reports of HfO_2-based FETs date back to only about 10 years), it is important to treat performance and reliability on equal footing as it is well known from Si MOSFET literature that fundamental reliability (and variability) issues might reduce significantly the design margins of circuits based on CMOS technology, especially at ultra-scaled nodes [18]. Therefore, the true advantages of HfO_2-based FeFETs and NCFETs over other emerging technologies can only be determined by performing a careful assessment of both performance and reliability.

In this paper, we propose an integrative theoretical framework based on the Landau Theory to investigate the reliability of HfO_2-based FeFETs and NCFETs. Although reliability concerns are in general different for these two classes of devices depending on operating conditions, design, application, etc., we show how they can be analyzed with the same theoretical framework presented here. For the purpose of this work, FeFETs are intended for memory applications only (due to the non-volatile storage of polarization charge), whereas NCFETs are for logic applications only (due to the steep-switching behavior guaranteed by the negative capacitance effect). We first review the features of this model – developed from the simple "single-domain" Landau-Devonshire theory of phase transition – and then derive some general rules to identify the design space of

FeFETs and NCFETs. We then present the derivation of a simple analytical formula that accounts for the interface and oxide traps generation that leads to the closure of the memory window (*MW*) in FeFETs, which is the most pressing challenge to endurance of these memories. Then, we discuss the principles of negative bias temperature instability (NBTI)-free operation in NCFETs, by showing how the negative feedback action obtained through the stabilized NC effect can effectively reduce (or even suppress) this persistent reliability issue of traditional MOSFETs. Finally, we interpret a specific reliability aspect of both FeFETs/NCFETs, namely Hot Atom Damage (HAD) [19]–[21], with the established theoretical framework, as well as discuss the design strategies that can be adopted to mitigate it. The modeling based on Landau theory of performance and reliability should be considered as an initial conceptual framework to capture the essence of these reliability challenges. In future, the model must be generalized further to analyze issues associated with polycrystallinity, multi-domain "history effect", etc. [22], [23].

To summarize, both hysteretic (FeFET) and steep-switching (NCFET) operation can be described with the same set of equations derived from Landau theory. The two devices, however, have very different design space and operating conditions. Consequently, the proposed theoretical framework allows investigating the reliability issues of either FeFETs or NCFETs, considering that the specific design and operating conditions (e.g., bias, frequency, etc.) of the two devices determine the specific degradation mechanisms that would eventually dictate the functional reliability of the devices.

2. FEFET AND NCFET DESIGN RULES

To understand the design rules of FeFET and NCFET one needs to first derive the body factor *m* of the device. We will consider only the electrostatics for simplicity and thus ignore short channel effects [24]. In this case, it is useful to consider the gate stack as depicted in Figure 1.

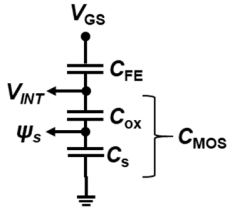

Figure 1. Simplified capacitance network representing the gate stack of a FeFET/NCFET.

From the simple capacitance network of Figure 1 one can thus write the body factor *m* expression as:

$$m \equiv \left(\frac{d\psi_s}{dV_{GS}}\right)^{-1} = \left(\frac{d\psi_s}{dV_{INT}} \cdot \frac{dV_{INT}}{dV_{GS}}\right)^{-1} = \left(1 + \frac{C_s}{C_{ox}}\right)\left(1 - \frac{C_{MOS}}{|C_{FE}|}\right), \tag{1}$$

where C_{FE}, C_{ox}, C_s are the ferroelectric, oxide, and semiconductor capacitances (see Figure 1), and $C_{MOS}^{-1} = C_{ox}^{-1} + C_s^{-1}$. In general, the steady state (i.e., $\rho = 0$) C_{FE} expression can be derived by considering $Q = \varepsilon_{FE}E+P$ (i.e., by imposing the continuity of the displacement field between the ferroelectric, insulator, and semiconductor) [34], and reads:

$$C_{FE} = \frac{1}{t_{FE}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)} + \frac{\varepsilon_{FE}}{t_{FE}}. \tag{2}$$

Because C_{FE} as expressed in Eq. (2) represents a differential capacitance (the first term in fact is obtained from Eq. (11) discussed in Methods as $(\partial E/\partial P)^{-1}$), the voltage drop across the ferroelectric should be accordingly evaluated as $V_{FE} = \int C_{FE}^{-1} dQ$. Without loss of generality, in this section we consider $C_{FE} = (\partial E/\partial P)^{-1} = [t_{FE}(2\alpha+12\beta P^2+30\gamma P^4)]^{-1} < 0$ (i.e., $\varepsilon_{FE} = 0$) for simplicity.

From Eq. (1), one can show that from the point of view of electrostatics, stabilized NC effect can be accessed if the following is satisfied:

$$C_{MOS} < |C_{FE}| < C_{ox}. \tag{3}$$

The first inequality in Eq. (3) needs to be satisfied for hysteresis-free operation, whereas the second one (i.e., the same as Eq. (13) considering the linear term only) ensures that voltage amplification occurs (i.e., $dV_{INT}/dV_{GS} > 1$). On the other hand, if $C_{MOS} > |C_{FE}|$ then hysteresis will appear in the *I–V* transfer curves and thus FeFET operation is achieved. Notice that in general hysteresis does not necessarily imply non-volatility, as this property is achieved when the stored state can be read even with no or small applied bias. However, since in most cases the *P–E* loop of ferroelectrics is symmetric with respect to the origin (except for intended volatile designs), hysteretic behavior implies non-volatility.

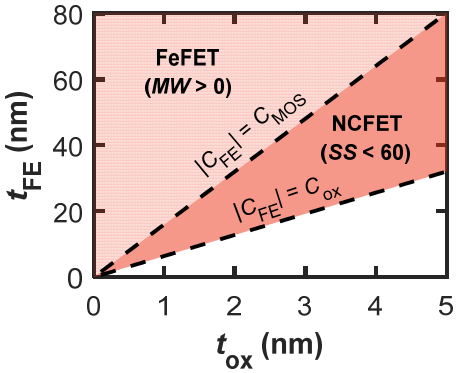

Figure 2. FeFET/NCFET design space considering a constant $C_{MOS} = 2/5 \times C_{ox}$ (i.e., assuming the semiconductor capacitance $C_s = C_D$, depletion capacitance). Al_2O_3 ($\kappa_{ox} = 8$) was considered, $\alpha = -1.1 \times 10^9$ m/F, $\beta = 3.3 \times 10^{10}$ m^5/(C^2 F) as in [25].

Eq. (3) is plotted in Figure 2 for $C_{MOS} = 2/5 \times C_{ox}$ (i.e., assuming the semiconductor to be biased in the depletion region). Ferroelectric parameters were taken from [25]. From Figure 2, one can appreciate the constraints on t_{FE} and t_{DE} to either obtain hysteretic (FeFET) or NC operation (NCFET). In general, one should consider the bias-dependence in C_s [26], [27] as well as additional capacitance contributions from interface traps, parasitic as well as quantum effects [24]. Thus, although the constraints obtained from Eq. (3) are valid only as a first approximation, they provide a useful conceptual tool to think about FeFET/NCFET design.

Since in a well-designed NCFET $0 < m < 1$, the sub-threshold swing, $SS = (2.3 k_B T/q) \times m \approx 60 \times m$ mV/dec (with q being the elementary charge, k_B the Boltzmann constant, and T the temperature), is always lower than the thermionic limit of 60 mV/dec (at room temperature). Designing $|C_{FE}|$ as close as possible to C_{MOS} reduces SS but for $|C_{FE}| \leq C_{MOS}$ hysteresis will be present. This is, however, not the ideal design space for an NCFET, but rather for FeFET operated as a memory device. In this case, the most important parameter is the so-called memory window (MW), i.e., difference between high and low threshold voltages (V_{th}). The MW expression of MFIS FeFETs can be analytically derived with the theoretical framework based on the LT presented earlier; it can be shown that MW expression is [27], [28]:

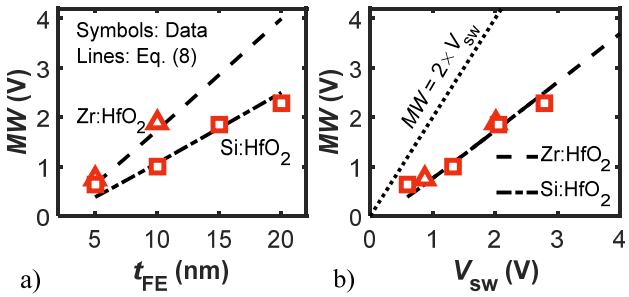

Figure 3. MW vs (a) t_{FE} and (b) V_{sw} for Zr- and Si-doped HfO_2 obtained from data in [29] (symbols) and compared with the MW analytical expression (lines), see Eq. (4). Adapted from [28].

$$MW = -(2V_t + V_{sw}) + 2V_t \ln\left(-\frac{4}{3}\frac{V_t}{V_{sw}}\right), \tag{4}$$

where $V_t = k_B T/q$ is the thermal voltage, $Q_{sw} = (-a/3b)^{1/2}$, $V_{sw} = -2/3\ aQ_{sw}$, $a = 2\alpha t_{FE} + 1/C_{ox}$, and $b = 4\beta t_{FE}$. Eq. (4) is shown in Figure 3 vs t_{FE} (a) and V_{sw} (b), respectively (with parameters set according to materials/geometries in [29]), correctly anticipating the linear dependence on t_{FE} observed from experiments [29] and predicted by other models (e.g., Preisach model [30], [31]).

According to both theory and experiments [29], [32], [33], the actual MW is always below the theoretical maximum of $2E_C \times t_{FE}$ (E_C being the coercive field of the ferroelectric); this can also be deduced from Eq. (4), as $V_{sw} \sim E_{C,LK} \times t_{FE}$ and $MW < 2V_{sw}$ as shown in Figure 3(b).

3. ENDURANCE OF FEFETs

One of the most pressing challenges to the widespread adoption of HfO_2-based FeFETs is their limited endurance, i.e., the ability of the memory to maintain its stored data after repeated writing cycles. Endurance values reported in the literature are typically in the 10^4–10^6 range [30], [33], [35] (depending on writing conditions and device design) although higher endurance – approaching 10^{12} cycles – has been recently reported [15], [36]. Still, there is considerable room for improvement to reach

the target set by recent technology roadmap (>10^{14}) [37] or best values reported for other emerging non-volatile memories (10^{15}–10^{16}), see [38] and references therein. Typically endurance is assessed by reading the state of the FeFET by performing I_D-V_G sweeps after the application of positive/negative writing gate pulses [39]. The writing sequence is repeated multiple times until gate stack breakdown occurs; the number of cycles (N) until breakdown is thus defined as the endurance limit of the device. Either bipolar or unipolar (i.e., always positive or negative) writing sequences can be applied for this kind of tests [39], as shown in Figure 4.

The main limiting factor to endurance in FeFETs is the wear out of the interfacial (IL) layer between the ferroelectric and the semiconductor [39]. The IL layer can be subject to very large fields during writing (in excess of tens of MV/cm [30]) which trigger trap generation either at the IL/semiconductor interface or in the IL itself [35], [40]. The MW analytical expression, see Eq. (4), can be straightforwardly generalized to account for the V_{th}'s shift due to the generated traps as follows [28], see Eq. (5).

$$\begin{aligned} \Delta MW = {} & 2V_t \ln\left(1+\frac{q\Delta D_{it,P}}{C_{eq}}\right)\times\left(1+\frac{q\Delta D_{it,P}}{C_{eq}}\right) \\ & -\frac{q}{C_{eq}}\left\{\left(\Delta N_{ot,P}-\Delta N_{ot,E}\right)-2V_t\Delta D_{it,P}\left[ln\left(\frac{2V_t}{|a|Q_0}\right)-1\right]+2V_t\Delta D_{it,E}\,ln\left(\frac{Q_{sw}}{Q_0}\right)+\left(\Delta D_{it,P}-\Delta D_{it,E}\right)\phi_b\right\}. \end{aligned} \tag{5}$$

In Eq. (5), $C_{eq}^{-1}=C_{FE}^{-1}+C_{ox}^{-1}$, φ_B is the body potential, $\Delta N_{ot,P/E}$ ($\Delta D_{it,P/E}$) is the generated oxide trap density (interface trap density of states) during either program (PGR) or erase (ERS) operation, see Figure 4 and $Q_0=(2\varepsilon_s k_B T n_i^2/N_a)^{1/2}$ (ε_s is the semiconductor dielectric constant, N_a is the semiconductor body doping, and n_i is the intrinsic carrier concentration). The ΔMW expression was validated against experimental data from [35] as shown in Figure 5 for different gate program pulse eight $|V_{P/E}|$. From the fitting of ΔV_{th} and ΔMW data in [28], an empirical power law for generated oxide defects $\Delta N_{ot} \sim N_0 \times t^n$ was extracted with exponent n = 0.3–0.5, possibly being signature of enhanced oxide defect-generation due to repeated cycling reducing Time-dependent Dielectric Breakdown (TDDB) lifetime [28].

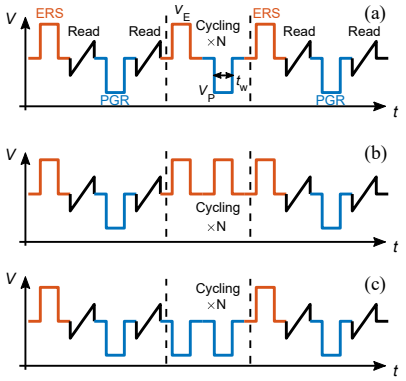

Figure 4. Gate voltage-time waveforms for (a) bipolar (b) positive unipolar and (c) negative unipolar endurance tests. Cycling is performed by repeating many times (up to N, endurance limit) the writing sequence.

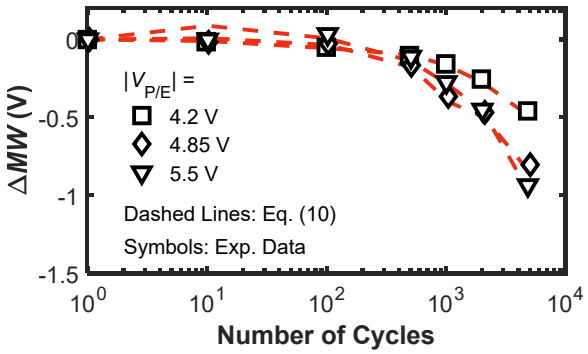

Figure 5. Comparison of ΔMW vs program/erase cycles calculated with Eq. (5) (dashed lines) and experimental data [35] (symbols). Adapted from [28].

Once the amount of generated traps is determined depending on the amplitude/duration of gate pulses, Eq. (5) can be used to evaluate the impact on endurance under a variety of cycling conditions. As such, the analytical model could serve either as an add-on to traditional techniques or as a stand-alone method to characterize endurance for different generated defect densities and writing conditions [28]. For instance, it is possible to estimate the net generated traps from the ΔMW expression as detailed in [28], thus allowing to correlate MW measurements with generated traps.

The quantitative estimation made from the simple analytical model will be helpful to develop next-generation FeFETs with improved endurance.

Possible strategies to improve endurance of FeFETs, as also pointed out by other authors, include: (*i*) employment of high-κ oxides instead of SiO_2 to reduce field in the IL layer [30], [36]; (*ii*) reducing the charge mismatch between ferroelectric polarization and semiconductor charge by tailoring the HfO_2 properties [41]; and (*iii*) improvement of the quality of the IL layer by annealing or other processing treatments [42], [43]. In general, these strategies aim at lowering the electric field sustained by the IL layer to reduce its wear-out. We emphasize that the reliability challenges must be solved without degrading performance. For instance, although complete removal of IL may improve endurance [44] it may degrade channel mobility, and thereby compromise FET switching performance and/or ON/OFF ratio.

4. NBTI-FREE OPERATION IN NCFETs

Negative Bias Temperature Instability (NBTI) is a critical reliability issue in regular p-type MOSFETs that causes $\Delta V_{th} < 0$ (i.e., negative shift) over time due to hole trapping at the interface between gate oxide and semiconductor [45]. This happens also for NCFETs [1], but thanks to the stabilized NC effect the V_{th} can be effectively compensated and, under proper design constraints, eliminated [46].

In presence of interface traps, the overall charge that compensates the polarization at any time (neglecting other parasitic components) can be written as $Q(t) = Q_s(t)–Q_{IT}(t)$ (Q_s is the semiconductor charge, Q_{IT} is the interface trapped charge). $Q_{IT} > 0$ when traps capture holes, $Q_{IT} < 0$ when they capture electrons; hereon we assume only holes are trapped in pMOS hence $Q_{IT}(t) > 0$ for all t. Over time, holes get trapped so that $\Delta Q(t) = –\Delta Q_{IT}(t) < 0$ and hence $\Delta V_{th} < 0$ for the regular pMOS. In an NCFET however, $\Delta Q(t)$ causes the capacitance matching between $|C_{FE}|$ and C_{MOS} to evolve over time (or equivalently, over interface trapped charge) so that the voltage amplification factor (or equivalently body factor m) changes [46], [47]. In other

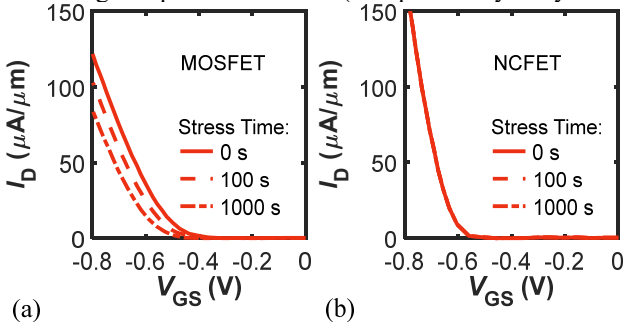

Figure 6. Simulated I_D-V_{GS} characteristics of the (a) MOSFET and (b) NCFET at different NBTI stress conditions (see legend). Proper NCFET design can lead to NBTI-free operation. Adapted from [46].

words, provided that the NC effect remains stable over time, the negative feedback action provided by the ferroelectric can compensate the ΔV_{th} or even suppress it. This is because the voltage drop on the ferroelectric (V_{FE}) is negative and hence ΔV_{FE} can be positive and compensate for the negative ΔV_{th} [46]. In fact it can be shown that [47]:

$$\Delta V_{th}(t) \approx -\Delta Q_{IT}(t)\left[\frac{\partial V_{FE}}{\partial Q} + \frac{\partial V_{ox}}{\partial Q}\right] = -\frac{\Delta Q_{IT}(t)}{C_{eq}}, \tag{6}$$

with $C_{eq}^{-1} = C_{FE}^{-1} + C_{ox}^{-1}$. If $C_{eq} < 0$ (as for the case of a NCFET), then Eq. (6) simply predicts that $\Delta V_{th} > 0$. The constraint that needs to be satisfied over time in order to guarantee self-regulation of NBTI is as follows [46]:

$$[Q(0)^3 - Q(t)^3] > [Q_{Vth,i}^3(0) - Q_{Vth,i}^3(t)], \tag{7}$$

where $t = 0$ is the pre-stress instant and $Q_{Vth,i}$ is the intrinsic pMOS charge at threshold condition [46]. Figure 6 shows the results of self-consistent numerical simulations in terms of I_D-V_{GS} curves for the p-type MOSFET and NCFET with same configuration (t_{FE} = 28 nm) at three different stress times (see legend). The simulation results in Figure 6 effectively show the ability of the NCFET to suppress NBTI-induced V_{th} shift thanks to the better capacitance matching condition achieved over stress time [46].

Achieving an optimum FE layer thickness to ensure NBTI-free operation can be challenging from a technological point of view (due to manufacturing constraints). However, even for relatively thin t_{FE} = 7 nm, simulations show NBTI degradation to be significantly reduced [46]. In other words, even if the FE thickness needs to be determined exclusively by process integration and capacitance matching constraints, it would still lead to beneficial NBTI reduction.

As pointed out in [48], due to the internal voltage amplification NCFETs would be more prone to interface trap generation than the corresponding MOSFETs (i.e., at the same node without the ferroelectric layer) if operated at the same supply voltage. On the other hand, at a given interface trap concentration (or equivalently, stress time) NCFETs have lower ΔV_{th} than MOSFETs

[48], as also explained previously. Hence, in practice NCFETs should be operated at lower supply voltage than their MOSFETs counterparts to slow down aging.

5. HOT ATOM DAMAGE (HAD)

In the preceding two sections, we have focused on interface/bulk defect generation at the Si/IL interface. The reliability of the FE layer itself could be a challenge. For example, Hot Atom Damage (HAD) is a reliability concern for FeFETs (although theoretically present also in NCFETs) that is inherent to the polarization switching mechanism [19], [20]. During switching, ferroelectric atoms across domain walls (transitioning from one polarization state to the other) might cause bond stretching beyond their critical breaking point causing damage [19]. This reliability concern is dynamic, in the sense that a DC signal would not involve periodic oscillations between energy minima in the energy landscape; hence, HAD manifests as AC stress [19]. The polarization overshoots occurring during transient switching lead to accumulation of broken bonds, and thus defects, resulting in increased gate leakage and degraded lifetime [19], [20].

Because NCFET do not require the application of high gate bias to switch and because the stabilized NC effect is inherently static, HAD is less relevant in this case [20]. Instead for FeFETs, HAD is a serious reliability concern limiting lifetime and thus endurance [19], [21].

The energy landscape corresponding to a switching event is schematically illustrated in Figure 7(a). When switching is triggered from equilibrium ($E = 0$) by applying a field larger than the coercive field (E_C), the polarization state is switched from one energy minima to the other, see Figure 7(a). If the transient is very rapid, an energy overshoot can be produced that can break atom bonds if the bond-breaking energy (E_B) is overcome [19], [21]. This effect in practice reduces device AC lifetime as shown in Figure 7(b). When a fast AC switching pulse is applied, lifetime (t_{HAD}) significantly reduces, see Figure 7(b). This lifetime reduction must be mitigated to avoid premature failure; this can be achieved by, for instance, increasing the pulse rise time (t_r) [19]. This is illustrated by the simulations in Figure 7(c), where polarization overshoots are reduced with increasing t_r. Simulations were carried out on a FE/DE structure by modeling the ferroelectric dynamics as that of a dipole oscillator by modifying Eq. (11) as follows [19], [20], [49]:

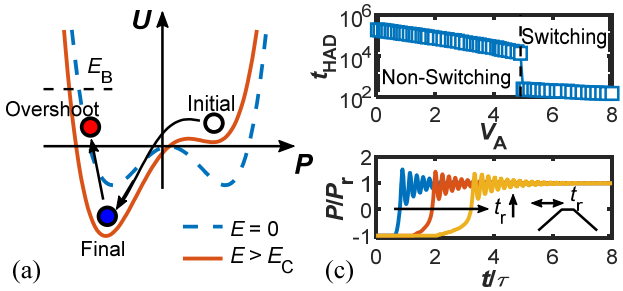

Figure 7. (a) Energy landscape at $E = 0$ and $E > E_C$ showing the switching event with transient overshoot approaching bond breaking energy (E_B). (b) Measured AC Lifetime (t_{HAD}) vs ac voltage amplitude V_A. t_{HAD} significantly reduces for switching conditions. (c) Simulated transient overshoots during polarization switching for different pulse rise time (t_r). Increasing t_r effectively reduces overshoots and increases lifetime. Simulation parameters are the same as those used in Figure 2. Adapted from [19], [21].

$$E = 2\alpha P + 4\beta^3 + 6\gamma P^5 + \rho\frac{\partial P}{\partial t} + l\frac{\partial^2 P}{\partial t^2}, \tag{8}$$

where l can be identified as a kinetic inductance (or inertia) of the ferroelectric [49]. In Figure 7(b), time was normalized to the time constant characterizing the decay of the oscillations $\tau = 2l/\rho$ [19].

Besides increasing t_r, other effective strategies to suppress transient overshoots and limit HAD involve increasing the oscillator time constant τ by either: (*i*) employing a series resistance (R_s), or (*ii*) increasing temperature to increase lattice scattering and thus ρ [19]. Although the afore mentioned strategies reduce HAD, they also increase the switching time, therefore in practice performance and reliability need to be traded-off according to the application requirements.

6. DISCUSSION AND CONCLUSIONS

Ferroelectric and negative capacitance FETs based on HfO_2 bring in additional reliability aspects compared to conventional MOSFETs that still need to be addressed/solved.

In addition to HAD discussed in Sec. 6, ferroelectric HfO_2 presents issues such as imprint (i.e., lateral rigid shift of P–E loop) [50], TDDB, wake-up and fatigue (i.e., increase and decrease of remnant polarization, P_r) [23], switching stochasticity [22], and ferroelectric phase non-uniformity [51]:

1) Imprint, in addition to depolarization field and leakage [5], cause polarization loss over time limiting retention [50].
2) TDDB leads to ultimate failure of the device and thus represents an upper bound to lifetime. From MOSFET theory, it is well-known that TDDB lifetime scales with area, as also experimentally verified on ferroelectric HfO_2 capacitors [52], [53]. Also, one must carefully analyze if increased lifetime associated with soft-breakdown [54]–[56] is still relevant for

NCFETs, where the leakage associated with the first breakdown may lead to significant shift in the threshold voltage. Additionally, the internal voltage amplification of NCFETs might reduce breakdown voltage compared to MOSFETs when operated at the same supply voltage [16].

3) Wake-up and fatigue (driven by defect formation mainly along grain boundaries) cause polarization de-pinning/pinning, respectively, and affect endurance characteristic of the ferroelectric [23]. Interestingly, as discussed in [39], endurance of FE-HfO_2 capacitors was higher than that of corresponding FeFETs realized with the same FE layer and geometry, pointing out to degradation of IL as the limiting factor to endurance [39], [40].
4) Switching is dominated by stochastic domain-wall nucleation causing variability issues especially in ultra-thin layers [22]. Variability is also enhanced by the non-uniformity of the ferroelectric phase across the HfO_2 layer [51].

Moreover, in addition to the endurance and NBTI issues discussed in Sec. 4 and 5, other MOSFET reliability challenges such as BTI, gate leakage, hot electron injection, self-heating, and radiation need to be addressed:

1) Bias Temperature Instability (BTI), i.e., V_{th} shift due to charge trapping, plays a role in FeFETs [30], [57] as well as NCFETs [46], [48]. V_{th}-shifts due to BTI can either cause fast, recoverable issues [30], [57] (i.e., causing instability) or permanent damage (related to trap generation) limiting reliability [28], [35], [40], [46].
2) Gate leakage limits endurance in FeFETs as it was found to correlate with IL degradation [39], whereas in NCFETs it can cause a de-stabilization of the NC effect at steady-state if MFMIS structure is employed [58].
3) Hot electron injection (HCI) from gate contact during negative voltage writing conditions was found to be the main endurance limiting factor in <5nm FE-HfO_2 FeFETs [59], due to the trapping of holes generated by the injected hot carriers [9], [59]. Because of their low-voltage operation, NCFET are likely less affected than FeFETs by HCI; however, this requires further investigation [1].
4) Self-heating (SH) is the device internal temperature rise due to power dissipation. In [60] it was shown that partial recovery of endurance degradation could be achieved in FeFETs by inducing SH through high current between the body and source/drain contacts. A simulation study showed that SH in NCFETs can be higher than that of MOSFETs due to the higher current at same supply voltage [61].
5) Ionizing radiation causes cumulative degradation of FeFET performance due to highly energetic electron/hole pairs that create new traps. In [62] it was verified that increased total ionizing dose reduces endurance potentially due to trap generation and hole trapping. Eq. (5) can be adapted to model radiation-induced *MW* closure due to trap generation in the gate stack. NCFETs may be more resilient than conventional MOSFETs to radiation as, shown in [63]. Similar to NBTI suppression, NCFETs are expected to have improved radiation hardness so long the degradation is primarily due interface trap generation. A recent study however highlights the importance of analyzing both interface and bulk trap generation self-consistently to quantify the dominant lifetime limiting mechanism [64].

In conclusion, our specific contribution in this work was focused on some of the most pressing challenges, such as trap generation (limiting FeFETs endurance), NBTI-free operation in NCFETs and HAD for both devices. We proposed an integrative theoretical framework based on Landau Theory to analyze the aforementioned reliability issues by means of either analytical models or self-consistent numerical simulations. The simple yet effective modeling approach proposed in this work allows gaining useful insights in the reliability/failure mechanisms of FeFETs/NCFETs as well as devising possible strategies to mitigate these issues. For instance, the proposed *MW* degradation analytical model can help interpreting the record endurance exceeding 10^{10} presented in [36], as the use of high-κ IL reduces the electric field and thus concentration of generated traps at given stress cycle. Nevertheless, given the diversity of the emerging doped high-k ferroelectric insulators and of the device configurations in which they are integrated, a large number of carefully designed experimental studies are required to systematically identify and classify the degradation mechanisms limiting reliability of FeFETs/NCFETs. In this sense, the theoretical framework proposed here is intended as a guide to design experiments as well as to interpret them.

7. METHODS: THEROETICAL FRAMEWORK

According to the phenomenological Landau Theory (LT), the energy of a system (U) near phase transition can be expressed as power-series expansion with respect to an order parameter (i.e., for FE, the polarization P) as follows [65]:

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - EP, \tag{9}$$

where α, β, γ are material-dependent parameters and E is the applied external electric field. The first parameter α depends on temperature ($\alpha = \alpha_0(T–T_0)$, where T_0 is the Curie temperature [65]) and at room temperature $\alpha<0$ for ferroelectrics. Under equilibrium (i.e., $E = 0$) the energy landscape resembles the one illustrated in Figure 8(a), with two-stable energy minima separated by an energy barrier.

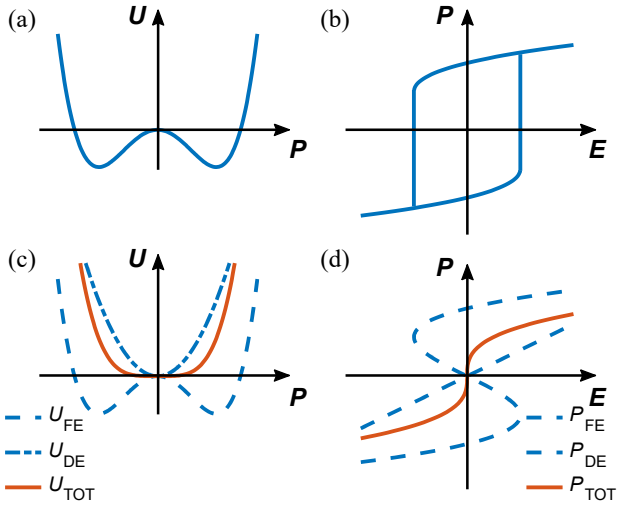

Figure 8. (a), (c) Energy landscape and (b), (d) corresponding P-E loop for the (a), (b) isolated FE and (c), (d) FE+DE system. In (c), (d) $t_{FE} = -t_{DE}/(2\alpha\varepsilon_{DE})$ so that $U_{TOT} = P_{TOT} = 0$ becomes accessible and negative capacitance can be harnessed.

This energy barrier is at the origin for the hysteresis in the *P–E* loop (typical of ferroelectrics) as the energy required to jump from one energy minima to the other depends on the history of the transition. The *P–E* relationship can be derived by applying Landau-Khalatnikov equation (LKE), that reads [2]:

$$\rho\frac{\partial P}{\partial t} + \frac{\partial U}{\partial P} = 0, \tag{10}$$

where ρ is also a material-dependent parameter. Combining Eqs. (9) and (10) yields:

$$E = 2\alpha P + 4\beta^3 + 6\gamma P^5 + \rho\frac{\partial P}{\partial t}, \tag{11}$$

which can be visualized in Figure 8(b) in the steady-state case, i.e., $\partial P/\partial t = 0$.

The point corresponding to ($U = P = 0$) is unstable for an isolated FE layer, as the energy is not minimized, giving rise to a sudden transition from one stable point to the other as the applied field is raised above $E_{C,LK}=E|_{(\partial P/\partial E\,=\,0)}$, see Figure 8(b). However, when placed in series with a conventional dielectric (DE) layer, the *total* energy of the system can be stabilized in the $U = P = 0$ point corresponding to the *negative capacitance* region [2]. Accordingly, Eq. (9) is modified as follows:

$$U_{TOT} = U_{FE} + U_{DE} = \left(\alpha + \frac{1}{2\varepsilon_{DE}}\right)P^2 + \beta P^4 + \gamma P^6 - EP, \tag{12}$$

where $\varepsilon_{DE} = \varepsilon_0\kappa_{DE}$ is the dielectric constant of the DE. For the time being we assume that $\varepsilon_{FE} = 0$ and that the polarization charge is completely compensated by the charge on the DE (we will discuss the case $\varepsilon_{FE} > 0$ in Section 3). For a system with energy U_{TOT} as expressed by Eq. (12), if the following condition is satisfied [2], [34], [66]:

$$t_{FE} < \frac{t_{DE}}{2|\alpha|\varepsilon_{DE}}, \tag{13}$$

where t_{FE} (t_{DE}) is the ferroelectric (dielectric) thickness, then the point $U_{TOT} = P_{TOT} = 0$ becomes stable (i.e., energy minimum) and the negative capacitance region can be accessed [67]. Eq. (12) is depicted in Figure 8(c) and the corresponding "S-shaped" *P–E* relationship is shown in Figure 8(d). Basically, Eq. (13) identifies (on first approximation) the design constraint for either hysteretic or stabilized NC operation. In Section 3 we will generalize Eq. (13) for the transistor case including the non-linear MOSFET capacitance, see Eq. (3).

The NC can be either a stabilized (DC) or transient effect [66]. In the first case, the depolarization field caused by the DE layer renders the $U = P = 0$ point stable, as discussed previously, and as such "small-signal" like, hysteresis-free amplification can occur [1], [66]. In the second case, instead, NC is a consequence of polarization switching, occurring when moving from one stable polarization state to another and as such leads to hysteresis and vanishes at steady-state [66], [68], [69]. Although stabilized NC effect in HfO_2-based NCFETs has not been yet unambiguously demonstrated [66], we will assume this to occur throughout this paper.

In general, the gate stack structure of FeFETs/NCFETs is the metal-ferroelectric-insulator-semiconductor (MFIS), optionally integrating a floating metal in between the ferroelectric and the insulator, i.e., MFMIS (this case is equivalent to consider an MFM capacitor in series with the gate metal of a regular MOSFET). MFIS and MFMIS structures are identical only under ideal

conditions, i.e., without leakage (that destabilizes the NC effect [58]) and without domain formation [34]. Thus, MFMIS in practice is useful for analysis purposes only, and MFIS should be the design of choice for realistic devices.

Landau theory discussed so far is phenomenological in the sense that it allows describing the macroscopic behavior of polarization across the whole layer, neglecting the microscopic details [65]. Thus, the model discussed so far represents a simplification of the actual behavior of the ferroelectric. More accurate descriptions need to take into account the multi-domain nature of polarization (i.e., non-uniformity across the ferroelectric) [70] as well as the stochasticity inherent to the switching dynamics [22], [71]. Moreover, polycrystallinity of the ferroelectric HfO_2 layer (i.e., containing both FE and DE grains) – giving rise to variability [51], [72] – needs also to be taken into account.

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DECLARATIONS

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