A Memory Window Expression to Evaluate the Endurance of Ferroelectric FETs

Nicolò Zagni,[1, a)] Paolo Pavan,[1] and Muhammad A. Alam[2]
[1)]*Department of Engineering "Enzo Ferrari", University of Modena and Reggio Emilia, Modena, 41125, Italy*
[2)]*School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, USA*

The recent discovery of ferroelectricity in HfO_2 has revived the interest into non-volatile memories based on ferroelectric transistors (FeFETs). Among their advantages stand out the low power consumption and the compatibility with existing CMOS process. On the other hand, issues related mainly to endurance still represent a challenge to the development of the technology. In this letter, we propose to exploit an analytical expression for the Memory Window (*MW*) as a simple yet effective characterization tool to evaluate endurance in FeFETs. *MW* is defined as the difference between threshold voltages occurring due to polarization switching. The analytical formulation of *MW* allows one to quickly estimate the generated trap concentration as a function of number of writing cycles (or time) without recurring to numerical simulations. With the aid of the analytical model, we find that for a specific set of program/erase pulse amplitude and duration, endurance has weak dependence on writing conditions. The characterization technique based on *MW* would allow the systematic comparison of the performance and endurance of next-generation FeFETs.

The first demonstration in the early 1960s of a thin-film ferroelectric transistor (FeFET) by Moll and Tarui[1] started the quest for realizing low-power and efficient Non-Volatile Memories (NVMs) based on this technology. After more than fifty years, the discovery of ferroelectricity in binary oxides such as HfO_2 and ZrO_2 revived the interest of the community in the FeFET technology[2–4]. FeFETs in fact, offer a wide range of improvements in terms of nonvolatility, scaling potential, read-write speed, and power dissipation with respect to DRAM, SRAM and Flash memory[2]. However, issues at device level limiting retention, and - mostly - endurance still need to be solved. In fact, while HfO_2-based FeFETs have reduced trapping and lower depolarization over coercive field ratio - leading to improved retention time with respect to older device generations based on PZT or SBT ferroelectrics[5] - endurance is still a major issue. Indeed, recent reports showed that endurance typical range is $\sim 10^4 - 10^6$ writing cycles[6,7]; this is far from meeting the International Roadmap for Devices and Systems (IRDS) requirements of 10^{12} cycles[8]. Nonetheless, the successful demonstration of a ultra-scaled CMOS-compatible FeFET would advance a broad range of applications, such as: *i)* Logic-In-Memory (LiM) circuits[9]; *ii)* artificial neural networks[10,11]; and *iii)* Ternary Content Addressable Memories (TCAMs)[9,11].

Thus, deployment of characterization tools that quantify and identify the limiting factors to endurance would facilitate the development of next-generation FeFETs[12]. In this letter, we propose to evaluate the endurance of FeFETs by using a simple characterization tool based on an analytical expression of the Memory Window (*MW*). The *MW* expression allows quantifying the impact of oxide and interface traps generated over time. In addition, from the *MW* expression it is possible to estimate the generated trap concentration during endurance tests without the need for numerical TCAD simulations. We find also that under specific assumptions regarding the program/erase pulse amplitude and duration endurance weakly depends on writing conditions.

The *MW* is expressed as the difference between the on- and off-threshold voltage ($V_{th,on}$, and $V_{th,off}$) that correspond to the right and left path of the FeFET $I_D - V_{GS}$ characteristics[3], respectively. These path differ because of polarization switching and represent the logic binary states "0" and "1" of the memory. The expressions for $V_{th,on}$, and $V_{th,off}$ used in this work are a generalization of the ones derived by Chen et al.[13] for a Metal-Ferroelectric-Insulator-Semiconductor (MFIS) stack. The *MW* is then simply written as $V_{th,on} - V_{th,off}$. The derivation is based on the electrostatic behavior of the FeFET described by the MOSFET surface potential equation (SPE)[13,14]:

$$V_{GS} - V_{FB} = V_{ins} + \psi_s \tag{1}$$

where V_{GS} is the applied gate-source bias, V_{FB} is the flatband voltage, V_{ins} is the insulator voltage (including both ferroelectric and oxide interface layer), and ψ_s is the surface potential. V_{ins} includes the contribution from the ferroelectric and oxide interlayer and is expressed as follows:

$$V_{ins} = Q_s \left(\frac{1}{C_{FE}} + \frac{1}{C_{ox}} \right), \tag{2}$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance (SiO_2 in this work) and C_{FE} is the ferroelectric capacitance. The latter can be written in a compact form by using the Landau-Devonshire (LD) theory[13,15]:

$$C_{FE} = \frac{1}{t_{FE}(2\alpha + 12\beta Q_s^2)} + \frac{\varepsilon_{FE}}{t_{FE}} \tag{3}$$

where Q_s is the semiconductor charge, α, β are the Landau parameters for the ferroelectric layer, ε_{FE} is the parameter accounting for the dielectric response of the ferroelectric layer[16,17], and t_{FE} is the ferroelectric thickness. The two terms

[a)]Was visiting scholar at the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA;
Corresponding Author: nicolo.zagni@unimore.it.

in Eq. (3) reflect the contributions to the displacement of the electric field (D) obtained from the spontaneous polarization and the applied electric field[16], i.e., $D = \varepsilon_{FE}E + P$. Incidentally, we mention that the LD formulation of C_{FE} is commonly employed to describe the operation of Negative Capacitance transistors (NCFETs) for logic[15] and other applications (such as bio-sensing[18]). However, it can be used also to model the operation of hysteretic FeFETs[13]. Thus, the approach based on the LD theory followed in this work can serve as a bridge between the NC- and Fe-FETs communities thanks to their common theoretical framework.

The closed-form expressions for $V_{th,on}$, $V_{th,off}$ and MW read as (see the Supplementary Material for the derivation):

$$V_{th,on} = V_{FB} + 2V_t \ln\left(\frac{2V_t}{|a|Q_0}\right) - 2V_t \tag{4}$$

$$V_{th,off} = V_{FB} + 2V_t \ln\left(\frac{Q_{sw}}{Q_0}\right) - V_{sw} \tag{5}$$

$$MW = 2V_t \ln\left(\frac{2V_t}{|a|Q_{sw}}\right) + (V_{sw} - 2V_t) \tag{6}$$

where $V_t = k_B T/q$ is the thermal voltage, k_B is the Boltzmann constant, T is the device temperature, q is the elementary charge, $a \equiv 2\alpha t_{FE}/(1 + 2\alpha\varepsilon_{FE}) + 1/C_{ox}$, $Q_0 = \sqrt{2\varepsilon_s k_B T n_i^2/N_a}$, ε_s is the semiconductor dielectric constant, n_i is the intrinsic carrier density, and N_a is the substrate doping density (for a p-type substrate in a NMOS device). V_{sw} is the V_{ins} at which switching from off- to on- occurs (Q_{sw} is the corresponding charge). V_{sw} and Q_{sw} are calculated following the procedure described in the Supplementary Material. Since $V_{sw} \propto t_{FE}$, and $MW \sim V_{sw} \propto t_{FE}$, Eq. (6) correctly anticipates the theoretical (and experimentally observed) linear thickness-dependence of the MW[4,14,19]. While the traditional Preisach model could also be used to describe the hysteretic polarization behavior[14], it does not allow to de-couple V_{FE} (ferroelectric voltage) from P[14,20] and thus requires a self-consistent, numerical analysis to obtain the results. Instead, relying on the LD theory allows to derive simple, closed-form expressions as (4)-(6) (and subsequent ones). More details regarding the derivation and approximations introduced as well as the applicability limits of the analytical model are given in the Supplementary Material.

Endurance is defined as the time taken (or total number of cycles) during repeated program/erase operations before the "0" and "1" states become indistinguishable. The main limiting factor to FeFETs endurance is the trap generation in the oxide interlayer between the ferroelectric and the semiconductor body[22]. This effect is the subject of investigation in this work. Other limitations to endurance of these devices are related to ferroelectric aging that might lead to additional V_{th}'s shifts, premature breakdown due to formation of percolation paths[23,24] and remnant polarization degradation[22]. A more detailed discussion on these effects is given in the Supplementary Material. We do not explicitly take into account the fast MW decay (due to depolarization fields and trapping/detrapping) because it is expected to mainly influence retention[5,22].

During stress tests to probe endurance, the high electric field in the gate stack accelerates trap generation. The electric field mainly concentrates on the oxide interlayer rather than in the ferroelectric because of its lower dielectric constant[20]. Thus, generation is assumed to only occur at the oxide/semiconductor interface and in the oxide itself. The effect of generated defects is modeled by adding to the right-hand side of Eq. (1) these additional terms[25]:

$$V_{ot} \equiv -\frac{q\Delta N_{ot}}{C_{eq}} \quad V_{it} \equiv \frac{q\Delta D_{it}}{C_{eq}}(\psi_s - \phi_b), \tag{7}$$

where ΔN_{ot} is the generated trap concentration in the oxide interface layer (cm^{-2}), ΔD_{it} is the generated interface trap density of states ($\mathrm{cm}^{-2}\mathrm{eV}^{-1}$), and ϕ_b is the body potential ($C_{eq}^{-1} = C_{FE}^{-1} + C_{ox}^{-1}$). We assume that the charge neutrality level for the interface traps is located at Si mid-gap[25]. Stress is induced by positive and negative pulses applied on the gate to erase and program the FeFET, respectively. Hence, $V_{th,on}$ tends to decrease and $V_{th,off}$ to increase[21]. The concentration of generated defects during writing of the memory is in general different depending on the sign of the writing pulse, therefore the shifts in $V_{th,on}$ and $V_{th,off}$ are not symmetric. This is reflected in the different symbols used to indicate the generated defects during program and erase cycles, namely, $\Delta N_{ot,P/E}$ and $\Delta D_{it,P/E}$ for oxide and interface traps, respectively.

The degraded $V_{th,on}$, $V_{th_o ff}$, and MW expressions are modified by taking into account the additional potential drops due to defects expressed in Eq. (7) (see the Supplementary Material for the derivation). The V_{th}'s and MW variation is expressed as follows:

$$\Delta V_{th,on} = 2V_t \ln\left(1 + \frac{q\Delta D_{it,P}}{C_{eq}}\right) \times \left(1 + \frac{q\Delta D_{it,P}}{C_{eq}}\right) - \frac{q}{C_{eq}} \times \left\{\Delta N_{ot,P} - \Delta D_{it,P}\left[2V_t \ln\left(\frac{2V_t}{|a|Q_0}\right) - 2V_t - \phi_b\right]\right\} \tag{8a}$$

$$\Delta V_{th,off} = -\frac{q}{C_{eq}}\left\{\Delta N_{ot,E} - \Delta D_{it,E}\left[2V_t \ln\left(\frac{Q_{sw}}{Q_0}\right) - \phi_b\right]\right\} \tag{8b}$$

$$\Delta MW = 2V_t \ln\left(1 + \frac{q\Delta D_{it,P}}{C_{eq}}\right) \times \left(1 + \frac{q\Delta D_{it,P}}{C_{eq}}\right) - \frac{q}{C_{eq}}\left\{(\Delta N_{ot,P} - \Delta N_{ot,E}) - 2V_t\Delta D_{it,P}\left[\ln\left(\frac{2V_t}{|a|Q_0}\right) - 1\right] + 2V_t\Delta D_{it,E}\ln\left(\frac{Q_{sw}}{Q_0}\right) + (\Delta D_{it,P} - \Delta D_{it,E})\phi_b\right\}. \tag{8c}$$

To assess the accuracy of the above expressions, we compared the analytical results with experimental data of endurance tests from Ref. 21. The results in terms of $\Delta V_{th,on}$ and $\Delta V_{th,off}$ for three different values of program/erase pulse amplitude, $|V_{P/E}|$ are shown in Fig. 1 [$|V_{P/E}| = 4.2\,\mathrm{V}$ (a), $4.85\,\mathrm{V}$ (b), and $5.5\,\mathrm{V}$ (c)]. The $\alpha = -3 \times 10^9\,\mathrm{m/F}$, $\beta = 2 \times 10^{11}\,\mathrm{m^5/F/C^2}$, $\varepsilon_{FE} = 8\varepsilon_0$ were set to match the experimental data trends. $t_{FE} = 10\,\mathrm{nm}$ and $t_{ox} = 3\,\mathrm{nm}$. The duration of both program and erase pulse for each $|V_{P/E}|$ is $t_{P/E} = 100\,\mathrm{ns}$, thus the time

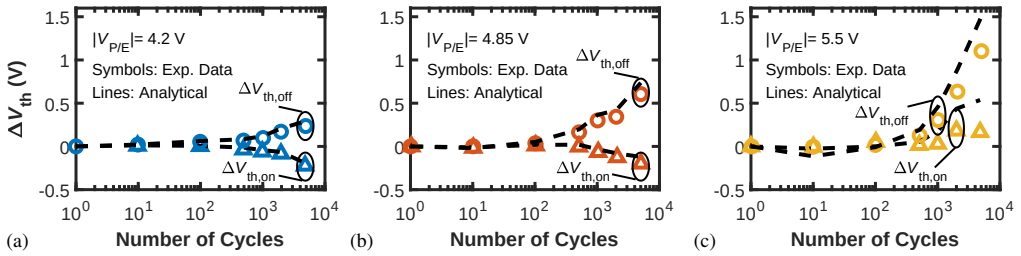

FIG. 1. Calculated (dashed lines) and experimental data (symbols, taken from Ref.21) $\Delta V_{th,on}$ and $\Delta V_{th,off}$ vs program/erase cycle number. The different panels show different program/erase pulse amplitude: (a) $|V_{P/E}| = 4.2\,\mathrm{V}$, (b) $|V_{P/E}| = 4.85\,\mathrm{V}$, and (c) $|V_{P/E}| = 5.5\,\mathrm{V}$, respectively.

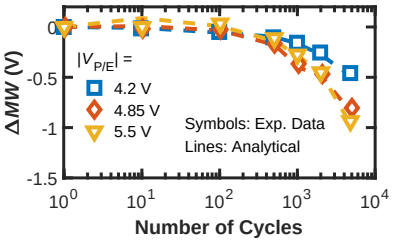

FIG. 2. Calculated (dashed lines) and experimental data (symbols, taken from Ref.21) ΔMW vs program/erase cycle number.

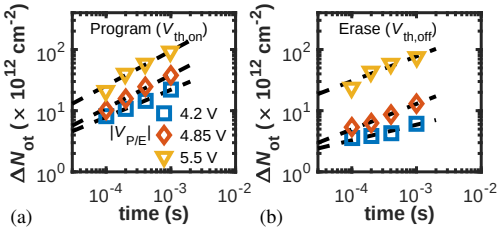

FIG. 3. Generated oxide traps, ΔN_{ot}, vs program/erase time for different $|V_{P/E}|$ (see legend) determining (a) $V_{th,on}$ and (b) $V_{th,off}$ degradation. Black dashed lines are the fitting of experimental data (symbols, from Ref. 21) with Eq. (10).

it takes for a single writing cycle is $t_{cycle} = 200\,\mathrm{ns}$[21]. The variation in $V_{th,on}$ and $V_{th,off}$ is in turn reflected to the MW, as shown in Fig. 2 for the same $|V_{P/E}|$ values of Fig. 1. Because degradation primarily occurs in the insulator layer, the trend of the degraded V_{th}'s and MW is fully captured by V_{ot} and V_{it} only. From this observation, simplified $\Delta V_{th,on}$, $\Delta V_{th,off}$ and ΔMW expressions can be obtained, as reported in the Supplementary Material. The good agreement between analytical and experimental results in Figs. 1 and 2 was obtained by extracting the generated oxide and interface trap concentrations from $\Delta V_{th,on}$ and $\Delta V_{th,off}$ data in[21] following the approach described in[26]. That is, N_{ot} and D_{it} were extracted by separating the threshold voltage shifts due to oxide (ΔV_{mg}) and interface traps (ΔV_{it}) separately. The former is obtained from the mid-gap voltage, V_{mg}, that correlates with N_{ot}-induced V_{th} drifts as at $V_G = V_{mg} \Rightarrow \psi_s = \phi_b$ and $\Delta V_{it} = 0$, see Eq. (7); the latter is obtained by letting $\Delta V_{it} = \Delta V_{th} - \Delta V_{ot}$[21,26]. To summarize, Eq. (8a)-Eq. (8c) directly connect the FeFET parameters to the stress-dependent oxide and interface trap generation. As such, Eq. (8c) represents the proposed MW-based characterization tool for extracting oxide and interface defects. This could serve either as an alternative to traditional techniques, or as a stand-alone method to characterize defect densities under a variety of stress conditions. For instance, notice that when only N_{ot} generation affects MW degradation then it is possible to estimate the *net* generated traps from the simplified $\Delta MW'$ expression found in the Supplementary Material:

$$\Delta N_{ot,net} \equiv \Delta N_{ot,P} - \Delta N_{ot,E} \approx -\Delta MW' \frac{C_{eq}}{q} \tag{9}$$

This expression allows to simply and directly correlate MW measurements with generated traps. In the following we show that the endurance extrapolated from the equations derived previously is weakly influenced by the writing conditions (in terms of $|V_{P/E}|$ and $t_{P/E}$). With the N_{ot} and D_{it} data extracted from Fig. 2, it is possible to extrapolate the generated trap concentration for an arbitrary number of writing cycles. For simplicity and clarity of presentation, we assume that the MW degradation is induced by oxide traps only (as supported by the experimental data from 21) and neglect the generation of interface traps. The generated oxide trap density, N_{ot} is shown in Fig. 3(a), (b) for both program and erase operation that set $V_{th,on}$ and $V_{th,off}$, respectively. By fitting the experimental data in Fig. 3 it is found that generated oxide trap concentration follows a power law with respect to writing time (with $t_{cycle} = 200\,\mathrm{ns}$):

$$\Delta N_{ot} \sim N_0 \times (t_{cycle})^{\beta_s}. \tag{10}$$

The values of N_0 and β_s coefficients are collected in Table I for different writing conditions. Exponent β_s is in the range

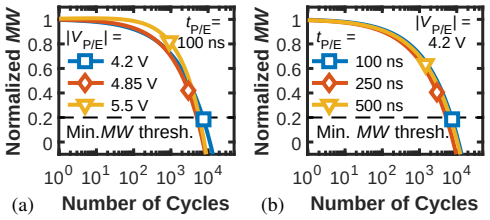

FIG. 4. Normalized MW degradation calculated from $\Delta MW'$ with only the contribution of ΔN_{ot} extrapolated from Fig. 3. (a) and (b) show the dependence for different $|V_{P/E}|$ and $t_{P/E}$ values, respectively. An arbitrary minimum MW threshold defines endurance.

of $0.3-0.5$, which might be a signature of enhanced TDDB due to repeated cycling[27].

The extrapolated MW degradation obtained by using the predicted ΔN_{ot} from the generation model is shown in Fig. 4(a), (b) for different $V_{P/E}$ and $t_{P/E}$ values, respectively. Note that MW values are normalized to the respective initial value for a fair comparison with different writing conditions. The FeFET is considered to fail to retain its memory operation after reaching the arbitrary threshold set as the 20% of the initial MW, see Fig. 4. That is, endurance is defined as the number of cycles at which MW reaches 20% of its initial value. Interestingly, notice from Fig. 4(a) that $|V_{P/E}|$ increment does not degrade endurance significantly (at least for the range of values as in Ref. 21). This is because higher $|V_{P/E}|$ leads to higher initial MW[4] but also higher ΔN_{ot}, see Fig. 3. Similarly, Fig. 4(b) shows that increasing the pulse duration negligibly influences endurance. Note that in this case it was assumed that $t_{P/E}$ increase leads to the same increase in MW and initial N_{ot} to that caused by $V_{P/E}$. This was done for the specific purpose of illustrating that if both MW and initial N_{ot} increase with program conditions, then the combined effect leads to negligible variation in endurance. However, if the assumption regarding MW and N_{ot} increase with $V_{P/E}$ (or $t_{P/E}$) is not satisfied, then the endurance limit will be affected by the writing conditions.

The model can also predict the endurance improvement obtained if the generated trap are decreased, either by improving the SiO_2/Si interface quality or by reducing the field in the oxide layer. For instance, if N_0 is decreased by one order of magnitude (and assuming every other parameter constant) then endurance can be extended to 10^6 cycles.

Endurance improvements where observed also in experiments employing either: i) unipolar stress pulses instead of conventional, bipolar ones[22]; or ii) large-area samples with improved interface quality and low gate leakage[28]. These results can be predicted by the developed analytical model, provided that adequate degradation model (i.e., by choosing proper N_0 and β_s in Table I) is employed.

In this letter, we evaluated the endurance of FeFETs by using an analytical expression of the Memory Window, MW, for the conventional MFIS structure. The MW expression takes into account the contribution from generated interface and oxide traps and was validated against experimental data. We find that: (*i*) MW can be used to extract oxide and interface traps being generated during endurance tests, see Eq. (9); (*ii*) the generation trend follows a power-law with time exponent $\sim 0.3-0.5$, see Eq. (10); and (*iii*) under specific assumptions, the endurance limit is essentially independent of writing conditions, see Fig. 4. The considerations drawn from the simple analytical formulation can be helpful to develop next-generation FeFET with improved endurance.

TABLE I. Coefficients of the power law in Eq. (10).

	Program ($V_{th,on}$)		**Erase ($V_{th,off}$)**	
$V_{P/E}$ (V)	N_0 (cm^{-2})	β_s	N_0 (cm^{-2})	β_s
4.2	9.6×10^{13}	0.45	4.6×10^{12}	0.25
4.85	3.28×10^{14}	0.54	3.1×10^{13}	0.41
5.5	9.5×10^{14}	0.54	1.7×10^{14}	0.41

SUPPLEMENTARY MATERIAL

See supplementary material for: (*i*) the detailed derivation of the analytical expressions; (*ii*) the design constraints to ensure hysteretic operation; (*iii*) the applicability limits of the analytical approach; and (*iv*) the limiting factors to endurance related to ferroelectric aging.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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