The Effects of Carbon on the Bidirectional Threshold Voltage Instabilities Induced by Negative Gate Bias Stress in GaN MIS-HEMTs

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ABSTRACT

In this paper, numerical device simulations are used to point out the possible contributions of Carbon doping to the threshold voltage instabilities induced by negative gate bias stress in AlGaN/GaN Metal Insulator Semiconductor High Electron Mobility Transistors (MIS-HEMTs). It is suggested that Carbon can have a role in both negative and positive threshold voltage shifts, as a result of the changes in the total negative charge stored in the Carbon-related acceptor traps in the GaN buffer as well as the attraction of Carbon-related free holes to the device surface and their capture into interface traps or recombination with gate-injected electrons. For a proper device optimization of Carbon-doped MIS-HEMTs, it is therefore important to take these mechanisms into account, in addition to those related to defects in the gate dielectric volume and interface which are conventionally held responsible for threshold voltage instabilities.

KEYWORDS

GaN Power Devices; Threshold Voltage Instability; Negative Gate Bias Stress; NBTI; Carbon Doping.

1. INTRODUCTION

GaN technology has eventually found its way to the power electronics market [1, 2], thanks to the lower total losses at higher breakdown voltage and higher switching frequency allowed by GaN-based transistors compared to Si power devices [3]. While normally-off devices, either based on the junction-gated High-Electron Mobility Transistor (HEMT) (aka p-GaN HEMT) or the fully recessed gate Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) concepts are intensively being developed at both research and industry level [1, 2], the two-chip cascode connection of a low-voltage Si MOSFET with a high-voltage, normally-on AlGaN/GaN Metal Insulator Semiconductor High Electron Mobility Transistor (MIS-HEMT) still represents a commonly adopted solution mainly for its compatibility with Si drivers [1]. Concerning the substrate material for the GaN device, a large-area Si wafer is the solution of choice for cost competitiveness [1, 2].

Given the insulated-gate structure of the MIS-HEMT, threshold-voltage (V_T) stability is a major concern critically impacting yield [4]. For normally-on devices with negative threshold voltages of several volts, V_T stability after the application of a large and negative gate bias is, in particular, a key aspect that needs careful evaluation during technology development. Assessing the V_T stability under negative gate bias is important also for normally-off devices, as negative gate bias can be applied to prevent false turn-on and ensure safe operation against the voltage spike on the gate [5]. These considerations have actually been the rationale for several recent research works on both normally-on MIS-HEMT and fully-recessed MOSFETs [5–13]. These works can be divided into three categories depending on the sign of the observed V_T shifts: 1) works showing a negative V_T shift (i.e. V_T becoming more negative) [6–8], 2) those illustrating a positive V_T shift (i.e. V_T becoming less negative) [5, 9–11], 3) the ones demonstrating V_T shifts of both sign, depending on device type or stress conditions [12, 13].

In the above published works, the physical mechanism that is held responsible for the negative V_T shifts is: A) electron emission from interface and/or border traps [6, 7,

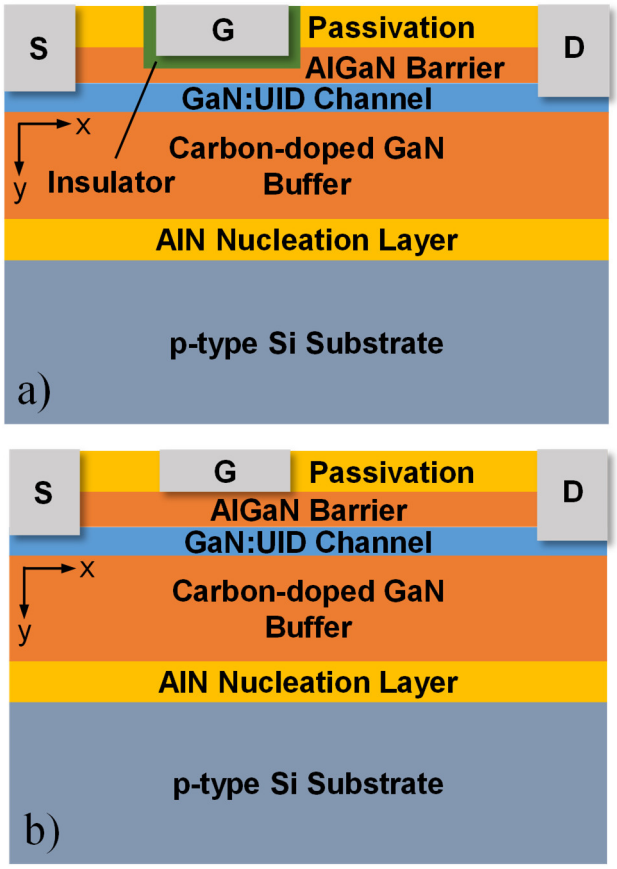

Figure 1. Cross-section of the simulated (**a**) MIS-HEMT and (**b**) HEMT.

12]; B) the decrease in the negative charge associated to C-related acceptor traps (C_N states) [8]. Positive V_T shifts are instead attributed to: C) electron injection from the gate and consequent electron capture into traps in the gate dielectric [10, 12]; D) hole-induced defect generation in the gate insulator [5, 9, 11] or interface-state generation [13]; E) Zener electron trapping into GaN traps localized under the gate edges [13].

In GaN power devices, Carbon (C) is widely adopted as compensation doping to suppress the unintentional conductivity in the GaN buffer and transition layers underlying the MIS-HEMT channel and to avoid premature breakdown related to source-to-drain punch-through [1, 14, 15]. The possible contributions of C doping to V_T instabilities are however generally disregarded with the exception of [8], despite (i) C related acceptor traps are of course not only present in the gate-drain access region (where they are held responsible for dynamic on-resistance, R_{ON}, degradation after off-state stress [16, 17]) but also under the gate (where they could impact V_T stability after negative gate bias stress), (ii) C-doped GaN is a weakly p-type semiconductor [16] and, in response to large and negative gate voltages, free holes can in principle drift to the surface and accumulate/recombine under the gate at the dielectric/barrier interface.

The aim of this paper is to investigate the possible role(s) played by C doping within the complex picture of negative gate bias V_T instabilities in AlGaN/GaN MIS-HEMTs. This has been pursued by means of device simulations, allowing the effects of C doping to be isolated from mechanisms A)-E) above, that however remain likely to play a role and whose impact depends on the specific device and the sign of the V_T shift observed experimentally.

The paper is organized as follows. In Section 2, the modeling framework is illustrated, including analyzed device structures and relevant physical models. Results are shown and discussed in Section 3. Conclusions are eventually drawn in Section 4.

2. MODELING FRAMEWORK

The two-dimensional (2D) numerical device simulations were carried out with the SDevice simulator (Synopsys Inc.) [18]. The analyzed structures are sketched in Fig. 1(a) and (b), resembling a typical power AlGaN/GaN MIS-HEMT and AlGaN/GaN Schottky-gate HEMT, respectively. While the focus of this paper is on AlGaN/GaN MIS-HEMTs for power switching applications, an AlGaN/GaN HEMT sharing the same epitaxial structure is also simulated and adopted as a useful, comparison case. What we are proposing here is a "simulated experiment", allowing us to decouple V_T instability effects related to Carbon from those connected to the gate dielectric. This will be done by considering the latter completely ideal or affected by defects and leakage currents and by even removing it so as to obtain a Schottky gate HEMT with the same epitaxy as the MIS-HEMT. Both structures have a grounded, p-type Si substrate, a C-doped GaN buffer (1.5 µm), an unintentionally doped (UID) GaN channel (150 nm), an $Al_{0.25}Ga_{0.75}N$ barrier (25 nm) and a Si_3N_4 passivation layer over the two access regions (150 nm). The MIS-HEMT features also a gate dielectric Al_2O_3 layer (15 nm) that is added to the structure after partially recessing the barrier and leaving 4 nm of residual AlGaN under the gate.

Charge transport was modelled by means of the drift-diffusion model. Electron mobility in the undoped and doped GaN layers were set to 1800 $cm^2/V{\cdot}s$ [19] and 900 $cm^2/V{\cdot}s$ [20], respectively. The latter value was taken as representative of a highly compensated GaN layer [20]. For easier simulation convergence, a silicon-like, monotonic velocity-field curve was assumed, with an electron saturation velocity of $1.5x10^7$ cm/s [19]. Table 1 collects the most relevant geometrical and model parameters of the simulated structures. Hole mobility and saturation velocity were left to their default values. All other material-specific parameters, including mobilities in materials other than GaN, dielectric constants, SRH and Auger recombination parameters, were left to the simulator's default values for the respective material. Impact ionization and self-heating were neglected. Piezoelectric polarization was included by using the default strain model of the simulator. Note that at the passivation/barrier and gate insulator/barrier interfaces the polarization model was deactivated. This approach is equivalent to assume that the polarization charge is completely compensated by a positive fixed surface charge [21].

As far as the trap model is concerned, a fully dynamic approach was adopted, with one SRH trap-balance equation

Tab. 1. Geometrical and model parameters of the simulated MIS-HEMT.

Geometrical Parameters (μm)		Model Parameters	
Si_3N_4 Passivation Thickness	0.15	2DEG Low-field mobility μ_n ($cm^2/V{\cdot}s$)	1800
Al_2O_3 Gate Insulator Thickness	0.015	Buffer Low-field mobility μ_n ($cm^2/V{\cdot}s$)	900
AlGaN Barrier Thickness	0.025	Saturation velocity v_{sat} (cm/s)	$1.5x10^7$
Residual Barrier Thickness (Under the Gate)	0.004	Al molar fraction x ($Al_xGa_{1-x}N$)	0.25
GaN:UID Channel Thickness	0.150	UID Doping (cm^{-3})	$1x10^{15}$
GaN:C Buffer Thickness	1.5	Deep Acceptor Conc. $N_{C,A}$ (cm^{-3})	$8x10^{17}$
Gate-to-Source Length L_{GS}	1	Deep Acceptor Level $E_{C,A} - E_V$ (eV)	0.9
Gate-to-Drain Length L_{GD}	10	Deep Donor Conc. $N_{C,D}$ (cm^{-3})	$4x10^{17}$
Gate Length L_G	0.7	Deep Donor Level $E_C - E_{C,D}$ (eV)	0.11

for each distinct trap level, describing the dynamics of trap occupation without any quasi-static approximation.

C doping in the GaN buffer was modelled by considering a dominant deep acceptor trap at 0.9 eV above the valence-band edge and a shallow donor trap at 0.11 eV below the conduction-band edge [22]. Adopted concentrations were 8×10^{17} cm^{-3} and 4×10^{17} cm^{-3} for C-related acceptors and donors, respectively, corresponding to an effective acceptor density of 4×10^{17} cm^{-3}. The adopted C-doping model based on discrete point defects can lose validity for C doping concentrations larger than 10^{19} cm^{-3}, for which a dominant defect band behaviour is more appropriate [23].

For the case of the MIS-HEMT, Fig. 1(a), the Al_2O_3/AlGaN interface will either be considered with no interface traps (i.e., surface states), or characterized by a density-of-interface-trap (D_{IT}) distribution consisting of donor-like states with a density of 1×10^{12} cm^{-2} eV^{-1} uniformly distributed across the AlGaN bandgap [24, 25]. Despite the assumed D_{IT} is simplified, it allows us to point out the possible interplay between interface traps and holes generated by C doping and attracted to the surface by the negative gate bias. Besides C-related traps and D_{IT}, no other traps were included, while in all nitride layers an n-type unintentional doping density of $1x10^{15}$ cm^{-3} was assumed.

When specified, the gate dielectric was modelled as a conductive insulator characterized by Ohmic transport and boundary conditions (imposed at the dielectric/semiconductor interfaces). This way, the current flow in the insulator is limited by its bulk resistivity only (set to 10^{11} Ω.cm) [18]. Otherwise, it was assumed to be an ideal insulator, with no gate leakage current flow. Although the adopted leaky dielectric model is a simplification, a more accurate description of dielectric transport mechanisms like that proposed in [26] leads to similar or larger gate leakage magnitude to that computed with the leaky dielectric model ($\approx$ 10^{-5} A/cm^2) for the gate stress voltages under consideration.

In the Schottky-gate HEMT, gate current was modelled by the thermionic- and field-emission mechanisms. The field emission component is calculated self-consistently by the simulator through a nonlocal tunnelling model based on the WKB approximation [16].

The above C doping model was adopted since it allowed us to reproduce current-collapse and breakdown effects in different GaN power HEMTs yielding an acceptable agreement with experimental results [27–33]. The key feature of this model is that dominant, deep, acceptor-type, hole traps are partially compensated by shallow, donor-type, electron traps. The actual energy position of donor traps, if sufficiently shallow, has little influence on simulation results. C-related donors could actually be moved even closer to E_C or be modelled as completely ionized dopants [34], in agreement with recent hybrid-functional Density Functional Theory (DFT) calculations [35, 36], without significant changes on simulation results. On the other hand, assuming that only acceptor levels are introduced with concentrations in the order of the nominal C density (10^{18}-10^{19} cm^{-3}) resulted in all our previous works in a very large overestimation of current-collapse effects [27–30]. An experimental indication that C doping introduces also donor levels (besides dominant acceptor ones) can be found in [37]. The capability of the acceptor-donor model for C doping to reproduce source-drain leakage currents and off-state breakdown is demonstrated in [38].

Table 2. Simulated devices for the different cases in Figures 2-6.

Case	Device
I	MIS-HEMT with Ideal Insulator and without D_{IT}
II	MIS-HEMT with Ideal Insulator but with D_{IT}
III	MIS-HEMT with Conductive Insulator and D_{IT}
IV	HEMT

3. RESULTS AND DISCUSSION

Simulated drain-current per 1-mm device width (I_D) vs gate-source-voltage (V_{GS}) characteristics at a drain-source voltage (V_{DS}) of 0.5 V of "fresh" and "stressed" devices are shown in Figure 2(a)-(d) for the following four cases: (I) the MIS-HEMT with ideal gate dielectric and without D_{IT}, (II) the MIS-HEMT with ideal gate dielectric but with D_{IT}, (III) the MIS-HEMT with both conductive gate dielectric and D_{IT}, (IV) the Schottky-gate HEMT. The four different cases are labelled I-IV and are collected in Tab. 2 for easier reference to the readers. Note that "Fresh" device here means that the simulation of the transfer curve was carried out starting from a (V_{GS}, V_{DS}) = (0 V, 0 V) equilibrium bias point by applying short V_{DS} and V_{GS} sweeps. "Stressed" device means that the same simulation was carried out (with the same short sweep times) immediately after application of a 100-s negative gate

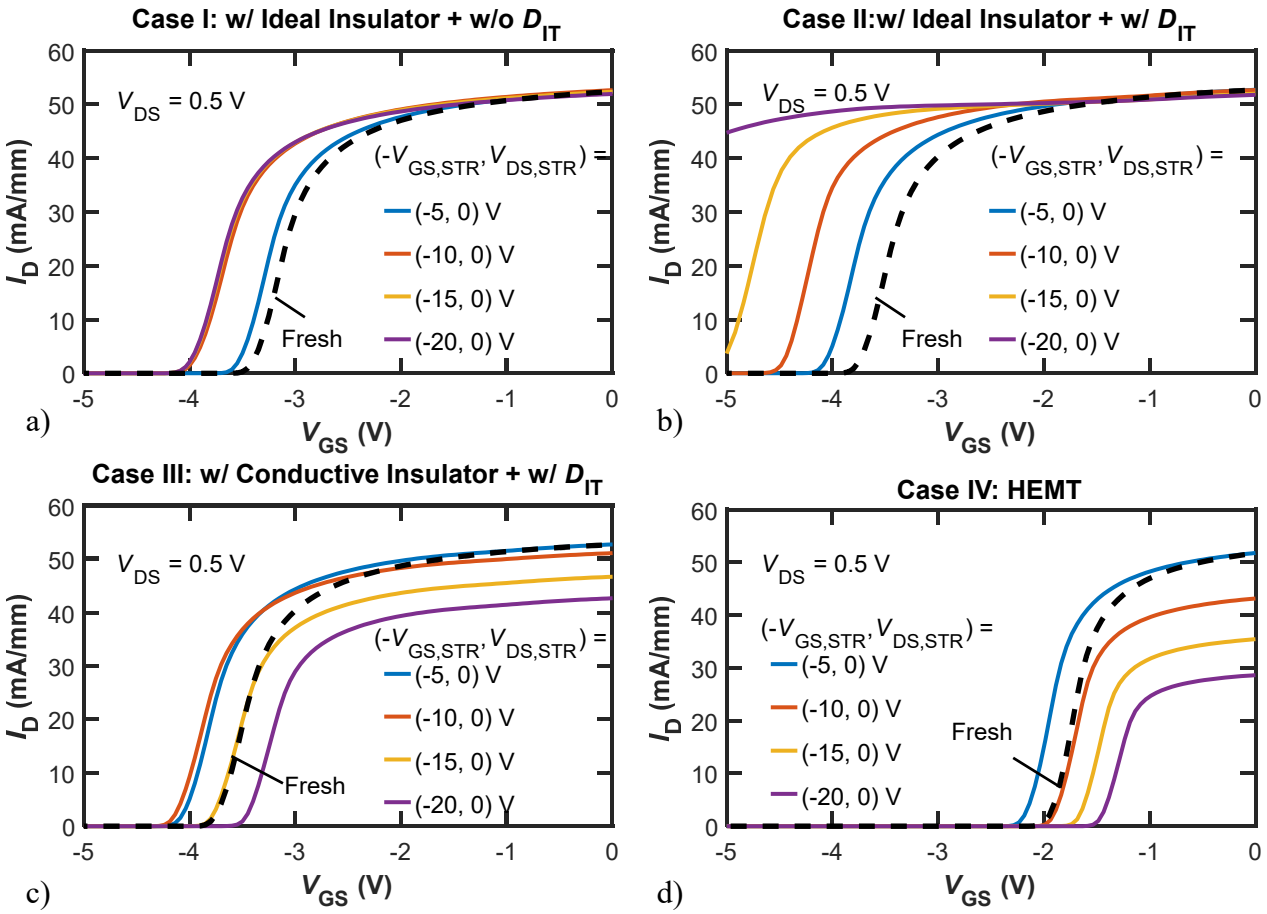

Figure 2. Simulated drain-current per 1-mm device width (I_D) vs gate-source-voltage (V_{GS}) characteristics at a drain-source voltage (V_{DS}) of 0.5 V of "fresh" and "stressed" devices (for $V_{DS,STR}$ = 0 V and different $V_{GS,STR}$ values) for Case I (a), Case II (b), Case III (c), and Case IV (d). Cases I-IV are defined in the heading of each panel (see also Tab. 2).

bias stress at (V_{GS}, V_{DS}) = (-$V_{GS,STR}$, 0 V) with $V_{GS,STR}$ values ranging from 5 to 20 V. Stress conditions were chosen to reproduce conventional setup used to analyse threshold voltage instabilities under negative gate bias stress and to compare to other reports in the literature [6, 7, 13].

More precisely, characterization is performed with a double 10-µs V_{GS}, V_{DS} sweep to "immediately" take the device to starting measurement conditions (i.e., V_{DS}=0.5 V and V_{GS}=-5V), followed by a 1-ms V_{GS} sweep to obtain the transfer curves shown in Fig. 2, emulating the "benign" characterization step that is typically adopted to monitor the evolution of degradation effects during stress experiments. These very short voltage sweeps were adopted to prevent the occupation state of C related traps from changing significantly. The V_T shifts (ΔV_T) extracted from I_D-V_{GS} curves shown in Fig. 2(a)-(d) are plotted against the stress gate bias (-$V_{GS,STR}$) in Fig. 3. In all cases V_T was defined as the V_{GS} voltage at which the normalized I_D is 1 mA/mm.

As it can be noted in Fig. 2(a) and 3, in Case I, the effect of the negative gate bias stress is a negative V_T shift for all $V_{GS,STR}$ values considered. Increasing $V_{GS,STR}$ leads to a larger shift up to $V_{GS,STR}$ = 10 V, while a very small additional shift is induced by further increasing $V_{GS,STR}$. This effect is present in our simulations despite the absence of interface/border traps at the dielectric/barrier interface and can be considered as the *contribution of C-related traps to the negative V_T shift*. In Case II, D_{IT} is added to the simulated device, yielding a

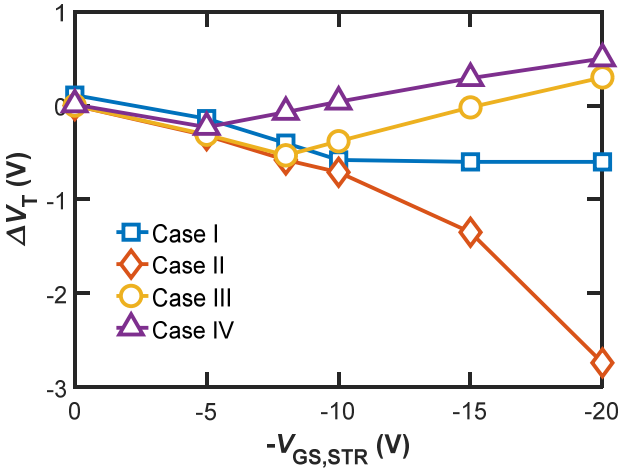

Figure 3. Threshold-voltage shifts (ΔV_T) vs gate stress bias (-$V_{GS,STR}$) for Cases I-IV as defined in Tab. 2.

larger negative V_T shift compared to Case I for the same $V_{GS,STR}$. In this case, the negative V_T shift significantly increases at increasing $V_{GS,STR}$ over the entire $V_{GS,STR}$ range considered. The *extra negative V_T shift compared to Case I can be attributed to the D_{IT}*. A bidirectional V_T instability is instead present in Case III, with V_T shifting negatively for $V_{GS,STR}$ values up to 10 V, going back about to the "fresh" value for $V_{GS,STR}$= 15 V, and eventually exceeding the initial

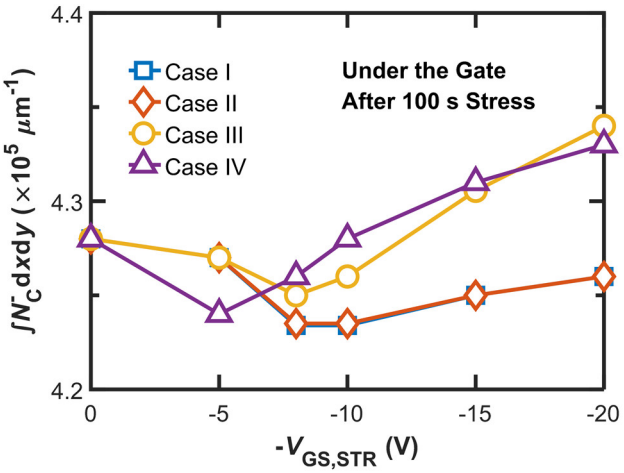

Figure 4. Gate stress bias ($-V_{GS,STR}$) dependence of the 2D integral of the negatively ionized C-related acceptor concentration (N_C^-). The integral is extended to the device region under the gate footprint. Cases I-IV are defined in Tab. 2.

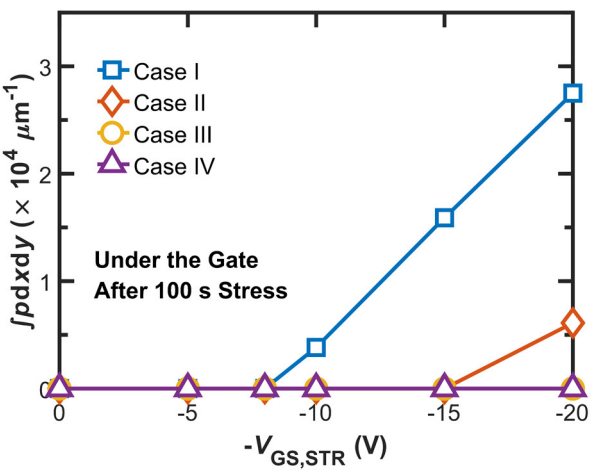

Figure 5. Gate stress bias ($-V_{GS,STR}$) dependence of the 2D integral of the free hole density (p). The integral is extended to the device region under the gate footprint. Cases I-IV are defined in Tab. 2.

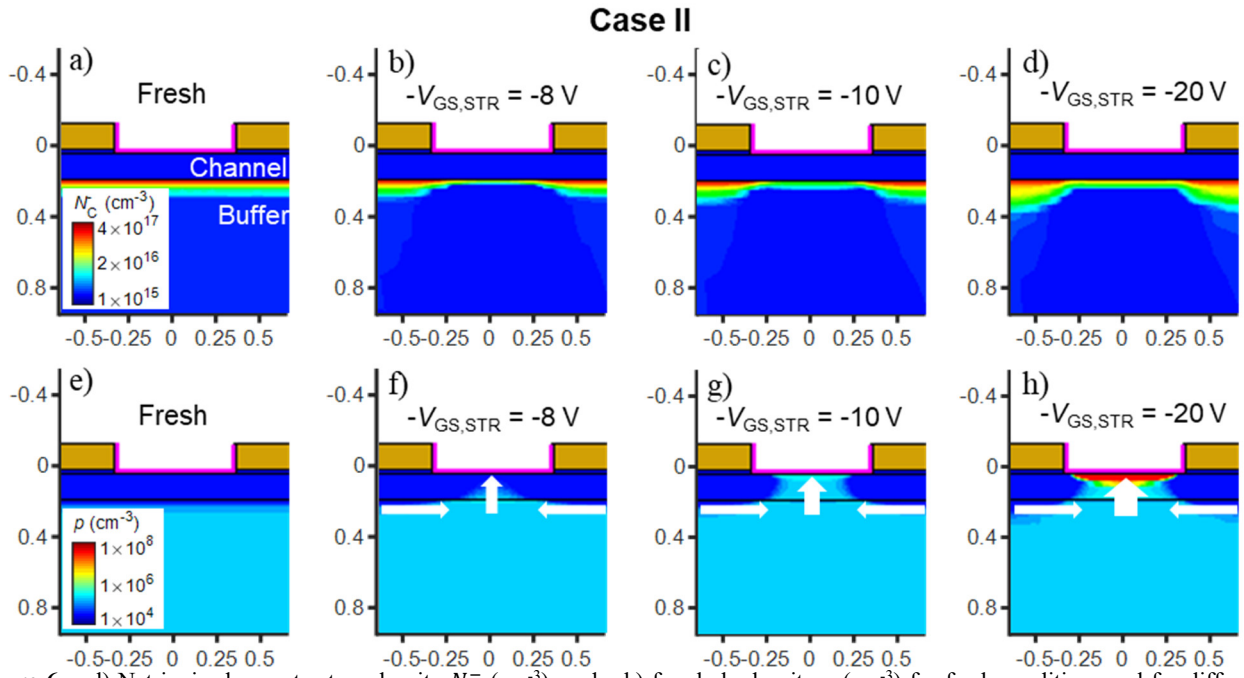

Figure 6. a-d) Net ionized acceptor trap density N_C^- (cm^{-3}), and e-h) free hole density p (cm^{-3}) for fresh conditions and for different -$V_{GS,STR}$ after 100 s stress for Case II. x-y axes scale is µm.

value for the largest $V_{GS,STR}$ of 20 V. This is the *combined effect of C doping and gate electron injection*. Interestingly (but not surprisingly), Case IV shows a similar trend to that of Case III, suggesting that a Schottky gate has a similar impact on the V_T instability as an insulated one if the gate insulator conductivity is non-negligible.

The physical mechanisms underlying the different V_T shifts can be understood with the aid of Figs. 4-6, showing the gate stress bias dependence of the 2D integrals under the gate of the following quantities: the negatively ionized C-related acceptor trap concentration (N_C^-), the free hole density (p), and the positively ionized interface trap density (N_{IT}^+). All of the three integrals are extended to the device region under the gate footprint from the gate dielectric/barrier interface (MIS-HEMT) or the Schottky contact (HEMT) to the buffer/nucleation layer interface.

The N_C^- integral features a non-monotonic dependence on -$V_{GS,STR}$ for all the four Cases I-IV above, see Fig. 4. This results from the presence of two opposite processes taking place during the 100-s stress phase at negative gate bias and dominating at small and large $V_{GS,STR}$, respectively: 1) the drifting of holes from the two access regions towards the gate region of the GaN buffer and the consequent hole capture increase into the C-related acceptor traps, leading to the decrease in the N_C^- integral under the gate; 2) the attraction of free holes from the GaN buffer region to the device surface and consequent enhanced hole emission from C-related acceptor traps, this instead leading to the increase in the N_C^- integral under the gate. This non-monotonic dependence of the N_C^- integral translates to bidirectional V_T shifts in cases III and IV, whereas other phenomena are at play in cases I

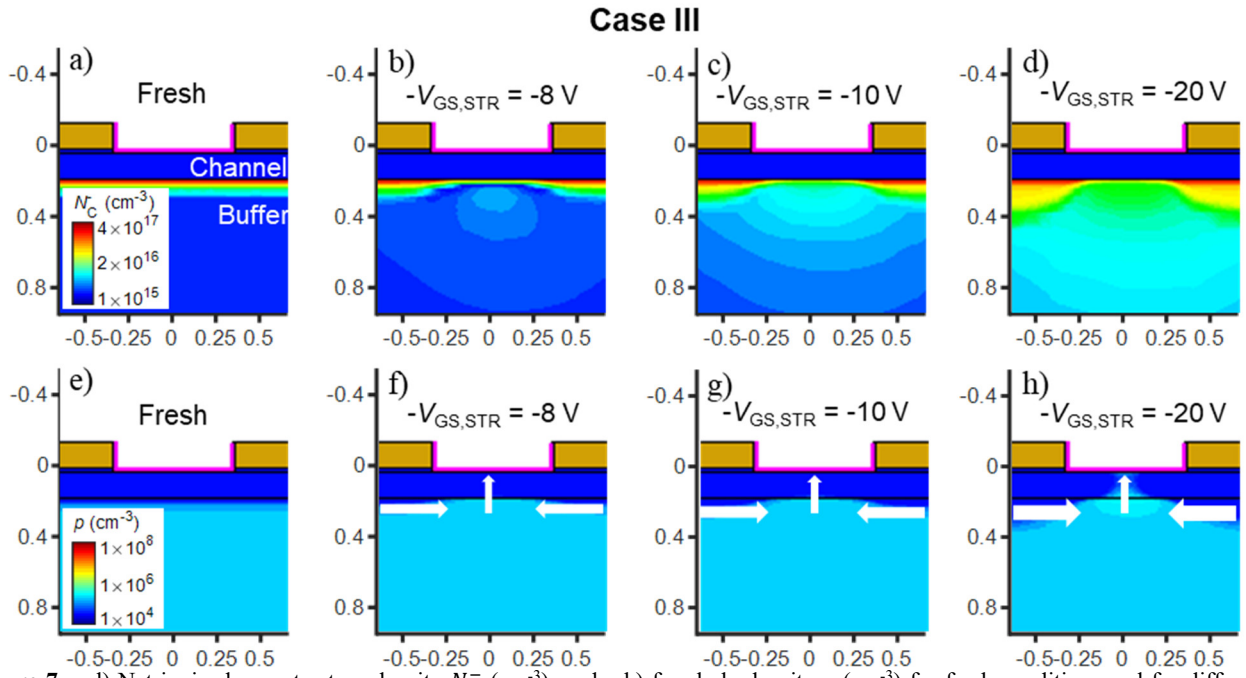

Figure 7. a-d) Net ionized acceptor trap density N_C^- (cm^{-3}), and e-h) free hole density p (cm^{-3}) for fresh conditions and for different -$V_{GS,STR}$ after 100 s stress for Case III. x-y axes scale is µm.

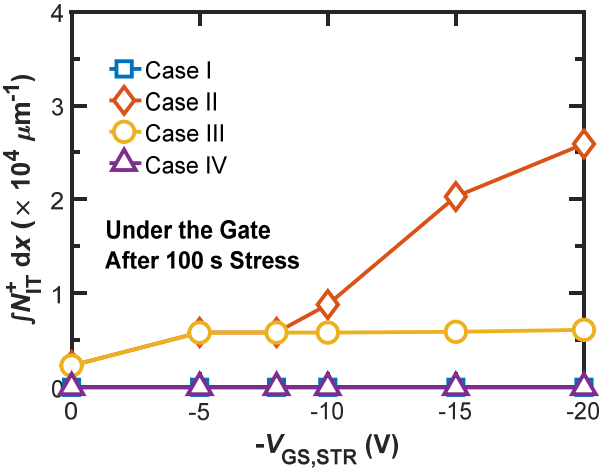

Figure 8. Gate stress bias (-$V_{GS,STR}$) dependence of the 2D integral of the positively ionized interface trap concentration (N_{IT}^+). The integral is extended to the device region under the gate footprint. Cases I-IV are defined in Tab. 2.

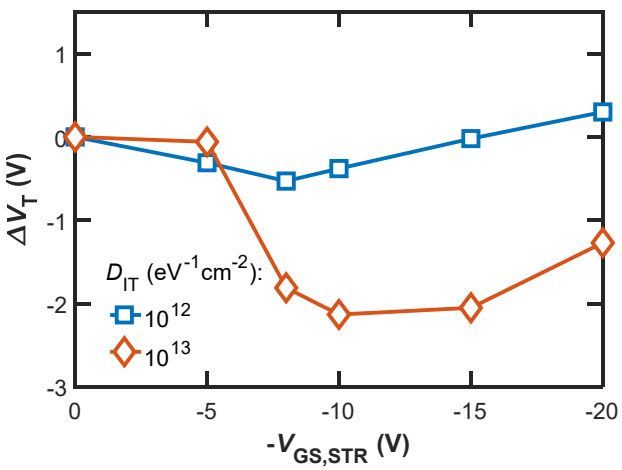

Figure 9. Threshold-voltage shifts (ΔV_T) vs gate stress bias (-$V_{GS,STR}$) for two values of D_{IT} for Case III.

and II compensating the increase in the N_C^- integral at large $V_{GS,STR}$ and thus making ΔV_T always negative.

The p integral becomes significant at sufficiently large $V_{GS,STR}$ for Case I and II, i.e. for the MIS-HEMT device with ideal gate dielectric, whereas it is always zero in Case III and IV, i.e. for the MIS-HEMT with conductive gate dielectric and the Schottky-gate HEMT, see Fig. 5. This results from the accumulation of free holes at the dielectric/barrier interface that can take place only in the MIS-HEMT structure with ideal gate dielectric (Case I and II). This accumulated positive charge contributes to making the V_T shits always negative even at large $V_{G,STR}$. On the other hand, holes attracted at the surface recombine with gate-injected electrons in the MIS-HEMT with conductive gate dielectric (Case III) or leak out from the device at the Schottky-gate contact in the HEMT (Case IV), explaining why the p integral is zero in these two cases.

Figures 6 and 7 show the 2-D contour plots of the N_C^- and p distributions in the device near the gate region for Case II and III, respectively. These figures better illustrate the difference between the above cases in terms of obtained ΔV_T trends. In Case II, the accumulation of free holes at the gate/insulator interface is much higher than in Case III leading to negative ΔV_T only. In the latter scenario, Case III, the holes emitted from C-related acceptors recombine with the electrons injected from the gate. Thus, the increase in the negative ionized charge in the buffer prevails determining the positive ΔV_T.

As can be seen in Fig. 8, the N_{IT}^+ integral is obviously always zero in Case I and IV where no D_{IT} is present. It can become significant for Case II, i.e. for the MIS-HEMT device with D_{IT} but with ideal gate dielectric, as a result of the concurrent effect of electron emission and hole capture into

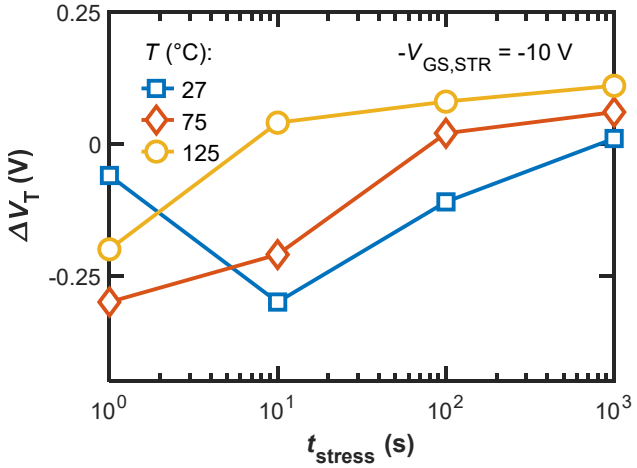

Figure 10. Threshold-voltage shifts (ΔV_T) as a function of stress time (t_{stress}) for a gate stress bias of -10 V and different temperatures for Case III.

interface traps. These effects explain the large, negative V_T shifts obtained for case II. It is finally non-zero but saturates at large $V_{GS,STR}$ for Case III, i.e. for the MIS-HEMT device with D_{IT} and conductive gate dielectric as a consequence of the competing effect of the trapping of gate-injected electrons into the interface traps and/or electron-hole recombination at the interface.

The contribution of the D_{IT} to the V_T instability is further analysed in Fig. 9, where ΔV_T is plotted against the stress voltage for case III for two different D_{IT} values. As can be noted, a higher D_{IT} results in a larger negative V_T shift. In devices with large D_{IT}, the effect of C doping on the V_T instabilities can therefore be masked. On the contrary, if/when the quality of the gate insulator/barrier interface is optimized and interface defects are reduced, V_T instabilities still occur as a result of Carbon doping in the buffer.

The impact of temperature is illustrated by Fig. 10, showing ΔV_T as a function of stress time for different temperatures. The analysed device is the MIS-HEMT with leaky dielectric (case III) featuring the more complex behaviour among those shown in Fig. 3, i.e. a bidirectional V_T instability. From Fig. 10, it can be noted that (i) a bidirectional V_T instability can be present not only depending on stress bias at room temperature (see Fig. 3) but also on increasing stress time for a given stress bias, (ii) increasing temperature shifts the ΔV_T curves to the left, this being a result of the shortened hole emission processes from C-related traps. This behaviour is similar to that reported for GaN MOSFETs in [13].

4. CONCLUSIONS

We have analyzed by means of numerical device simulations the possible role played by Carbon doping in the negative gate bias V_T instabilities in AlGaN/GaN MIS-HEMTs. Bidirectional threshold voltage shifts can at least in part be related to C doping, as a result of the modulation of the negative charge trapped into the C-related acceptors as well as the accumulation/recombination at the device surface of free holes generated by C doping.

More specifically, our simulation results point out that *negative V_T shifts* can be the result of:

1) the increase in the positive interface charge due to electron emission from interface traps,
2) the decrease in the total negative charge stored in the C-related acceptors in the GaN buffer,
3) the increase in the positive interface charge due to hole capture into interface traps, where holes are provided by the C doping and not necessarily by a high-field electron-hole generation mechanism.

Process 1) is the one that is conventionally assumed and can be present also in devices without C doping. Processes 2) and 3) are consequences of the C doping.

On the other hand, *positive V_T shifts* can be the result of:

1) the increase in the negative charge stored in the insulator due to electron injection from the gate (in our simulations oxide traps are concentrated at the insulator/barrier interface),
2) the recombination of holes provided by the C doping (and attracted to the device surface) with electrons injected from the gate.

Process 1) is the one that is conventionally assumed and can be present also in devices without C doping. Process 2) is an effect of C doping.

In actual devices, the role of Carbon in V_T shifts can be masked by or, as mentioned above, have an interplay with other effects. Nevertheless, it is important for the technologist not to neglect it when interpreting V_T instability experiments during the device optimization loop. Moreover, our analysis points out that, even in devices with optimized gate dielectric and interface, residual V_T instabilities, related to Carbon doping, can still be present. These detrimental effects should ultimately be traded off with breakdown voltage similarly to what is done for Carbon-induced dynamic Ron degradation.

As a guideline for technologists, our results also suggest that negative-only V_T shifts at varying negative gate bias stresses are typical of MIS-HEMTs with negligible gate dielectric conductivity, whereas bidirectional, or even positive-only V_T shifts can be associated with non-negligible gate electron injection and leakage current through the gate dielectric.

REFERENCES

1. Chen, K.J., Haberlen, O., Lidow, A., Tsai, C.L., Ueda, T., Uemoto, Y., Wu, Y.: GaN-on-Si power technology: Devices and applications. IEEE Trans. Electron Devices. 64, 779–795 (2017). https://doi.org/10.1109/TED.2017.2657579
2. Amano, H., Baines, Y., Beam, E., Borga, M., Bouchet, T., Chalker, P.R., Charles, M., Chen, K.J., Chowdhury, N., Chu, R., De Santi, C., De Souza, M.M., Decoutere, S., Di Cioccio, L., Eckardt, B., Egawa, T., Fay, P., Freedsman, J.J., Guido, L., Häberlen, O., Haynes, G., Heckel, T., Hemakumara, D., Houston, P., Hu, J., Hua, M., Huang, Q., Huang, A., Jiang, S., Kawai, H., Kinzer, D., Kuball, M., Kumar, A., Lee, K.B., Li, X., Marcon, D., März, M., McCarthy, R., Meneghesso, G., Meneghini, M., Morvan, E., Nakajima, A., Narayanan, E.M.S., Oliver, S., Palacios, T., Piedra, D., Plissonnier, M., Reddy, R., Sun, M., Thayne, I., Torres, A., Trivellin, N., Unni, V., Uren, M.J., Van Hove, M., Wallis, D.J., Wang, J., Xie, J., Yagi, S., Yang, S., Youtsey, C., Yu, R., Zanoni, E., Zeltner, S., Zhang, Y.: The 2018 GaN power electronics roadmap. J. Phys. D. Appl. Phys. 51, 163001 (2018). https://doi.org/10.1088/1361-

6463/aaaf9d
3. Dogmus, E., Zegaoui, M., Medjdoub, F.: GaN-on-silicon high-electron-mobility transistor technology with ultra-low leakage up to 3000 v using local substrate removal and AlN ultra-wide bandgap. Appl. Phys. Express. 11, 034102 (2018). https://doi.org/10.7567/APEX.11.034102
4. Del Alamo, J.A., Lee, E.S.: Stability and Reliability of Lateral GaN Power Field-Effect Transistors. IEEE Trans. Electron Devices. 66, 4578–4590 (2019). https://doi.org/10.1109/TED.2019.2931718
5. Hua, M., Wei, J., Bao, Q., Zhang, Z., Zheng, Z., Chen, K.J.: Dependence of VTH Stability on Gate-Bias Under Reverse-Bias Stress in E-mode GaN MIS-FET. IEEE Electron Device Lett. 39, 413–416 (2018). https://doi.org/10.1109/LED.2018.2791664
6. Meneghini, M., Rossetto, I., Bisi, D., Ruzzarin, M., Van Hove, M., Stoffels, S., Wu, T.L., Marcon, D., Decoutere, S., Meneghesso, G., Zanoni, E.: Negative bias-induced threshold voltage instability in GaN-on-Si power HEMTs. IEEE Electron Device Lett. 37, 474–477 (2016). https://doi.org/10.1109/LED.2016.2530693
7. Guo, A., Del Alamo, J.A.: Unified Mechanism for Positive- and Negative-Bias Temperature Instability in GaN MOSFETs. IEEE Trans. Electron Devices. 64, 2142–2147 (2017). https://doi.org/10.1109/TED.2017.2686840
8. Viey, A.G., Gaillard, F., Modica, R., Iucolano, F., Meneghini, M., Zanoni, E., Meneghesso, G., Ghibaudo, G., Vandendaele, W., Jaud, M.-A., Cluzel, J., Barnes, J.-P., Martin, S., Krakovinsky, A., Gwoziecki, R., Plissonnier, M.: Investigation of nBTI degradation on GaN-on-Si E-mode MOSc-HEMT. In: 2019 IEEE International Electron Devices Meeting (IEDM). pp. 4.3.1-4.3.4. IEEE, San Francisco, CA, USA (2019)
9. Hua, M., Wei, J., Bao, Q., He, J., Zhang, Z., Zheng, Z., Lei, J., Chen, K.J.: Reverse-bias stability and reliability of hole-barrier-free E-mode LPCVD-SiNx/GaN MIS-FETs. In: Technical Digest - International Electron Devices Meeting, IEDM. pp. 33.2.1-33.2.4. IEEE, San Francisco, CA, USA (2018)
10. He, J., Hua, M., Zhang, Z., Chen, K.J.: Performance and VTH Stability in E-Mode GaN Fully Recessed MIS-FETs and Partially Recessed MIS-HEMTs with LPCVD-SiNx/PECVD-SiNx Gate Dielectric Stack. IEEE Trans. Electron Devices. 65, 3185–3191 (2018). https://doi.org/10.1109/TED.2018.2850042
11. Hua, M., Wei, J., Bao, Q., Zheng, Z., Zhang, Z., He, J., Chen, K.J.: Hole-Induced Threshold Voltage Shift under Reverse-Bias Stress in E-Mode GaN MIS-FET. IEEE Trans. Electron Devices. 65, 3831–3838 (2018). https://doi.org/10.1109/TED.2018.2856998
12. Sang, F., Wang, M., Zhang, C., Tao, M., Xie, B., Wen, C.P., Wang, J., Hao, Y., Wu, W., Shen, B.: Investigation of the threshold voltage drift in enhancement mode GaN MOSFET under negative gate bias stress. Jpn. J. Appl. Phys. 54, 044101 (2015). https://doi.org/10.7567/JJAP.54.044101
13. Guo, A., Del Alamo, J.A.: Negative-bias temperature instability of GaN MOSFETs. In: IEEE International Reliability Physics Symposium Proceedings. pp. 4A11-4A16 (2016)
14. Bahat-Treidel, E., Brunner, F., Hilt, O., Cho, E., Würfl, J., Trankle, G.: AlGaN/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1 kV and low RON× A. IEEE Trans. Electron Devices. 57, 3050–3058 (2010). https://doi.org/10.1109/TED.2010.2069566
15. Soni, A., Ajay, Shrivastava, M.: Novel Drain-Connected Field Plate GaN HEMT Designs for Improved VBD-RON Tradeoff and RF PA Performance. IEEE Trans. Electron Devices. 67, 1718–1725 (2020). https://doi.org/10.1109/TED.2020.2976636
16. Uren, M.J., Moreke, J., Kuball, M.: Buffer design to minimize current collapse in GaN/AlGaN HFETs. IEEE Trans. Electron Devices. 59, 3327–3333 (2012). https://doi.org/10.1109/TED.2012.2216535
17. Chini, A., Iucolano, F.: Evolution of on-resistance (RON) and threshold voltage (VTH) in GaN HEMTs during switch-mode operation. Mater. Sci. Semicond. Process. 78, 127–131 (2018). https://doi.org/10.1016/j.mssp.2017.10.029
18. Synopsys: Sentaurus SDevice Manual (N-2017.09), (2017)
19. Sabui, G., Parbrook, P.J., Arredondo-Arechavala, M., Shen, Z.J.: Modeling and simulation of bulk gallium nitride power semiconductor devices. AIP Adv. 6, (2016). https://doi.org/10.1063/1.4948794
20. Ioffe Institute: New Semiconductor Materials. Characteristics and Properties, http://www.matprop.ru/
21. Ber, E., Osman, B., Ritter, D.: Measurement of the Variable Surface Charge Concentration in Gallium Nitride and Implications on Device Modeling and Physics. IEEE Trans. Electron Devices. 66, 2100–2105 (2019). https://doi.org/10.1109/TED.2019.2901869
22. Armstrong, A., Poblenz, C., Green, D.S., Mishra, U.K., Speck, J.S., Ringel, S.A.: Impact of substrate temperature on the incorporation of carbon-related defects and mechanism for semi-insulating behavior in GaN grown by molecular beam epitaxy. Appl. Phys. Lett. 88, 082114 (2006). https://doi.org/10.1063/1.2179375
23. Koller, C., Pobegen, G., Ostermaier, C., Pogany, D.: Effect of Carbon Doping on Charging/Discharging Dynamics and Leakage Behavior of Carbon-Doped GaN. IEEE Trans. Electron Devices. 65, 5314–5321 (2018). https://doi.org/10.1109/TED.2018.2872552
24. Bao, S.Q.G.W., Ma, X.H., Chen, W.W., Yang, L., Hou, B., Zhu, Q., Zhu, J.J., Hao, Y.: Method of evaluating interface traps in Al2O3/AlGaN/GaN high electron mobility transistors. Chinese Phys. B. 28, (2019). https://doi.org/10.1088/1674-1056/28/6/067304
25. Marcon, D., Van Hove, M., De Jaeger, B., Posthuma, N., Wellekens, D., You, S., Kang, X., Wu, T.-L., Willems, M., Stoffels, S., Decoutere, S.: Direct comparison of GaN-based e-mode architectures (recessed MISHEMT and p-GaN HEMTs) processed on 200mm GaN-on-Si with Au-free technology. Gall. Nitride Mater. Devices X. 9363, 936311 (2015). https://doi.org/10.1117/12.2077806
26. Dutta, G., DasGupta, N., DasGupta, A.: Gate Leakage Mechanisms in AlInN/GaN and AlGaN/GaN MIS-HEMTs and Its Modeling. IEEE Trans. Electron Devices. 64, 3609–3615 (2017). https://doi.org/10.1109/TED.2017.2723932
27. Verzellesi, G., Morassi, L., Meneghesso, G., Meneghini, M., Zanoni, E., Pozzovivo, G., Lavanga, S., Detzel, T., Häberlen, O., Curatola, G.: Influence of buffer carbon doping on pulse and AC behavior of insulated-gate field-plated power AlGaN/GaN HEMTs. IEEE Electron Device Lett. 35, 443–445 (2014). https://doi.org/10.1109/LED.2014.2304680
28. Meneghesso, G., Silvestri, R., Meneghini, M., Cester, A., Zanoni, E., Verzellesi, G., Pozzovivo, G., Lavanga, S., Detzel, T., Haberlen, O., Curatola, G.: Threshold voltage instabilities in D-mode GaN HEMTs for power switching applications. IEEE Int. Reliab. Phys. Symp. Proc. 6–10 (2014). https://doi.org/10.1109/IRPS.2014.6861109
29. Iucolano, F., Parisi, A., Reina, S., Patti, A., Coffa, S., Meneghesso, G., Verzellesi, G., Fantini, F., Chini, A.: Correlation between dynamic Rdsou transients and Carbon related buffer traps in AlGaN/GaN HEMTs. IEEE Int. Reliab. Phys. Symp. Proc. CD21–CD24 (2016). https://doi.org/10.1109/IRPS.2016.7574586
30. Chini, A., Meneghesso, Meneghini, M., Fantini, F., Verzellesi, G., Patti, A., Iucolano, F., Meneghesso, G., Meneghini, M., Fantini, F., Verzellesi, G., Patti, A., Iucolano, F.: Experimental

and Numerical Analysis of Hole Emission Process From Carbon-Related Traps in GaN Buffer Layers. IEEE Trans. Electron Devices. 63, 3473–3478 (2016). https://doi.org/10.1109/ted.2016.2593791
31. Zagni, N., Puglisi, F.M., Pavan, P., Chini, A., Verzellesi, G.: Insights into the off-state breakdown mechanisms in power GaN HEMTs. Microelectron. Reliab. 100–101, 113374 (2019). https://doi.org/10.1016/j.microrel.2019.06.066
32. Zagni, N., Chini, A., Puglisi, F.M., Pavan, P., Verzellesi, G.: The Role of Carbon Doping on Breakdown, Current Collapse, and Dynamic On-Resistance Recovery in AlGaN/GaN High Electron Mobility Transistors on Semi-Insulating SiC Substrates. Phys. status solidi. 217, 1900762 (2019). https://doi.org/10.1002/pssa.201900762
33. Zagni, N., Chini, A., Puglisi, F.M., Pavan, P., Meneghini, M., Meneghesso, G., Zanoni, E., Verzellesi, G.: Trap Dynamics Model Explaining the R ON Stress / Recovery Behavior in Carbon-Doped Power. In: IEEE International Reliability Physics Symposium Proceedings. p. Accepted (2020)
34. Joshi, V., Tiwari, S.P., Shrivastava, M.: Part II: Proposals to Independently Engineer Donor and Acceptor Trap Concentrations in GaN Buffer for Ultrahigh Breakdown AlGaN/GaN HEMTs. IEEE Trans. Electron Devices. 66, 570–577 (2019). https://doi.org/10.1109/TED.2018.2878787
35. Lyons, J.L., Janotti, A., Van De Walle, C.G.: Effects of carbon on the electrical and optical properties of InN, GaN, and AlN. Phys. Rev. B - Condens. Matter Mater. Phys. 89, 1–8 (2014). https://doi.org/10.1103/PhysRevB.89.035204
36. Matsubara, M., Bellotti, E.: A first-principles study of carbon-related energy levels in GaN. I. Complexes formed by substitutional/interstitial carbons and gallium/nitrogen vacancies. J. Appl. Phys. 121, 195701 (2017). https://doi.org/10.1063/1.4983452
37. Fariza, A., Lesnik, A., Bläsing, J., Hoffmann, M.P., Hörich, F., Veit, P., Witte, H., Dadgar, A., Strittmatter, A.: On reduction of current leakage in GaN by carbon-doping. Appl. Phys. Lett. 109, 212102 (2016). https://doi.org/10.1063/1.4968823
38. Joshi, V., Tiwari, S.P., Shrivastava, M.: Part I: Physical Insight into Carbon-Doping-Induced Delayed Avalanche Action in GaN Buffer in AlGaN/GaN HEMTs. IEEE Trans. Electron Devices. 66, 561–569 (2019). https://doi.org/10.1109/TED.2018.2878770