Self-Heating Effect in Silicon-Germanium Heterostructure Bipolar Transistors in Stress and Operating Conditions

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***Abstract*— In recent times many systems in a wide range of application fields (e.g., health, material science, security, and communications) exploit the mm- and sub-mm-wave spectrum, which dramatically sped up the growth of the BiCMOS technology integrating silicon–germanium (SiGe) heterojunction bipolar transistors (HBTs) and passives. Today, the reliability of such devices is of primary concern, and particular attention is given to the device self-heating (SH), the importance of which is supposed to increase with the device scaling. In this work we develop a TCAD model for SiGe HBT devices that is used to investigate the SH effects in SiGe HBTs both in operating and stress conditions. We underline the different role played by impact ionization and carriers' and lattice heating on the device degradation. Results show the important role played by the back-end-of-line (BEOL) and by the substrate thermal resistance in dissipating the heat generated by impact ionization and hot-carriers. Simulations of the SH effects in stress conditions excluded annealing as the possible reason for the degradation dynamics reported in the literature, while simulations of stressed devices in measurement conditions revealed the presence of a hole hot spot that suggests a possible physical mechanism involved in the degradation slowdown at long stress times reported in the literature.**

Keywords – SiGe, Heterostructure Bipolar Transistor (HBT), Self-Heating, TCAD Simulation, Interface Traps, Stress.

I. INTRODUCTION

Recently, the increased interest in the mm-wave and sub-mm-wave portion of the electromagnetic spectrum [1-5] fostered the growth of the BiCMOS technology as a promising and attractive solution seamlessly integrating silicon–germanium (SiGe) heterojunction bipolar transistors (HBTs) and passive components. BiCMOS circuits such as amplifiers for next-generation 5G networks, dedicated circuits for the Internet of Things and automotive sectors, and THz industrial sensors find applications in many sectors, e.g., health, smart cities, security, and communications, thus constituting a large market not currently tackled by CMOS technology [1-5]. Indeed, also ultra-scaled FinFETs are definitely slower than SiGe HBTs when interconnections and parasitic effects are considered, with HBTs outperforming CMOS transistors in terms of cutoff and maximum oscillation frequencies. In addition, fabricating circuits in CMOS technology for relatively small markets such as those targeted by the BiCMOS technology would be extremely costly due to the necessary integration of on-chip passive components.

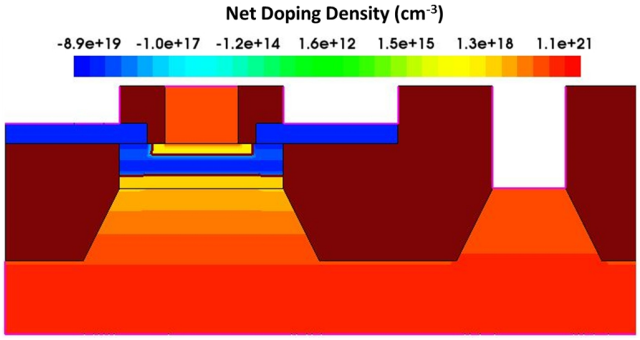

Fig. 1 – Schematic representation of the simulated HBT SiGe device. Color-code reflects the net doping density in the different regions of the device.

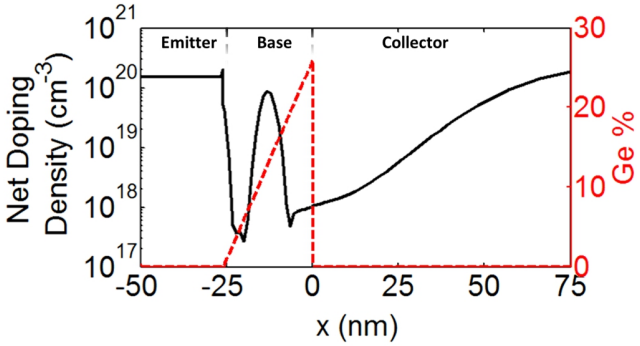

Fig. 2 – Doping (black solid line, left y-axis) and Ge % (red dashed line, right y-axis) vertical profiles. The emitter, base, and collector regions are evidenced.

Nowadays, a primary concern is the reliability of scaled SiGe devices, especially from the perspective of the device self-heating (SH) that becomes an increasingly significant issue as scaling proceeds [6-8]. Particularly, it is important to investigate the reliability issues of this technology in conditions that closely resemble the operating ones. In this paper we develop a 2D TCAD model for state-of-the-art SiGe HBTs and calibrate it on experimental data. The developed model is then used to investigate the SH effects in 55-nm BiCMOS SiGe HBT devices in operating conditions, as well as the role played

Parameter	Value
Emitter Doping	$1.5 \cdot 10^{20}$ cm^{-3}
Base Peak Doping	$9.9 \cdot 10^{19}$ cm^{-3}
Coll. Doping (min/max)	$2 \cdot 10^{18}/10^{21}$ cm^{-3}
Peak Ge %	26 %
R_{TH} Emitter	2 cm^2·mK/W
R_{TH} Base	0.1 cm^2·mK/W
R_{TH} Collector	0.2 cm^2·mK/W
R_{TH} Substrate	3.5 cm^2·mK/W *

Tab. I – Calibrated process parameters (doping levels, peak Ge % in the base, and thermal resistance at both the electrical contacts and the substrate). * from [11].

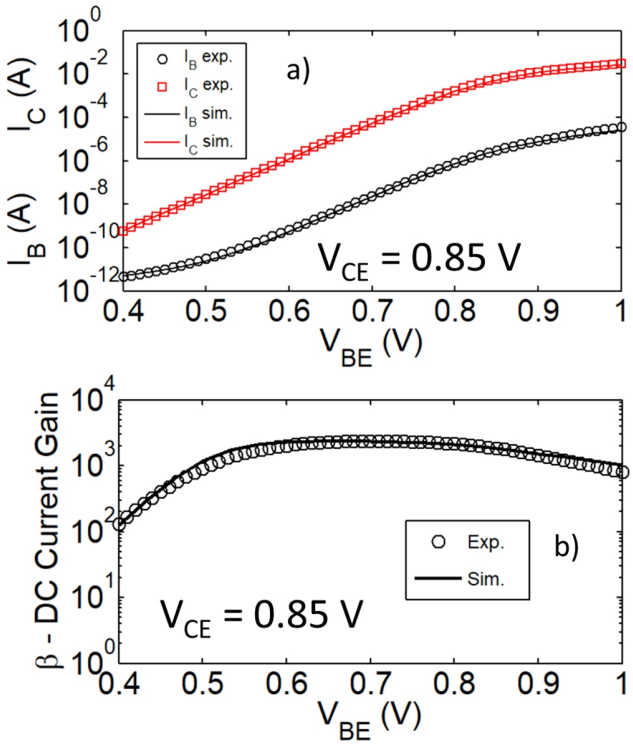

Fig. 3 – Comparison between experimental data (symbols) and 2D TCAD simulations (lines). (a) I_C vs V_{BE} (black) and I_B vs V_{BE} (red) at V_{CE} = 0.85V. (b) DC current gain ($\beta = I_C / I_B$) vs. V_{BE} at V_{CE} = 0.85V.

by SH in the degradation dynamics observed in mixed-mode stress experiments. We focus on SH effects not only in operating conditions but also during stress to gain further insights into the physical mechanisms ruling over the device degradation, underlining the different roles played by the thermal design of the substrate and of the metallization, the impact ionization, and the carriers' and lattice heating in the two regimes.

II. Devices, Experiments, and Simulations

The devices under study are state of the art SiGe HBTs in 55-nm BiCMOS technology, Fig. 1. Devices, in CBEBC configuration, have an emitter window of 5.56 x 0.42 μm^2. Forward Gummel and output curves are collected on both fresh and stressed devices at different stages of cumulative stress. Stress is performed by applying an emitter current density, J_E =

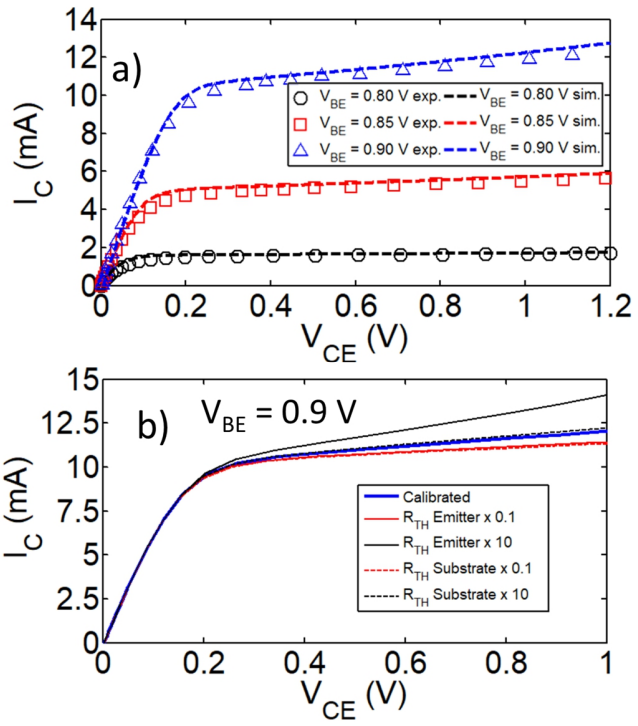

Fig. 4 – Experimental (symbols) and simulated (lines) output curves at different V_{BE} in the range 0.8 V to 0.9 V typically used in circuits (different symbols and colors). (b) Output curve sensitivity to the substrate (dashed lines) and emitter (solid lines) thermal resistance values.

1 mA/μm^2, corresponding to a V_{BE} value in the typical operating range where the peak f_T is obtained [1], and V_{CB} = 3 V to get non negligible degradation in a reasonable amount of time while keeping stress conditions close to the operating ones. The structure of the device implemented in SDevice™ is reported in Fig. 1, while in Fig. 2 the vertical doping and Ge content profiles are reported. The doping profile in the emitter is assumed constant, while a Gaussian doping profile is assumed in the base region. The doping profile in the collector and sub-collector regions (as well as the overall profile shown in Fig. 2) is also in-line with the predictions of the TCAD-based roadmap developed few years ago in the framework of the DOTSEVEN project [1]. The Ge content linear profile in the base is shown in Fig. 2. The peak doping values in all regions and the peak Ge relative content in the SiGe base are reported in Tab. I. Carefully reproducing the device transfer (forward Gummel) and output curves, Figs. 3 and 4, required hydrodynamic simulations [9] including calibrated models for carriers' recombination (Shockley-Read-Hall including trap-assisted contribution), impact ionization (Okuto model), and field-, material-, and doping-dependent mobility. However, the calibration procedure of the parameters of such models for SiGe only required slight adjustments of few parameters, while default values for Si and polysilicon were used, which further supports the dependability of our TCAD model. Series resistances were included at all contacts, and their values were calibrated to capture the behavior of the output curves in the saturation region. The emitter contact non-idealities are included by assuming a finite recombination velocity for holes, as reported in the literature [10]. To capture the behavior of the

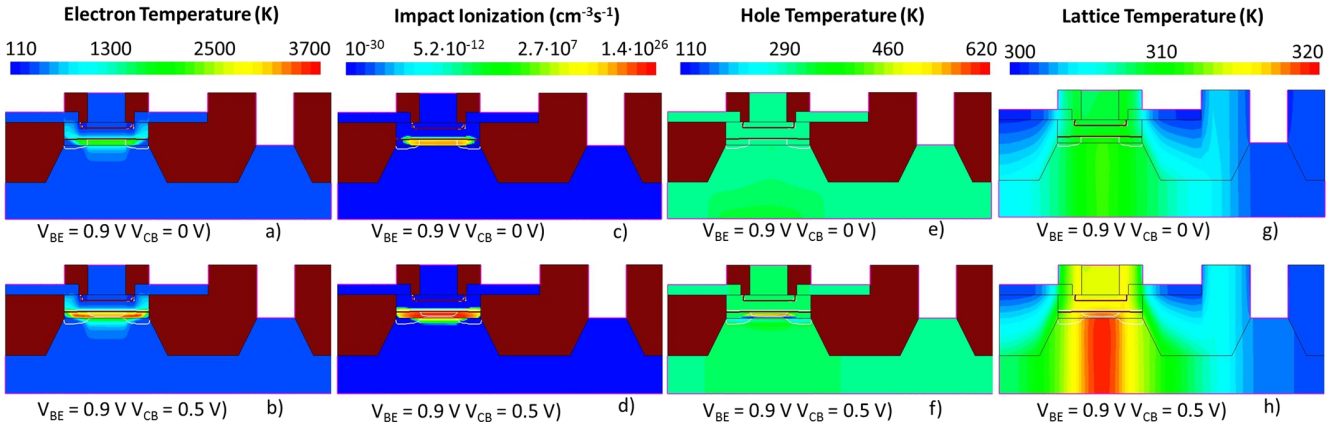

Fig. 5 – Simulated 2D maps of (a-b) e^- temperature, (c-d) impact ionization rate, (e-f) h^+ temperature, and (g-h) lattice temperature at V_{BE} = 0.9V and (a, c, e, g) V_{CB} = 0V, (b, d, f, h) V_{CB} = 0.5V. The bottleneck for heat dissipation is the substrate due to its larger thermal resistance as compared to the one given by the BEOL over the contacts.

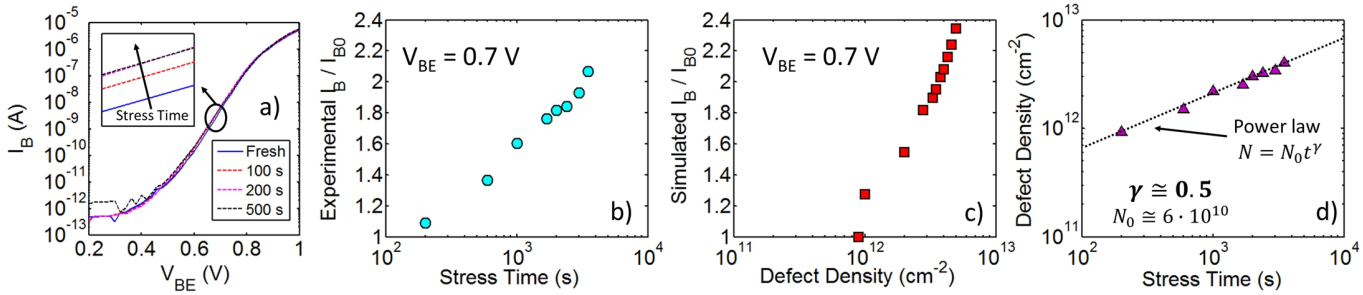

Fig. 6 – (a) Experimental I_B vs. V_{BE} curves at different levels of cumulative stress. (b) Experimental I_B degradation as in (a) measured at V_{BE} = 0.7 V vs. cumulative stress time. (c) Simulated I_B degradation at V_{BE} = 0.7 V at different defect density values. (d) Extracted defect density vs. cumulative stress time along with a power-law fitting.

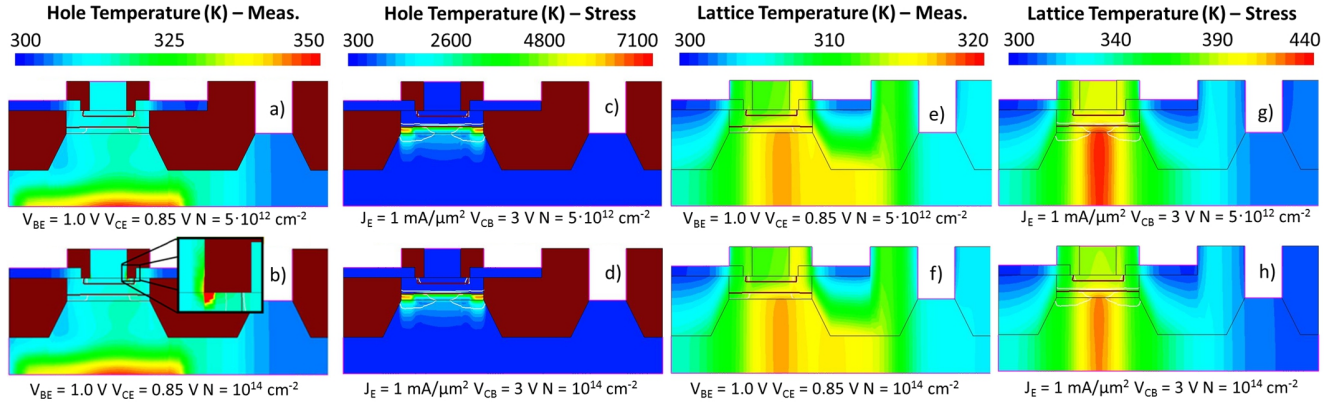

Fig. 7 – Simulated 2D maps of (a-b-c-d) h^+ temperature, and (e-f-g-h) lattice temperature in (a, b, e, f) measurement conditions, i.e., V_{BE} = 1.0 V and V_{CE} = 0.85 V, and (c, d, g, h) stress conditions – J_E = 1 mA/μm², V_{CB} = 3 V – at defect density of (a, c, e, g) $5 \cdot 10^{12}$ cm^{-2}, and (b, d, f, h) 10^{14} cm^{-2}. In (b) a zoom-in shows a hot hole spot close to the region where defects are located.

output curves in the active region, i.e., at relatively high V_{CE}, Fig. 4, thermal resistance for all the *thermodes* (thermal interfaces located at the emitter, base, and collector contacts and at the bottom of the substrate) needs to be included, and their value strongly affect the output curve slope in the active region [11], since they determine the SH dynamics, Fig. 4b. The value of thermal resistance at the emitter, base, and collector contacts may strongly vary with processing schemes and conditions due to the presence of the metal lines of the back-end of line (BEOL), the properties of which have a strong influence on the local thermal dissipation. As such, these values were calibrated to obtain the best possible fit of the output curves, Fig. 4. The thermal resistance of the substrate *thermode* was instead set in agreement with previous results reported in the literature [11]. The calibrated values for all thermal resistances are reported in Tab. I. Finally, fitting the I_B-

V_{BE} curve at low V_{BE} required including auger recombination, band to band tunneling, and trap-assisted tunneling at defects at the emitter-base (E-B) spacer interface, that are included with a density of $6 \cdot 10^{10}$ cm^{-2}.

III. Self-Heating in Operating Conditions

The proposed model is used to make predictions on the reliability of these devices in operating and stress conditions. Particularly, we explore the detrimental effects of hot-carrier degradation (HCD) on i) the device self-heating (SH) and ii) the formation of interface defects at the E-B spacer that cause an excess base current due to trap-assisted recombination. Fig. 5 shows the 2D maps of the impact ionization rate, and of electron, hole, and lattice temperature in operating conditions. Hot-carriers (e^- and h^+) driven by the V_{CB} cause impact ionization in the depleted collector-base junction leading to localized power dissipation and the generation of e^-/h^+ pairs. This is evidenced in Fig. 5(a-f), where it can be easily seen that i) the impact ionization rate strongly depends on the field in the depleted collector-base junction, hence on the V_{CB}, and ii) the electron and hole temperature maps well correlate with the impact ionization rate map. The carriers generated by impact ionization are then driven by the applied electric field toward the E-B spacer where they are able to dissociate Si-H bonds at the Si/SiO_2 interface generating new interface defects [7, 12]. Nevertheless, the heat that is locally produced is transferred to the lattice and then dissipated through the substrate and the BEOL over the electrical contacts that act like heat sinks. Evidently, the metal BEOL constitutes a much better heat sink than the substrate. For this reason, the lattice temperature map badly correlated with the carriers' temperature maps, and the lattice temperature reaches its peak in the collector region, as the substrate behaves as the thermal dissipation bottleneck. Decreasing the effective thermal resistance at the substrate interface could hence be effective in minimizing SH. Indeed, recent attempts are found in the literature that try to perform thermal-management design for HBT devices (although in GaAs technology) by placing a 2D graphene heat spreader in contact with the substrate [13]. However, SH in operating conditions is not critical for the technology under study, as the lattice temperature increase is limited to few tens of degrees in typical operating conditions (~20 K increase from 300 K at V_{BE} = 0.9 V and V_{CB} = 0.5 V).

IV. The Role of Self-Heating during Stress

Besides being involved in the device SH, HCD plays a crucial role during stress by creating defects at the E-B spacer interface. The corresponding measured I_B degradation is shown in Fig. 6(a-b), and has been reproduced by simulations with increasing defect density in the range $10^{12} – 5 \cdot 10^{12}$ cm^{-2}, Fig. 6c, consistently with previous estimates [7]. This allows mapping the defect density evolution over time during stress, Fig. 6d, that is well reproduced by a power-law (t^{γ}), with γ = 0.5. This value agrees with the one reported in the literature [7] for SiGe HBT devices stressed in both similar and different conditions, as well as with a new compact ageing model [12] (for the stress time range used in this study), further validating the proposed TCAD model. However, at very long cumulative stress times (i.e. on the order of 1000 hours, depending on the stress condition) the degradation trend tends to change showing a reduction in γ, as reported in the literature [7, 12]. The model is now used to gain insights into this phenomenon, by analyzing the role of temperature during the i) stress and ii) measurement phases cyclically run during the stress experiment. In Fig. 7 we compare the results of simulations at medium (i.e., $5 \cdot 10^{12}$ cm^{-2}) and very high (i.e., 10^{14} cm^{-2}) defect density, both in stress and in measurement conditions. Notice that the two defect density values chosen for this analysis correspond to a cumulative stress time of few thousands of seconds (medium defect density) and ~800 hours (very defect high density) in the stress conditions used in this work. In stress conditions neither the lattice nor the carriers' temperature profiles change with defect density, which excludes annealing as a possible mechanism leading to the observed reduction in γ. The latter is thought to be related to a saturation of the available Si-H bonds [12]. However, in measurement conditions, while the lattice temperature is unaffected by defect density (as expected), the hole temperature profile shows a hot spot at the defects' location only when considering a high defect density, suggesting that hot holes could be involved in the observed γ reduction as well. The hot spot indicates a loss of trapped holes due to electron injection, which is accompanied by a reduction of interface traps [14], contributing to the slowdown of the degradation dynamics. While the investigation of this mechanism deserves a more in-depth study, this demonstrates the usefulness of the developed model in exploring the reliability issues of SiGe HBT technology, not only at the device level but also for circuit reliability studies [15].

V. Conclusions

In this work, we developed a TCAD model for state-of-the-art SiGe HBT devices, calibrated on experimental data. The model was used to investigate the SH effects in both stress and measurement conditions. Results show the important role played by the thermal dissipation properties of the BEOL and by the substrate thermal resistance in dissipating the excess heat generated by impact ionization and transferred to the lattice. However, simulations in typical operating conditions show that the lattice temperature increase reaches at most 20 K, which can be further minimized by optimizing the substrate thermal resistance. Combining experimental mixed-mode stress data with TCAD simulations it has been possible to estimate the defect generation rate, which is found to be in agreement with earlier reports. Simulations of the SH effects in stressed devices in stress conditions excluded annealing as the possible reason for the slowdown of the degradation dynamics reported in the literature at long stress times. On the other hand, simulations of a stressed device (with a high defect density at the E-B spacer interface) in measurement conditions revealed the presence of a hole hot spot possibly involved in the γ reduction observed at very long stress times.

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