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The Role of Carbon Doping on Breakdown, Current Collapse and Dynamic R_{ON} Recovery in AlGaN/GaN High Electron Mobility Transistors on Semi-Insulating SiC Substrates

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Keywords: GaN HEMTs, C-doping, impact ionization, breakdown, current collapse, dynamic R_{ON} recovery

Abstract: In this work, the critical role of carbon doping in the electrical behavior of AlGaN/GaN High Electron Mobility Transistors (HEMTs) on semi-insulating SiC substrates is assessed by investigating the off-state three terminal breakdown, current collapse and dynamic on-resistance recovery at high drain-source voltages. Extensive device simulations of typical GaN HEMT structures are carried out and compared to experimental data from published, state-of-the-art technologies to: *i)* explain the slope of the breakdown voltage as a function of the gate-to-drain spacing lower than GaN critical electric field as a result of the non-uniform electrical field distribution in the gate-drain access region; *ii)* attribute the drain current collapse to trapping in deep acceptor states in the buffer associated with carbon doping; *iii)* interpret the partial dynamic on-resistance recovery after off-state stress at high drain-source voltages as a consequence of hole generation and trapping.

1. Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are widely investigated and developed for power switching and power RF applications thanks to their potentially superior

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performance compared to Si and SiC based devices. For example, in terms of the Baliga Figure Of Merit (B-FOM) – that relates the breakdown voltage, V_{BR}, to the specific on-resistance $R_{ON} \times A$ via material intrinsic properties – GaN has an outstanding value of 870 compared to 340 of SiC, with Si taken as reference (i.e., equal to 1) [1]. The reduction of the off-state punch-through currents to increase the high-voltage capability of AlGaN/GaN HEMTs is often achieved by introducing acceptor trap states in the buffer layer(s) underlying the device channel through carbon (C) dopant [2].

In this work, we discuss the critical role of C-doping to achieve lower drain-source leakage current and higher breakdown voltage as well as its impact on the dynamic on-resistance, R_{ON}. The analysis is carried out by means of numerical device simulations. Experimental data from state-of-art technologies reported in the open literature are adopted in order to calibrate device simulations as well as to show their suitability to explain actual device behavior. More specifically three experimentally observed phenomena are analyzed: *i)* V_{BR} dependence on gate-to-drain length, L_{GD}, with a slope lower than GaN critical field; *ii)* current-collapse in pulsed measurements of output characteristics; *iii)* dynamic R_{ON} recovery with increasing off-state stress bias. The rest of the paper is organized as follows. Section 2 describes the simulated device cross-section and the models employed to reproduce experimental data. Section 3 shows the results of the calibration process and the comparison between simulations and experimental data on V_{BR} vs. L_{GD} and $I_D - V_{DS}$ current collapse. In Section 4, we exploit the device model to interpret the results on the dynamic R_{ON} recovery found in several device technologies reported in the literature [3]–[6]. Conclusions are drawn in Section 5.

2. Simulated Device Structure and Models

The simulated device cross-section is shown schematically in **Figure 1**. Device dimensions resemble the ones of the fabricated device in [2]. Gate-source spacing (L_{GS}), gate length (L_G) and gate field plate overhang (L_{FP}) are 1, 0.7, 0.6 μm, respectively. The substrate is semi-insulating SiC,

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left floating during both measurements and simulations (except for the dynamic R_{ON} recovery analysis, as explained in Section 4). In general, the epitaxy of GaN HEMTs is more complex than that of [2], especially in technologies for power switching applications, in which the substrate is typically p-type Si and complex strain-relief layers are adopted. The conducting Si substrate is typically grounded, resulting in high vertical fields that influence charge storage and potential distribution in the device. This work focuses on GaN HEMTs on semi-insulating SiC which is the typical choice for RF applications. In particular, the simulated structure does not include strain relief layers, it includes a 100 nm thick AlN nucleation layer and a 100 um thick undoped SiC substrate. The main feature of the device is the C-doped GaN back-barrier underneath the channel that renders the buffer semi-insulating thereby increasing the maximum breakdown voltage and improving the B-FOM, as discussed more in detail in [2]. The simulation software adopted for the device analysis is the commercial suite SDevice^{TM} (Synopsys Inc.). Charge transport was accounted for by means of the drift-diffusion model. Deep-level traps were accounted for by including, for each distinct trap level, one trap-balance equation, describing, within the framework of the Shockley-Read-Hall theory, the dynamics of trap occupation without any quasi-static approximation. Piezoelectric polarization was included by using the default strain model of SDevice^{TM}. Both the gate and source/drain contacts were modeled as Schottky contacts with proper energy barriers. Electron tunneling was activated at the contacts to reproduce the gate leakage current and to mimic ohmic behavior at the source and drain contacts. Impact-ionization coefficients for both electrons and holes were set in agreement with recent Monte-Carlo calculations [7]. C-doping in the GaN back-barrier was modeled by considering a dominant deep acceptor level (at 0.9 eV from the valence-band edge, E_V), partially compensated by a shallow donor level (at 0.11 eV from the conduction-band edge, E_C). Specifically, the adopted C-related acceptor and donor concentrations were 8×10^{17} cm^{-3} and 4×10^{17} cm^{-3}, respectively. For more accurate determination of the effective trap concentration, one should rely on C-V measurements

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[8] . In this work, we calibrated the carbon-related trap concentration in order to match results in terms of DC characteristics and off-state breakdown, as C-V measurements were absent for the fabricated devices [2]. The choice of the C-doping model adopted in this work is justified by the fact that by adjusting the donor-acceptor auto-compensation ratio it is possible to accurately reproduce dynamic effects in different AlGaN/GaN power HEMTs [9]–[13]. Moreover, a higher donor concentration in C-doped GaN compared to the donor density measured in unintentionally doped samples was experimentally confirmed in [14], and attributed to the auto-compensation between C related donors and acceptors, as assumed here. Finally, a similar C-doping model with high donor-acceptor auto-compensation was found also by other authors to be instrumental to reproduce breakdown effects in C-doped AlGaN/GaN HEMTs by means of device simulations [15].

3. Breakdown and Current Collapse

The calibration of the simulation set-up against experimental results from [2] is illustrated by **Figure 2**. Figure 2a) shows the comparison between simulated and measured transfer characteristics of the GaN HEMTs under study. Figure 2b) shows the comparison between measurements and simulations of breakdown voltage for devices with different L_{GD} . The breakdown condition is defined as the V_{DS} bias necessary to reach 1 mA/mm of off-state I_D [2]. Detailed comparison between measured and simulated off-state $I_D - V_{DS}$ curves were reported elsewhere [16]. The achieved agreement shows that the model employed for the C-doping in the back-barrier is indeed effective in the prediction of the lateral breakdown limits of the fabricated devices. As shown in Figure 2b), the slope of the V_{BR} vs L_{GD} curve is lower than the critical field of GaN (of about 3.9 $\mathrm{MV/cm}$ [17]) despite breakdown being induced, according to our simulations, by avalanche generation. This is attributed to the highly non-uniform electric field distribution in the depletion region between gate and drain [16], allowing the critical field to be reached in a localized spot at the drain end of the gate-drain access region even if the average field is still much smaller than the critical field.

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One shortcoming of introducing traps in the GaN buffer is the DC-to-dynamic drain current dispersion, also referred to as current collapse, that limits the maximum achievable output power. This effect is commonly estimated through pulsed $I_D - V_{DS}$ measurements with different baseline conditions to either induce or suppress trapping. This is shown in **Figure 3**, where two different baseline biases are applied during $I_D - V_{DS}$ simulations and measurements (taken at V_{GS} of 1 V and 2 V), namely $\left(V_{GS,BL1}, V_{DS,BL1}\right) = (0, 0)$ V and $\left(V_{GS,BL2}, V_{DS,BL2}\right) = (-0.8, 30)$ V . Measurements are still taken from Ref. 2. The first baseline for gate and drain is benign with respect to charge trapping. On the other hand, the second baseline biases the device in semi-on conditions with a high drain voltage (corresponding to class-AB operating point [2]), causing the acceptor states in the buffer to accumulate negative charges (by emitting holes) and giving rise to current dispersion as the device is pulsed to on-state conditions. The model adopted for the C-doping in the simulations, see Figure 3a), is able to reproduce the experimental data, shown in Figure 3b), and also the drain current dispersion due to the acceptor traps associated with C-doping.

4. Dynamic R_{ON} recovery

In this section, we exploit the device model employed in Section 3 to give an interpretation of the partial recovery of the dynamic R_{ON}. This behavior was observed in several different state-of-art power GaN HEMT technologies on Silicon substrates for V_{DS} stress voltage beyond some critical value in the 100-300 V range [3]–[6]. A similar behavior is exhibited also by devices simulated in this work. The phenomenon is illustrated by the simulation results shown in **Figure 4a)**. The simulations were carried out on a structure similar to the one shown in Figure 1, with grounded substrate and with a gate-to-drain spacing L_{GD} of 10 μm. All other parameters are the same as for simulations allowing to reproduce DC, breakdown, and current collapse curves described in Sections 2 and 3. All simulations were carried out with the same off-state gate bias $V_{GS,OFF} = -5$ V, while the drain stress bias was increased from 0 to 600 V, activating/deactivating

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impact ionization. The results shown in Figure 4a) indicate that the R_{ON} recovery at high $V_{DS,OFF}$ can be reproduced only when impact ionization is included (red squares). In fact, if impact ionization is deactivated (yellow triangles), R_{ON} saturates and does not invert the degradation trend at high drain stress voltages. This can be appreciated also with the aid of **Figure 5a)**, showing the simulated $I_D - V_{DS}$ curves taken at $V_{GS} = 2$ V after the off-state stress, for low and high drain pre-stress voltage ($V_{DS,OFF} = 100$ V and 600 V , blue and red curves, respectively), activating/deactivating impact ionization (solid and dashed curves, respectively). Indeed, Figure 5a) shows that the drain current in the linear regime, where the drain access resistance has an impact, is increased after the stress at $V_{DS,OFF} = 600$ V with respect to the case at $V_{DS,OFF} = 100$ V only if impact ionization is included in the device simulation. This result is consistent with the plot in Figure 4a) and with measured $I_D - V_{DS}$ taken from [3] under similar conditions, shown in Figure 5b). The degradation followed by (partial) recovery of R_{ON} was observed in several different devices as documented in the literature [3]–[6], see Figure 4b). We interpret this recovery behavior as a result of hole trapping into C-doping related acceptor traps in the buffer. This is in turn due to the generation of holes by impact ionization. This process is illustrated by **Figure 6**, showing contour plots of the net ionized acceptor trap concentration (i.e., $N_A^- - N_D^+$) under the same conditions, with and without impact ionization. In the case with impact ionization included, compare Figure 6a), b), it is possible to observe a decrease in the concentration of the ionized acceptors with increasing drain stress voltage due to avalanche generated holes in the buffer and resulting hole trapping into C-related acceptor traps. Conversely, in the case without impact ionization included, compare Figure 6c), d), the ionized acceptor concentration increases (up to the effective acceptor concentration) with increasing stress, leading to the saturation of R_{ON}.

Other effects might arise which could explain the results discussed in this section. For example, the model in [4] relies on the vertical leakage paths between 2DEG and the carbon-doped GaN layer to explain the partial recovery of R_{ON}. In this work, we consider a simplified scenario

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with no leakage paths and focus only on the role of C-doping and show that impact ionization might be at the origin of (or might contribute to) the recovery of R_{ON} for high stress bias.

5. Conclusion

We conducted systematic device simulations of AlGaN/GaN HEMTs to assess the critical role of Carbon doping in the buffer. Through the simulation set-up calibrated through comparison with measurement data, we analyzed the breakdown voltage dependence on the gate-to-drain spacing, the current collapse under pulsed operation and the dynamic on-resistance recovery at increasing drain stress biases. We concluded that the observed breakdown voltage vs gate-to-drain spacing slope lower than the GaN critical field is due to the non-uniform electric field causing avalanche breakdown to occur in a localized spot of the drain access region. Current collapse is attributed to hole detrapping from the deep acceptor states associated with C-doping in the buffer during the off-state stress phase of pulsed measurements. Finally, it is suggested that generation of holes by impact ionization and subsequent hole trapping into the C-related acceptors can contribute to the dynamic on-resistance recovery at high drain stress voltages.

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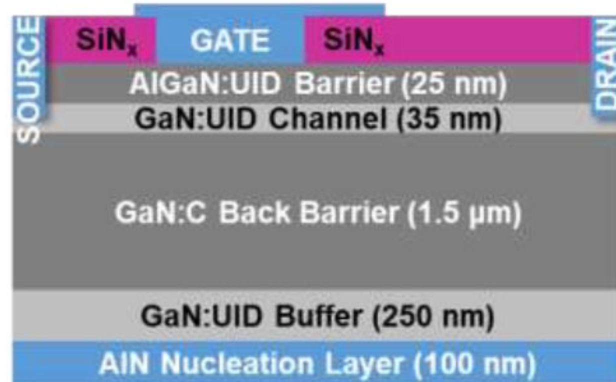

Figure 1. Simulated AlGaN/GaN HEMT cross-section to reproduce results from [2].

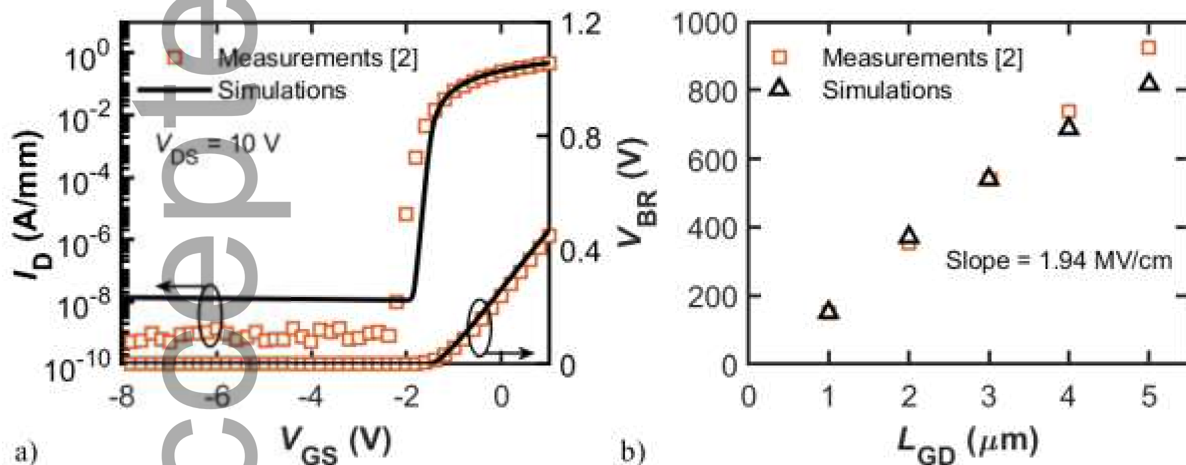

Figure 2. a) $I_D - V_{GS}$ curves, showing the agreement between measurements from [2] (red squares) and simulations (black solid curves). b) V_{BR} vs. L_{GD} curve showing that the simulation set-up reproduces the experimental breakdown data.

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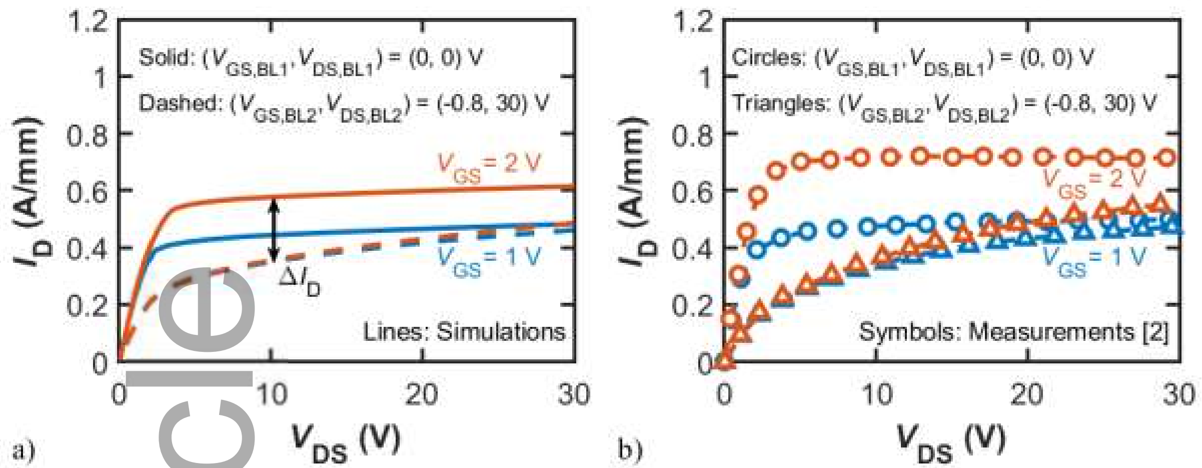

Figure 3. Current-Collapse (CC) in the a) simulated (lines) and b) measured (symbols) pulsed $I_D - V_{DS}$ curves. Curves have been taken for above-threshold V_{GS} of 1 V and 2 V. CC is evaluated as the drain current decrease ΔI_D occurring due to stress in the condition determined by the baseline voltages $V_{GS,BL}$ and $V_{DS,BL}$.

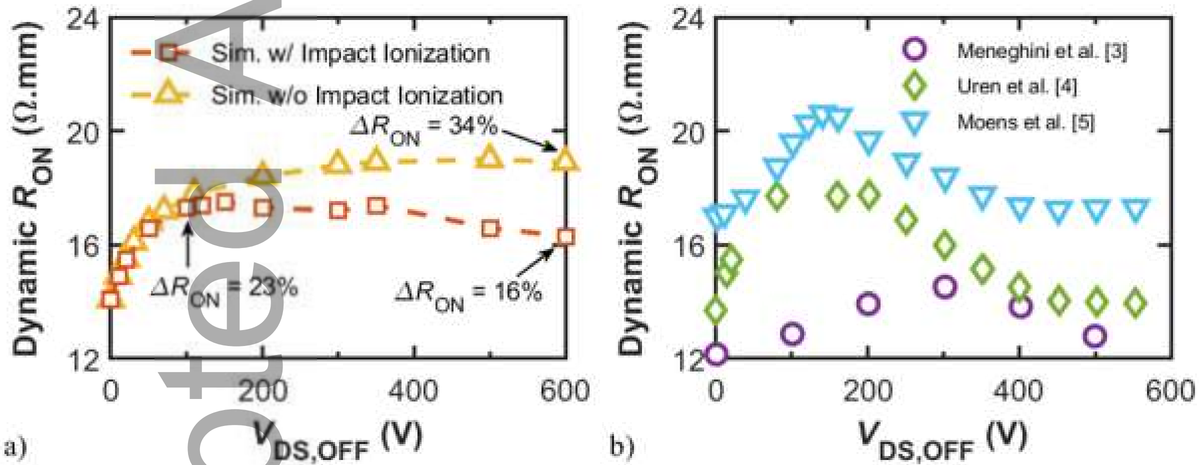

Figure 4. Dynamic R_{ON} degradation and recovery in a) simulated and b) measured devices. In a) simulations are carried out with (red squares) and without (yellow triangles) impact ionization, to show that only with hole generation it is possible to qualitatively reproduce the R_{ON} recovery behavior found in experimental data shown in b). A typical stress time of 100 s was adopted for simulations.

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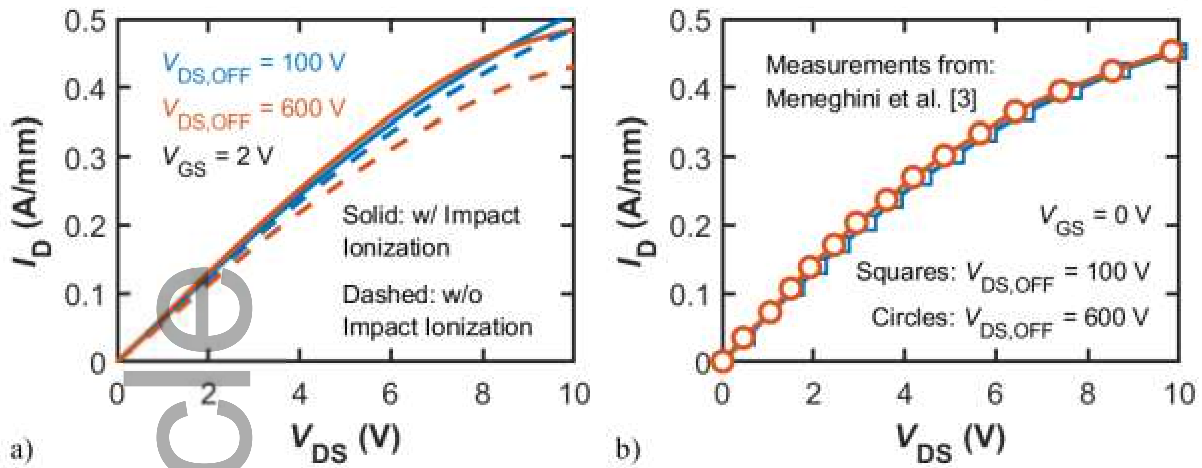

Figure 5. a) Simulated $I_D - V_{DS}$ curves taken at $V_{GS} = 2\ V$ for low ($V_{DS,OFF} = 100\ V$, blue curves) and high ($V_{DS,OFF} = 600\ V$, red curves) drain pre-stress in off-state ($V_{GS,OFF} = -5\ V$) held for 100 s. Solid (dashed) lines are simulations with (without) impact ionization activated. The drain current recovers for high stress only if the impact ionization is active, indicating less electron charge is trapped in the gate-to-drain access region. b) Comparison with measurement data taken from [3] shows a similar trend with respect to the simulation results.

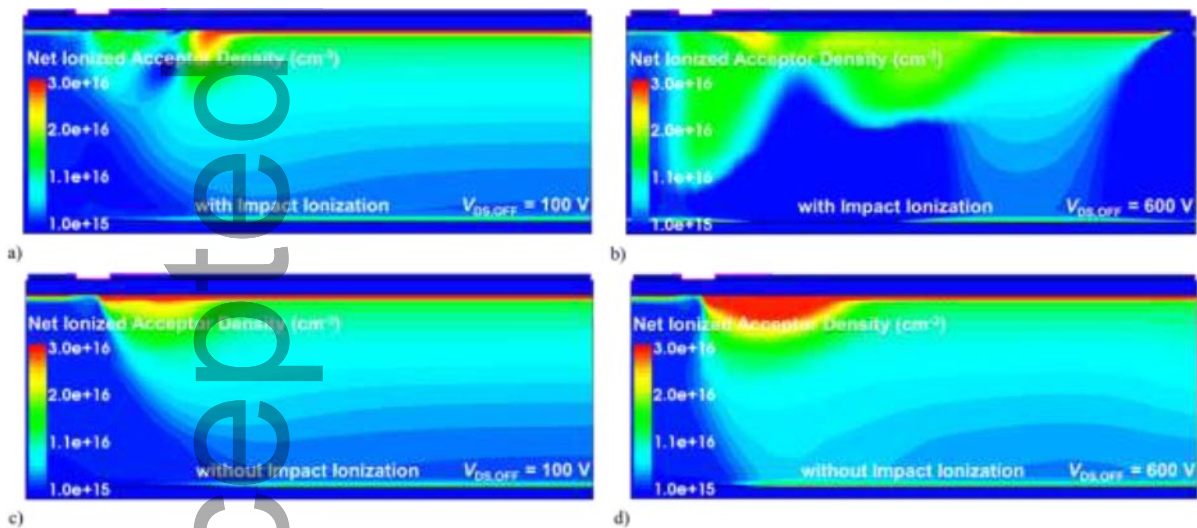

Figure 6. Contour plots of the net ionized acceptor trap density for the cases with (a, b) and without (c, d) impact ionization activated after 100 s of applied off-state stress with $V_{GS,OFF} = -5\ V$ and (a,c) $V_{DS,OFF} = 100\ V$, (b,d) $V_{DS,OFF} = 600\ V$. The scale of the legend is chosen to emphasize the difference in the buffer of the net ionized acceptor density (the maximum value actually exceeds this range).

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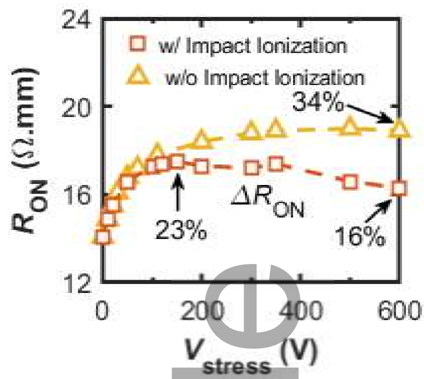

In this work, a carbon-related buffer-trap model for AlGaN/GaN HEMTs is developed by calibrating device simulations on static current-voltage characteristics and breakdown measurements. With this model, it is possible to explain the experimentally observed dynamic on-resistance recovery after off-state stress with hole generation and trapping in carbon-related deep acceptor states in the buffer.

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