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Halide Perovskite High-*k* Field Effect Transistors with Dynamically Reconfigurable Ambipolarity

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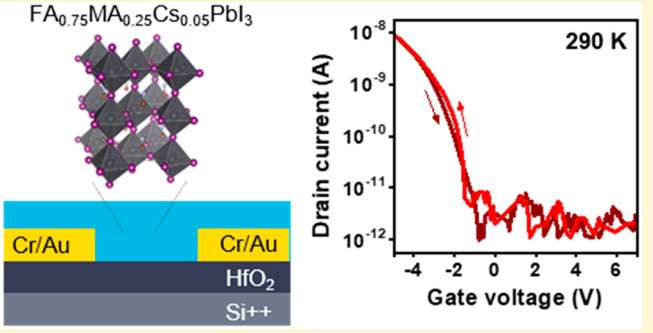
Supporting Information

ABSTRACT: Despite the remarkable optoelectronic properties of halide perovskites, achieving reproducible field effect transistor (FET) action in polycrystalline films at room temperature has been challenging and represents a fundamental bottleneck for understanding electronic charge transport in these materials. In this work, we report halide perovskite-based FET operation at room temperature with negligible hysteresis. Extensive measurements and device modeling reveal that incorporating high-*k* dielectrics enables modulation of the channel conductance. Furthermore, continuous bias cycling or resting allows dynamical reconfiguration of the FETs between p-type behavior and ambipolar FET with balanced electron and hole transport and an ON/OFF ratio up to 10^4 and negligible degradation in transport characteristics over 100 cycles. These results elucidate the path for achieving gate modulation in perovskite thin films and provide a platform to understand the interplay between the perovskite structure and external stimuli such as photons, fields, and functional substrates, which will lead to novel and emergent properties.



The field effect transistor (FET) is a fundamental component for realizing modern digital integrated circuits. It is also often utilized as a platform to evaluate lateral charge transport and (opto-)electronic transport properties in isotropic materials and for the investigation of new emergent properties by electrostatically doping the material, which are otherwise not easily accessible. Halide (or organic−inorganic) perovskites (HaP) have emerged as solution-processed semiconductors with outstanding properties for optoelectronics including low effective mass, high carrier mobility-lifetime product, weak exciton binding energy at room temperature, unusually high defect tolerance, and low trap density.[1−12] These characteristics have raised widespread interest in their exploration for optoelectronic devices, such as

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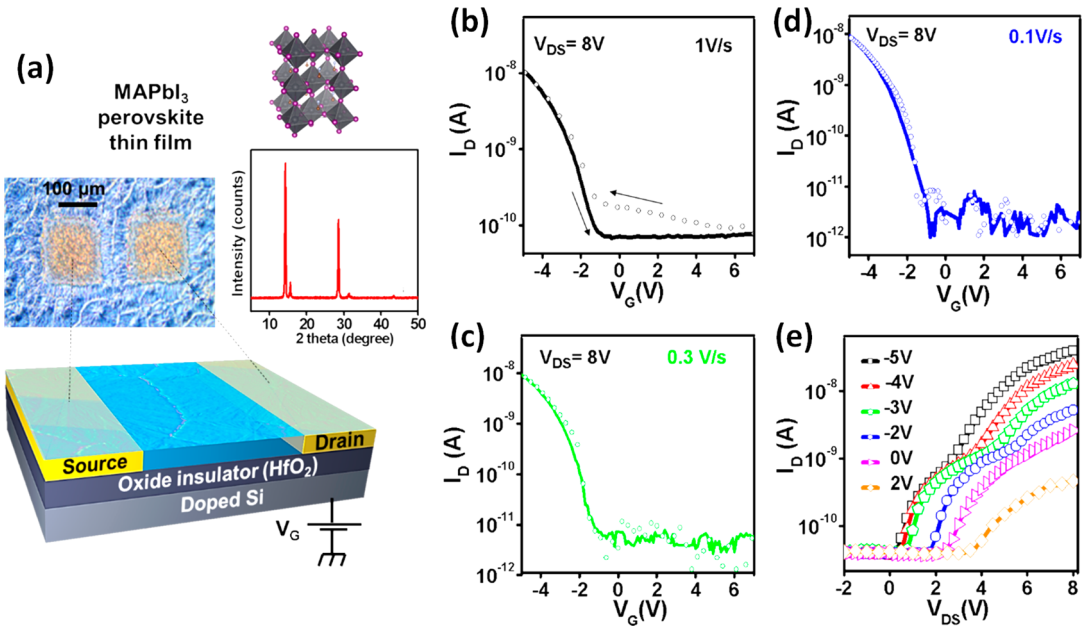

Figure 1. Characteristics of hybrid perovskite-based high-*k* field effect transistors. (a) Optical image of a typical 400 nm perovskite thin film spin coated onto a heavily doped silicon substrate with pre-patterned source and drain contacts (20 nm of Ti/180 nm of Au) separated by 70 μm and 100 μm wide. Here, a 30 nm layer of HfO_2 was used to insulate the films from the back gate. A single grain boundary is present in the conduction channel of the transistor. (inset) Structure and diffraction pattern of the main perovskite phase $MAPbI_3$. See details in Supplementary Figures 1 and 2. (b–d) Gate dependence of drain current (I_D–V_G) measured at different scan rates. Solid and symbol lines in the I_D–V_G curves illustrate the forward and reverse scans. (e) Current–voltage (I_D–V_{DS}) characteristics for different applied gate voltages measured at 1 V/s scan rate.

solar cells leading to high power conversion efficiency values exceeding 24%,[13−16] radiation detectors (gamma and X-rays), and optically pumped lasers.[7,17−22] Despite such unprecedented progress, several riddles remain to be solved including fundamental details of charge transport mechanisms in halide perovskite thin films.[10,23] Additionally, recent discoveries have highlighted the important role of external stimuli such as electromagnetic radiation and electric field on the structural dynamics,[11,23,24] which in turn strongly impacts the disorder and charge transport in hybrid perovskites. The dynamic nature of the material also provides opportunities to understand and unravel new physical phenomena that couple charge transport, structural dynamics, electric field, and light. FETs are an excellent platform for the elucidation of new physical properties such as electric-field-induced Rashba splitting and for the realization of novel perovskite devices, spin transistors, and in general gate-induced doping of the soft perovskite lattice.

While there have been some pioneering previous works on using 2D HaP as an active material for FETs,[25,26] there exist limited reports on 3D HaP-based FETs which attests to the challenges of building a FET that operates at room temperature (RT). Recent work on 3D HaP FETs is summarized below. Chin et al.[27] reported methylammonium lead triiodide ($MAPbI_3$) hybrid perovskite-based FETs that had to be operated at low temperature to overcome screening of carriers due to ionic impurities, which otherwise prevented FET operation at RT. Other reports on perovskite FETs have revealed a processing dependent n- or p-type doping of perovskites, thus making it difficult to probe the intrinsic properties and charge transport.[23,28] Moreover, halide perovskite-based FETs have also been reported to exhibit significant hysteresis in the current–voltage transfer characteristics during device operation, with rapid degradation, which can strongly compromise their transport properties.[27−30] Zeidell et al. shows that FETs with mobilities approaching 10 cm^2/V.s can be obtained by using a solvent vapor approach to passivate the grain boundaries in methylammonium lead iodide ($MAPbI_3$)-based HaP FETs. More recently, Yusoff et al. demonstrated ambipolar FETs using triple cation 3D perovskites, although the origin of ambipolarity was not described. Ambipolar FET behavior was also observed by Amassian and co-workers,[31] in FET devices made with few microns thick $MAPbI_3/Br_3$ single crystals. However, the observation of ambipolarity for a large-band-gap semiconductor (the perovskite bandgap is larger than 1.55 eV) with symmetric source and drain gold contacts is surprising for the choice of dielectrics (PMMA and SiO_2), as the applied gate field is not large enough to tune the Fermi energy across the large band gap and thereby switch from p- to n-type conduction. Moreover, in the work by Yusoff et al., the output characteristics appear to be anomalous, as they show a square-law drain current scaling with gate overdrive (typical of long channel FETs) for the p-type curves and, at the same time, a linear scaling (typical of short channel FETs) for the n-type curves. Such scaling typically spans different generations of FET technologies, and there is no discussion on the physical origin of these two coexisting behaviors. All of these recent reports on demonstrating a working 3D halide perovskite FET use a wide range of device designs and configurations, which further motivates the investigation of 3D HaP-based FET studies to understand the working mechanism. Furthermore, the near intrinsic doping density[4,6,32] ($\sim 10^{16}/cm^3$) should facilitate either p-type or n-type transport with the appropriate choice of metal contacts and therefore energy band alignment with respect to the valence or the conduction band. However, in most cases, interface traps pin the Fermi level and prevent

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Table 1. Performance of $MAPbI_3$ Perovskite FETs Using Different Oxide Layers[a]

oxide layer	ε	EOT (nm)	conductance (nA/V)	ON/OFF ratio	threshold field (V/cm)	hysteresis area (a.u.)
SiO_2	7.5	100	0.02	$\sim10^2$ (n-type)	3	1
Si_3N_4	3.9	52	0.05	10^2–10^3 (n-type)	1	0.4
HfO_2	23.5	5	4.90	10^2–10^4 (p-type)	0.5	0.1

[a]The I_D–V_G characteristics are plotted in Supplementary Figure 4. ε is the oxide layer dielectric constant, and EOT stands for the equivalent oxide thicknesses indicating the equivalent SiO_2 layer needed to produce the same effect as the high-k oxide materials.

the effective modulation of the conductance by means of a capacitively coupled gate electrode. Therefore, the ability to modulate the conductance in halide perovskites using an FET geometry remains a challenge depending on a carefully designed architecture. Moreover, there has been no report on using high-k dielectrics, such as hafnium oxide (HfO_2) or silicon nitride (Si_3N_4), for HaP FETs. Such a study is important for both the elucidation of the charge transport properties in complex perovskite device architectures and the discovery of novel and emergent physical phenomena, which may lead to multifunctional devices.

In this paper, we report halide perovskite-based FETs with good gate modulation at room temperature without the need of preconditioning steps such as light soaking. We demonstrate reproducible electrostatic gating with p-type modulation of the channel conductance with negligible hysteresis. Furthermore, a novel aspect of the FETs is that, after continuous bias cycling, the as fabricated p-type devices progressively transform into ambipolar FETs, where the perovskite Fermi energy can be successfully modulated by the gate voltage, allowing the balanced transport of both electrons and holes with greater than 4 orders of magnitude gate modulation in the channel conductance. Analysis with different dielectrics such as SiO_2, Si_3N_4, and HfO_2 reveals that the fundamental challenge for the demonstration of perovskite-based FET operation at RT is the screening of the gate electric field by ionic vacancies. Density functional theory simulations show that the $MAPbI_3/HfO_2$ interface corresponds to the ideal band alignment configuration for a gate/channel interface in a FET device. Through device characterization coupled with quantitative device modeling, we show that such effects can be overcome by combining high-quality perovskite thin films with high-k dielectrics, thus allowing for the complete inversion of the channel. Our results elucidate the demonstration of hybrid perovskite-based FETs, enabled by the presence of high-k dielectrics, and pave the path toward the understanding of transport mechanisms in hybrid perovskite-based FETs as a platform.

Results. *Perovskite-Based FET Operation at Room Temperature.* The FETs were fabricated using the architecture illustrated in Figure 1a where the main conduction channel is composed of methylammonium lead iodide ($MAPbI_3$) organic–inorganic (hybrid) perovskite. Briefly, we used the previously developed hot-casting method[5,33,34] to grow large grain-sized crystalline thin films (400 nm thick) on top of a heavily doped Si wafer with a 30 nm thick layer of hafnium oxide film (HfO_2, dielectric constant ~23, experimental details are given in Supplementary Note 1) and pre-evaporated gold contact electrodes. The characteristics of the FETs measured at RT and in the dark, are reported in Figure 1b–e at different DC bias. The gate voltage (V_G or gate bias) dependent drain current (I_D) shows field effect modulation with p-type behavior (Figure 1b–d); i.e., the FET turns ON only for negative V_G in the operating range of gate bias without failure of the device. To confirm that our devices are truly hysteresis-free, we measured the FET device performances as a function of V_G scan speed and observed that the forward and reverse gate bias scan overlap with one another (Figure 1b–d). The gate leakage current was dynamically monitored during the measurements and remained 2 orders of magnitude or more below the current when the channel is ON under the normal operating conditions, with an average value of about 30 pA (Supplementary Figure 1). The lack of hysteresis observed here for the large-grain thin films is consistent with previous results demonstrating that reducing the number of grain boundaries (here we have only one, Figure 1a) results in a reduction of ionic transient motions and hysteresis effects.[5,35] We verified the detrimental effect of grain boundaries by first studying the perovskite FET as a function of channel length (Supplementary Figure 2) which has a strong impact on the device performances. This is mainly due to the dimension of the channel length being strongly correlated to the number of grain boundaries across the channel, which results in higher charge decay rate inside the perovskite channel and thus lower device performances.

Second, we used a planar p-i-n junction architecture to measure the spatial distribution of the photocurrent and electroluminescence in the perovskite thin films (Supplementary Figure 3). We observe a dramatic reduction of both the photocurrent and electroluminescence at the grain boundaries as compared to inside the grain which can only be explained by defect-induced charge losses at boundaries, under the reasonable assumption that grains and grain boundaries have similar optical absorption.[4] Recent studies have also reported that ionic motion, which is believed to be at the origin of part of the hysteresis in perovskite solar cells, is enhanced at grain boundaries.[36,37] These results demonstrate that the presence of a single grain boundary in the conduction channel of our perovskite FET devices is advantageous to minimize hysteresis effects and to achieve the gate field effect at RT.

We attributed our ability to obtain reproducible thin-film perovskite FET devices operating at RT not only to the reduction of the number of grain boundaries in the conduction channel to one as discussed above but also to the use of a high dielectric constant material (the HfO_2 dielectric constant ε is 23.5) as an oxide insulator in our metal-oxide-FET architecture. Indeed, FETs using low dielectric constant materials such as SiO_2 ($\varepsilon \sim 3.9$) or Si_3N_4 ($\varepsilon \sim 7.5$) constantly yield devices with lower performances and larger hysteresis (Supplementary Figure 4 and Table 1). We observe both a smaller gate modulation of the current and an n-type FET characteristic for devices made with SiO_2 or Si_3N_4, suggesting that the technique used to deposit gate insulator may play an important role in terms of interface defects leading to a defect-induced carrier transport (details on the preparation of the FETs are given in Supplementary Tables 5–8).

Next, the current–voltage characteristics (I_D–V_{DS}) as a function of applied gate bias were measured (Figure 1e),

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exhibiting a typical exponential response,[38] which is indicative of a Schottky barrier in our FET. Consistent with the p-type behavior observed from the I_D-V_G characteristics described above (Figure 1b), I_D increases from 0.4 to 40 nA for gate bias varying between 2 and −5 V. Surprisingly, we observe a decrease of the turn-on voltage from about 3 to 0 V while reducing the applied gate bias from 2 to −5 V. This behavior indicates that the gate bias is able to modify the built-in voltage via electrostatic modulation of the doping of the perovskite layer. Specifically, the gate bias in the perovskite FETs can fully deplete the conduction channel by reducing and almost suppressing the charge doping at the barriers between the contacts and perovskite. In order to understand the results described in Figure 1, we performed extensive modeling using first-principles calculations and device modeling, which are described in Figure 2 and Figure 3, respectively.

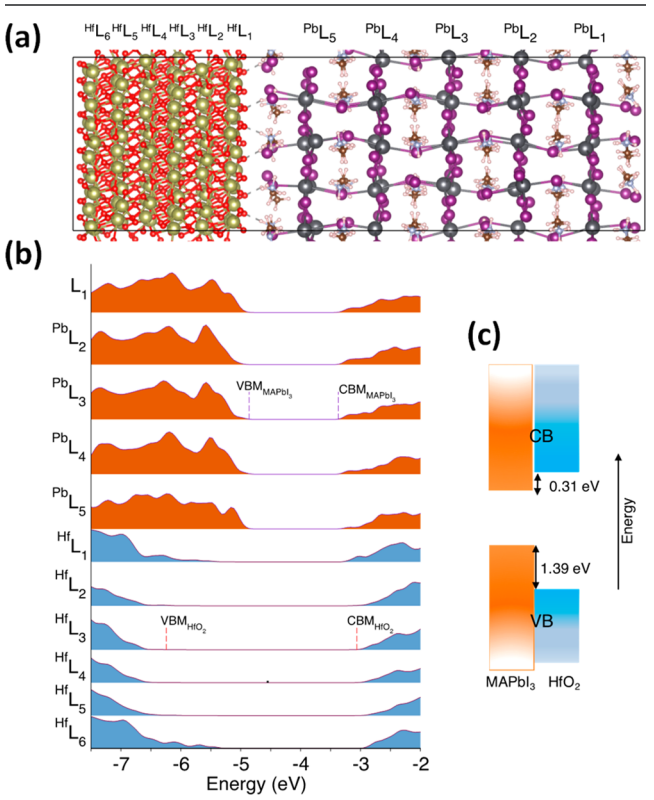

Figure 2. DFT modeling of the $MAPbI_3/HfO_2$ interface lattice structure. (a) Relaxed $MAPbI_3/HfO_2$ interface model from DFT calculations showing the labeling of the different layers. Here, Pb, I, Hf, O, N, C, and H are atoms depicted in dark, gray, purple, maroon, red, light blue, brown, and pale pink colors, respectively. (b) Layer-by-layer projected density of states (PDOS) of the relaxed interface model affording valence and conduction band alignments from the bulk-like parts of the $MAPbI_3$ and HfO_2. (c) Band alignment between $MAPbI_3$ and HfO_2 extracted from the PDOS shown in part b for the two bulk-like layers $^{Pb}L_3$ and $^{Hf}L_3$ for $MAPbI_3$ and HfO_2, respectively.

DFT Calculations Illustrating the $MAPbI_3/HfO_2$ Interface. A high-performance gate oxide in a FET device presents a very low-leakage current (*vide supra*), which requires high energy barriers for both holes and electrons across the gate/channel interface. These barriers are generally referred to as the valence band offset (VBO) and the conduction band offset (CBO) for holes and electrons, respectively. Hence, to compute these band offsets and thus gain a more fundamental understanding on the performance of the high-*k* dielectric as the gate oxide, we built a $MAPbI_3/HfO_2$ interface model and studied its properties using first-principles-based modeling.

The detailed procedure of the model construction along with the adopted computational approach are described in the Supporting Information (Supplementary note 3). Figure 2a shows the relaxed structure of the interface system with I atoms pointing to those of Hf at the interface region. Regarding the electronic structure of the system, the band edge states are formed by Pb−I states of $MAPbI_3$, while those of HfO_2 are either lower in energy at the valence band or higher at the conduction band (Supplementary Figure 6). From layer by layer resolved projected density of states (PDOS) shown in Figure 2b, we calculated the band offsets between $MAPbI_3$ and HfO_2. Here, VBO (CBO) is defined as the difference between VBM_{HfO_2} (CBM_{HfO_2}) and VBM_{MAPbI_3} (CBM_{MAPbI_3}) from their bulk-like layers,[39] which are emulated in Figure 2a by the two bulk-like layers $^{Pb}L_3$ and $^{Hf}L_3$ for $MAPbI_3$ and HfO_2, respectively. We calculated a VBO of 1.39 eV and a CBO 0.31, as summarized in the band diagram of Figure 2c. Interestingly, the latter corresponds to the ideal band alignment configuration for a gate/channel interface in a FET device and this is consistent with the improved FET characteristics measured with the $MAPbI_3/HfO_2$ interface. The calculated CBO presents a lower barrier as compared to VBO, which may hint to a possible electron tunneling across $MAPbI_3/HfO_2$. We stress, however, that our DFT calculations underestimate the calculated band gaps. The computations of proper many-body band gap corrections for both bulk materials and the $MAPbI_3/HfO_2$ superlattice (over 900 atoms) are computationally unaffordable. Hence, our calculated band offsets only yield a qualitative prediction, which highlight the suitability and performance of using HfO_2 as a gate dielectric in $MAPbI_3$-based FET devices.

FET Device Modeling. In order to validate the observed p-type FET behavior with Au as the source-drain electrode and further understand the underlying mechanisms of the perovskite FETs, we simulated the transfer characteristics (I_D-V_G) and analyzed the band diagrams of perovskite-based FETs using HfO_2 as a gate dielectric (Figure 3). Briefly, the numerical simulations involved the self-consistent finite element modeling of electron and hole transport in the two-dimensional device geometry, with appropriate potential barriers for the gate oxide as well as source drain contacts (see details of the numerical simulations in Supplementary Note 2 and Supplementary Tables 1−4). A single set of parameters allowed the $I-V$ characteristics to be predictably reproduced for a variety of device geometries (film thickness, source/drain separation, etc.), operating conditions (e.g., gate and drain voltages), and types of gate dielectrics (HfO_2, Si_3N_4, and so on). The analysis suggests that the key features of these transistors can be understood at the same level of sophistication as that of silicon MOSFETs.

The device structure implemented in the simulator is schematically represented in Figure 3a where the model device dimensions are also indicated (see also Supplementary Table 2). Figure 3b shows the I_D-V_G transfer characteristic for the device with a constant drain bias V_{DS} set to 6 V. The simulations predict a dominant hole current in the channel with device performance comparable to the experimental ones illustrated in Figure 1b. The I_D-V_{DS} output characteristics for

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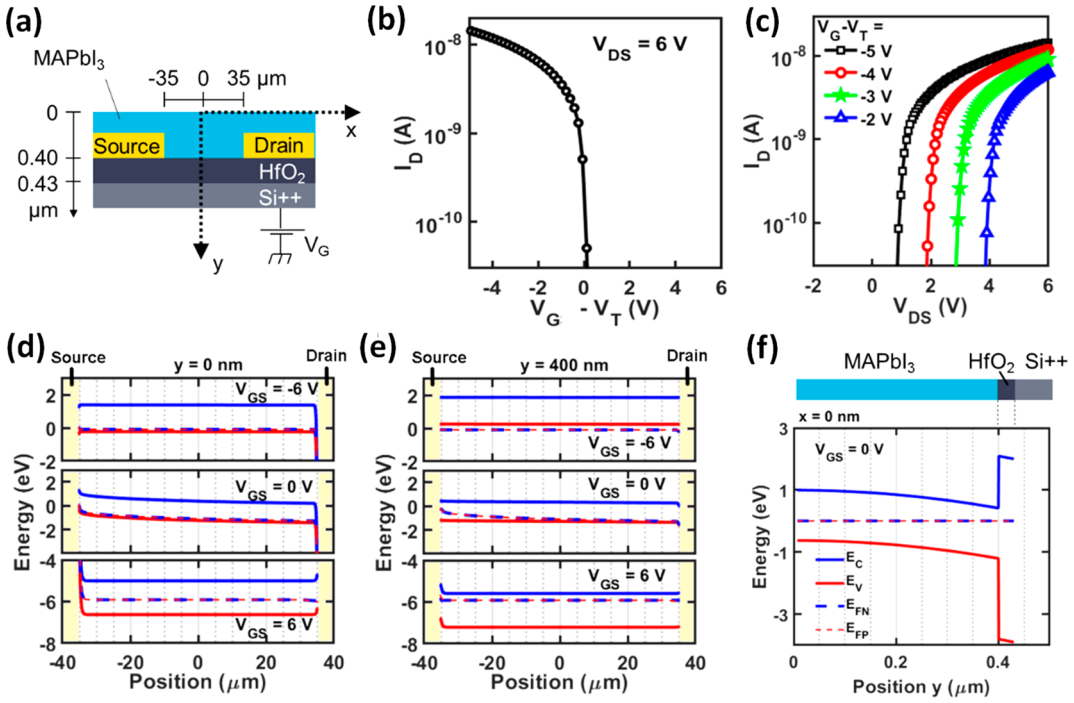

Figure 3. Device modeling of HaP field effect transistors fabricated using HfO_2 as a gate insulator layer. (a) Device schematic cross section implemented in the simulations. (b) Simulated I_D vs gate overdrive, i.e., V_G-V_T (with V_T being the threshold voltage). (c) Simulated output (I_D-V_{DS}) characteristics as a function of V_G. (d) Band diagrams in the $MaPbI_3$ close to the source and drain contacts (opposite side to the gate) for three different gate bias conditions. (e) Band diagram close to the interface between the perovskite and the HfO_2 layer. (f) Band diagram at equilibrium in the middle of the device. Details of the simulations and discussion of the results can be found in the Supporting Information. On the band diagrams, the notations are as follows: valence (E_V) and conduction (E_C) band edges and corresponding hole (E_{FP}) and electron (E_{FN}) quasi-Fermi energy levels.

the device with four different gate bias V_G values is illustrated in Figure 3c. The output characteristics are in agreement with the previous transfer characteristics (Figure 1e), predicting no considerable change in the device behavior because the gate bias values are all well below threshold.

To better understand the previous results, we analyzed the spatial distributions of the valence and conduction band edges as well as of the corresponding hole and electron quasi-Fermi energy levels (Figure 3d–f). Parts d and e of Figure 3 depict for three gate voltages the band diagrams along the source-drain direction at, respectively, the top and the bottom of the FET channel. We observe that the hole quasi-Fermi level is below or very close to the valence band edge at V_G set to −6 and 0 V. Conversely, when V_G is set to 6 V, the hole quasi-Fermi level is well above the valence band, thereby impeding the flow of holes in the channel. Although in this latter case the electron quasi-Fermi level is close to the conduction band edge, there is a relatively high Schottky barrier (about 0.6 eV) at the source contact which precludes the flow of electrons in the channel even at high positive gate bias. Figure 3f sketches the corresponding band diagram normal to the source-drain direction in the middle of the channel (vertical dashed line in the inset schematics of Figure 3f), crossing both the perovskite and oxide dielectric layer. We observe a decrease of the energy of the valence and conduction band edges by about 0.6 eV across the perovskite layer starting from the free surface. At the interface between the perovskite and oxide layer, we observe large barriers for both electrons and holes that prevent leakage, assuming an idealized situation with no ionic vacancies in the perovskite material at this interface (see discussion below). Given the relatively thin perovskite layer (400 nm), the gate can fully deplete the semiconductor (as shown in Figure 3f, for $V_{GS} = V_{DS} = 0$ V), as confirmed by the low free hole density (~10^7 cm^{-3}) compared to the doping (10^{16} cm^{-3}).

Our device simulations demonstrate that a high-k dielectric oxide layer such as HfO_2 is required to obtain perovskite-based FETs with a strong gate dependence for p-type carriers at room temperature, confirming the experimental results. We hypothesize that the key to obtaining such operational FETs using polycrystalline perovskite thin films is to reduce the screening of the gate electric field by charged ionic vacancies located supposedly at the interface between the perovskite and oxide dielectric which would otherwise hinder the complete inversion of the channel.

Dynamically Reconfigurable Perovskite FETs (Experiment). We experimentally tested the stability and reliability of the gate field effect in the perovskite FETs (HfO_2 as oxide insulator) described in Figure 1 by measuring the evolution of the I_D-V_G characteristics over several consecutive cycles of the gate bias (Figure 4). We observed that cycling the gate voltage several times from negative to positive and back to negative at a scan speed of 1 V/s resulted in a dramatic enhancement in the gate modulation for the n-type carriers. This operation resulted after 20 min in a transient I_D-V_G characteristic typical of ambipolar FETs with a negligible hysteresis and a comparable gate modulation for both the n- and p-type carriers (Figure 4a). As illustrated in Figure 4b, this transient effect provides control via the number of gate bias cycles over the modulation of the n-type carriers, i.e., the ON current and ON/OFF ratio. Interestingly, by resting the FET devices at zero gate bias for about 1 h, the original (before gate bias cycling) p-type behavior is recovered (Figure 4c). After that,

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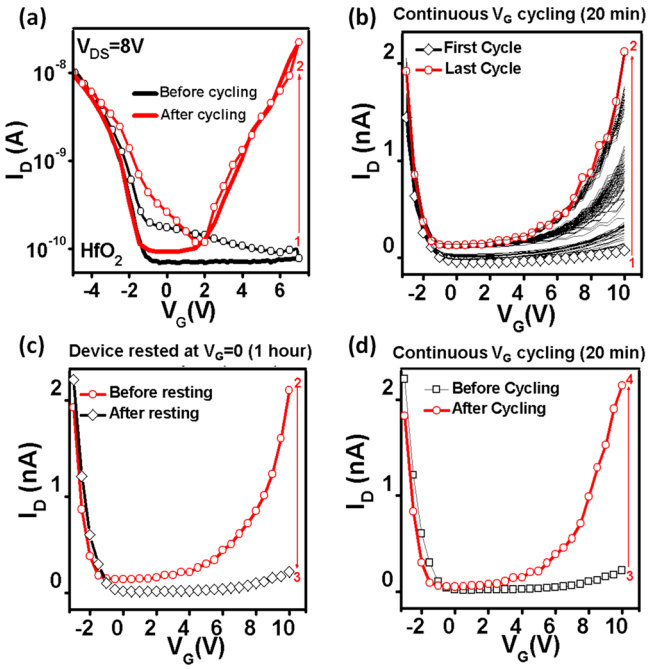

Figure 4. Dynamic reconfiguration between p-type and ambipolar operation in high-*k* $MAPbI_3$ perovskite FETs. (a) Transfer characteristics before (1. black line) and after 20 min of continuous gate voltage cycling (2. red line). V_G was scanned with a scan speed of 1 V/s. (b) Consecutive I_D-V_G cycles (forward direction) of lead iodide perovskite-based FETs performed continuously for 20 min. (c) Transfer characteristics of an ambipolar perovskite-based FET (2. symbol red line) after the device is rested at V_G = 1 V for 1 h (3. symbol black line). (d) Comparison of FET transfer characteristics after resting (3. symbol black line) and after a second 20 min long gate voltage continuous cycling at 1 V/s (4. symbol red line).

performing the gate bias cycling operation reproduced the progressive increase of the n-type gate modulation to reach after several minutes the same ambipolar behavior observed during the first cycling operation (Figure 4d). This unique and reversible reconfigurable behavior of FET operation via gate sweeping has not been reported in perovskite-based FETs and could pontentially be used for short-term, reconfigurable logic circuits, where the signals are dynamically reprogrammed.[40−42]

The remarkable reproducibility of this transient behavior suggests that it takes its origin in a dynamical effect in hybrid perovskites which can be activated by carrier doping in the dark. We hypothesize that the transformation from a p-type FET to an ambipolar FET after continuous gate voltage cycling results from local redistribution of the ions within the channels with gate bias cycling, which leads to the creation of stacks of n-type and p-type doped regions in the channel of the perovskite FETs. This is analogous to work by Dodabalapur et al.[43] which demonstrated a polarity tunable ambipolar FET by fabricating a channel with stacked p- and n-doped layers (achieved by using polymer and C_{60}). Another possibility involves changes in the energy diagram of the perovskite layer that modifies the contribution of n-type carriers during gate bias modulation. In the simulations, we have qualitatively reproduced the ambipolar behavior by considering possible electron tunneling from the source/drain contacts (see Supplementary Figure 6). While the exact mechanism for the observed ambipolarity is not clear, our simulations suggest that the redistribution of the electric field due to ion movement could enhance the field close to the contact and enhance the tunneling current from the source/drain contacts.

Finally, based on the understanding gained through our measurements (Figures 1−4), we proceed to demonstrate a high-performance FET operating at RT by replacing the $MAPbI_3$ with the recently discovered mixed cation perovskites, which exhibits higher intrinsic electronic conductivity.[11,14,44] We used a composition of $FA_{0.5}MA_{0.25}Cs_{0.25}PbI_3$ (details for the materials preparation and characteristics are given in Supplementary Note 1 and Supplementary Figure 5) as the active channel in FETs using HfO_2 as the gate insulator with the same device geometry as that illustrated in Figure 1a. The corresponding I_D-V_{DS} and I_D-V_G characteristics are shown in Figure 5a and b, where the measurements were performed after

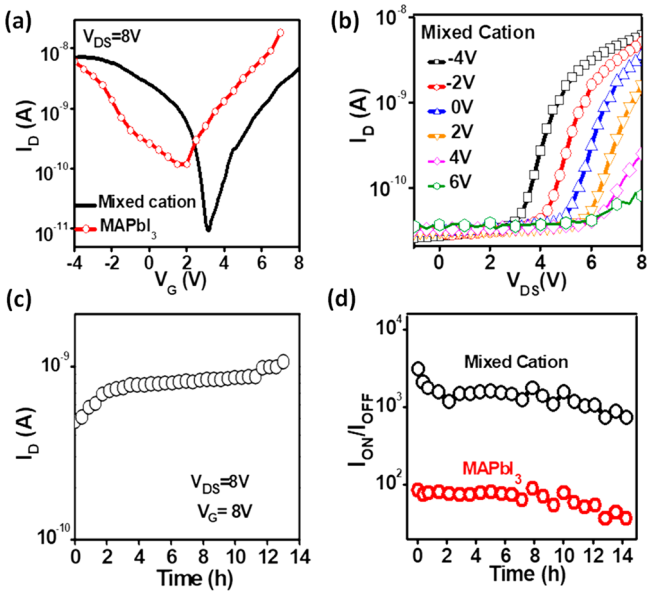

Figure 5. Performance and stability of mixed cation hybrid perovskite FETs using HfO_2 as a back gate oxide insulator. (a) Comparison of the transfer characteristics of FETs based on mixed cation perovskite and $MAPbI_3$. Measurements were acquired after continuous gate voltage cycling according to Figure 3. (b) I_D-V_{DS} output characteristics of FETs based on mixed cation perovskite. (c) Time evolution of I_D (measured at V_G = 8 V and V_{DS} = 8 V) in a mixed cation perovskite FET while the device is under continuous operation for 14 h. (d) Corresponding time evolution of the ON/OFF ratio.

gate bias cycling under the same conditions as those in Figure 4. In comparison with the $MAPbI_3$, the ON/OFF ratio is nearly 1 order of magnitude higher ($\sim 10^3$) in the mixed cation due to a significant reduction of the OFF current to about 10 pA. We also note an improvement in the mobility and subthreshold swing in the mixed-cation-based FETs as compared to their $MAPbI_3$ counterparts. We note that the overall mobility is still on the lower end of what has been reported, and we believe that this is probably related to the presence of traps at the interface of HfO_2/HaP. The I_D-V_{DS} characteristics at different applied gate bias values yield a typical diode behavior but with gate field dependent threshold voltage, analogous to $MAPbI_3$-based devices. We attribute the improvement of performances to the better film quality of the mixed cation perovskites as compared to $MAPbI_3$ (Supplementary Information Figure 5) and a reduction of the diode barriers.

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We also evaluated the reliability of both $MAPbI_3$ and $FA_{0.5}MA_{0.25}Cs_{0.25}PbI_3$-based perovskite FETs by scanning I_D-V_G characteristics continuously over 14 h. Parts c and d of Figure 5 show the time evolution of, respectively, the drain current at a fixed gate voltage (V_G = 8 V) and the ON/OFF current ratio, for both the $MAPbI_3$ and the mixed cation perovskite FETs. The results show that both types of FETs exhibit stable current output over 14 h with little degradation in the ON current and ON/OFF ration (factor of 4). These results are the first to address the long-standing problem of reliability and stability of hybrid perovskite-based FETs operating at room temperature.

In summary, we reported the first demonstration of a perovskite thin-film FET with strong gate dependence at room temperature and negligible hysteresis and good durability during the device operation. Moreover, we showed that persistent electrical cycling of the gate voltage leads to a FET, which can be dynamically reconfigured between p-type and ambipolar operation states. This behavior opens new opportunities for hybrid perovskite FETs toward applications in reprogrammable electronics including, for example, short- and mid-term memory devices. These devices exhibit a high (10^4) ON/OFF ratio and a charge carrier mobility of 10^{-3} $cm^2/V{\cdot}s$. Further improvements in the device figures of merit are expected to arise from improvements in the contacts and mitigating charge carrier scattering at the gate oxide/perovskite interface. These results pave the path for using perovskite-based FETs as a platform for the understanding and realization of new and emergent device concepts and for the elucidation of several predicted mechanisms that couple charge, lattice, electric field, and light.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsmaterialslett.9b00357.

Experimental details, details of the numerical simulations, and the detailed procedure of the model construction along with the adopted computational approach (PDF)

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Author Contributions

N.D.C. and N.Z. contributed equally to the work and will serve as joint first co-authors. A.D.M. conceived the idea, designed the experiments, analyzed the data, and co-wrote the manuscript along with J.-C.B and M.A.A. N.D.C., K.F., and F.L., performed FET device fabrication. H.B. performed photocurrent and electroluminescence under the supervision of J.-C.B. N.Z. performed device modeling simulations and analyzed simulation data with M.A.A., who conceived the device modeling and supervised the device modeling. B.T. constructed the DFT simulation model, performed and analyzed the calculations with the supervision of C.K. and J.E. R.R. and L.L.B. analyzed the data and supervised the project along with A.D.M. J.E. and M.G.K. discussed the results and provided inputs on the choice of material compositions along with H.T., W.N., and S.T. B.W.A. helped in optimizing the experiments and helped with analysis of the data. All authors have read the manuscript.

Notes

The authors declare no competing financial interest.
The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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