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A PV-Inspired Low-common-mode Dual Active Bridge Converter for Aerospace Applications

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***Abstract*—**

In the framework of the More Electric Aircraft, the use of isolated DC/DC power conversion for the electrical power distribution system is one of the most investigated solutions. If the DC/DC converter produces a variable common-mode voltage, leakage current can flow in the inter-winding parasitic capacitance of the high-frequency transformer, leading to insulation deterioration and early failure. This paper proposes to use modified H-bridge structures, already employed in the photovoltaic system for DC/AC power converters, to enable constant common-mode voltage for isolated DC/DC converters. The analysis shows that this solution can achieve the same efficiency as the conventional one, while simulations and experiments show a strong reduction of the common-mode current flowing through the transformer. A reliability analysis showed that the lifetime of the high-frequency transformer can be extended with the proposed solution.

I. Introduction

The More Electric Aircraft initiative aims at increasing the penetration of the electrical systems into the aircrafts, in order to decrease the weight and increase the overall efficiency and reliability. Already now, the newer aircrafts as the Boeing 787 and the Airbus A380, have an increased amount of electrical systems, and the tendency seems to be growing. If more power needs to be processed by electrical appliance, the need for power electronics converters increases as well [1].

Several DC/DC converters with galvanic isolation that could be interesting for the MEA were proposed. Among these, the Series Resonant Converter [2] allows obtaining very high efficiency at the price of a limited controllability, whereas the phase-shift full-bridge converter [3] is a bi-directional power converter with power control capabilities [4], [5]. The Dual Active Bridge (DAB) converter has attracted the interest of industry and academia because of the extended soft-switching operation and good power control. Its application to the aerospace field has already been proposed in several works [6]–[9].

An important requirement, that is peculiar of the aircrafts, is that the electrical equipment on-board should be grounded for safety reasons. Hard-grounding of the power bus is one of the possibilities to reduce the common-mode noise at the user interface [10]. However, as a common power ground exists, common-mode currents can flow between the converters, in a similar fashion to what happens in the low-voltage grids with the Terra-Terra (TT, doubly grounded) distribution system, where each converter shares the same ground [11]. These currents must be minimised as well, calling for low-common-mode power converters.

Since efficiency is one of the major concerns in todays converter design, different transformer structures and winding techniques were proposed in the literature for high-frequency transformers. The purpose is to limit the AC resistance of the windings, which is principally due to skin and proximity effects [12]–[14]. One of the most efficient solutions to limit the proximity effect is to realize the transformer with an interleaved primary and secondary structure. However, an extensive interleaved structure increases the inter-winding capacitance between the primary and the secondary of the transformer, exacerbating the EMI problem and increasing the circulation of common-mode currents. For a compact and very efficient structure, such as planar transformer, the primary- and the secondary-side inter-winding capacitances are very large due to the large winding area and short face-face distance.

The voltage across the turns, subjected to PWM converters, is not uniformly distributed. The high-frequency models of the coils show that step voltage impulses distribute exponentially among the turns and therefore the first ones, closer to transformer terminals, are subjected to higher voltage peaks [15]. If, for a winding design, the first turns are close to the negative terminal of the transformer, a maximum differential voltage is seen between them and the voltage stress is maximum. Furthermore, for aerospace applications subjected to pressure variations in function of the flight altitude, the Partial Discharge Inception Voltage (PDIV) decreases with the pressure drop [16]. Reducing the common-mode voltage variation between the transformer sides is a method to limit the detrimental effects of common-mode currents and lifetime degradation of the magnetics [17].

To reduce the common-mode voltage of power converters, in the recent years, many modifications of the H-bridge topology were proposed for DC/AC photovoltaic (PV) converters [11], [18]. The basic idea is to decouple the DC input and the AC output during the converter zero state; this can be done with additional switches in the DC side (like the H5 or H6 solutions) or a bi-directional switch in the AC side (Highly Efficient and Reliable Inverter Concept, HERIC). Marked reduction of the common-mode voltage was demonstrated both in academia and industry.

The scope of this paper is to investigate how these topologies, developed for non-isolated hard-switching DC/AC converters, behave when applied to isolated soft-switching DC/DC converters. Considering that the reflected secondary voltage at

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the primary side of the transformer is always lower than the primary voltage, employing a low common-mode topology as the primary side converter allows obtaining a constant common-mode voltage across the transformer. Since this paper focuses on the principle, only the H5, H6 and HERIC topologies will be analyzed, but the analysis can be extended to other topologies as well.

The paper is organized as follows. Section II describes the common-mode issue on aircrafts, Section III presents an analysis of the losses of the proposed power converter, Sections IV and V present the simulations and the experiments, Section VI discusses the reliability of the high-frequency transformer with the proposed solution and section VII draws the conclusions.

II. Common-mode Voltage Generation mechanism in the DAB

The DAB, whose schematic is shown in Fig. 1, is composed of two H-bridges driven by a PWM with 50 % duty-cycle. The phase-shifting between the resulting square waves at primary and secondary determines the power flow. The soft-switching operation of the DAB is however limited by the voltage ratio between the two ports and, in order to extend it, a dual-phase-shift modulation can be applied [19]. In this case, an additional phase-shift between the two legs of the primary or secondary side is introduced, allowing for further optimization. The dual-phase-shift technology is mature and well-accepted, as confirmed by a thriving literature and by the acceptance from industry. The soft-switching range extension and the efficiency improvements in the case of variable voltage ratio have already been demonstrated.

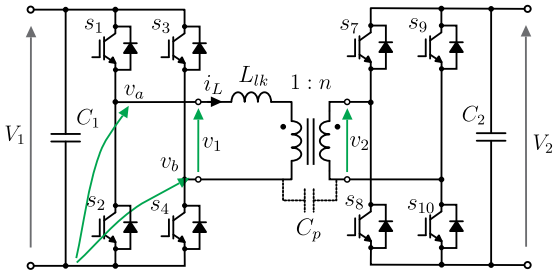
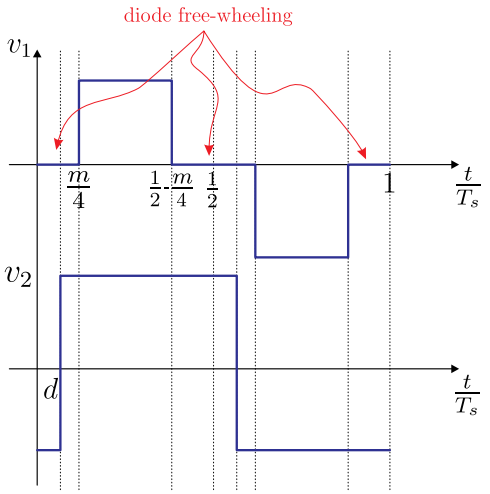


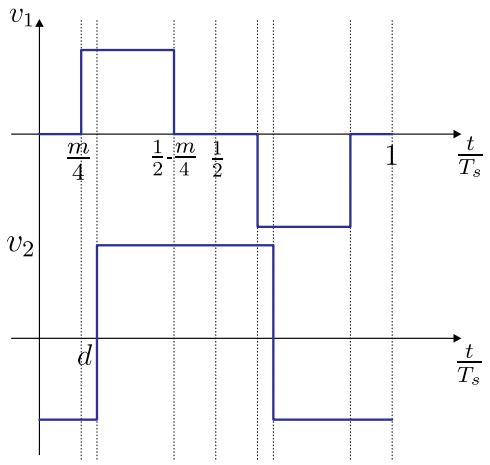
Fig. 1: Dual Active Bridge Converter.

Fig. 2 shows the idealized voltage waveforms for the dual-phase-shift modulation. d represents the normalized phase-shift of the secondary bridge, while the primary bridge is modulated by a three-level modulation, where the two legs have a normalized phase-shift of $m/2$. Two cases are possible, i.e. if the commutation of the secondary bridge happens before or after the commutation of the primary bridge.

A consequence of the dual-phase-shift modulation is a three-level waveform applied to the transformer. The third level is caused by the current free-wheeling on the upper or lower devices of the H-bridge. This operation is known to cause severe common-mode variations, that cause leakage current to flow through the windings parasitic capacitance, C_p, in Fig. 1.



(a)



(b)

Fig. 2: Primary and secondary voltage waveforms for the DAB converter with dual-phase-shift modulation. Case when $d < m/4$ (a) and case when $d > m/4$ (b).

In fact, the inter-winding capacitance provides a low-impedance path at high frequency between the primary and secondary windings; as a result, it deteriorates the system EMI performance [20]. Transformer shielding is a widely-adopted common-mode noise reduction technique in isolated power converters [21]. It limits the common-mode noise by reducing the effective parasitic capacitances associated with the most severe voltage pulsating nodes. However, inserting shielding layers in a transformer introduces additional power loss, and it is not practical in some applications like fully interleaved transformer winding structure, since too many shielding layers are needed.

Fig. 3 shows an equivalent schematic of the DAB, where the H-bridge is modeled as a common-mode voltage source v_{cmi} and a differential mode voltage source v_{di}. For the power transfer, only the differential mode voltage is relevant, however, because of the parasitic capacitance C_p of the transformer, common-mode current, $i_{cm} = C_p \frac{v_{cm}}{dt}$, can flow through the

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common ground. Minimizing the high frequency common-mode voltage variation over the transformer decreases the common-mode current.

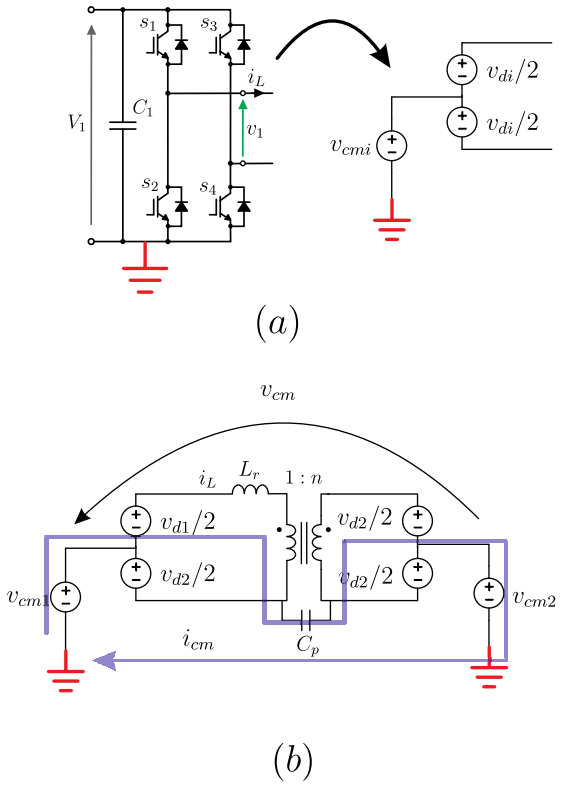

Fig. 3: Power electronics converters with a common ground allow the circulation of common-mode currents through the aircraft's chassis. (a) equivalent circuit of the H bridge, (b) equivalent circuit of the DAB converter.

III. Losses Analysis

A theoretical analysis is carried out for the DAB operated with the dual-phase-shift modulation.

Appendix I presents the equations that describe the behavior of the inductor current during each phase for the two cases. Depending on the topology chosen (H4, H6 or HERIC), the conduction and switching losses will concern different devices. In order to correctly estimate the semiconductors losses, the modulation strategies will be analyzed in the following. Figure 4 shows the schematic of the transformerless topologies under investigation.

Fig. 5 shows a typical case of the dual-phase-shift modulation as well as the commutation signals of the H6 and HERIC converters. H5 behaves very similarly to H6, except for the fact that only the high-side free-wheeling is present.

Fig. 5a shows the commutation sequence for the H6 modulation. The topology and the current flow are exemplified above the commutation signals. Assuming a positive current direction, at $t = \frac{T_s}{2} - \frac{mT_s}{4}$, the DC decoupling device s_5 turns off with hard-switching, while s_4 turns off at zero current. At $t = \frac{T_s}{2} + \frac{mT_s}{4}$, switch s_1 turns off with hard-switching. With this choice, one commutation affects s_5 and another commutation affects s_1. If s_5 was switched off after s_4, no switching losses would occur in the decoupling devices. Choosing which device to switch off earlier allows choosing which device will experience the switching loss.

Fig. 5b shows a possible sequence to commutate the HERIC converter. The basic idea would be to switch off s_1 and s_4 at $t = \frac{T_s}{2} - \frac{mT_s}{4}$ and then to switch on simultaneously s_5 and s_6 after a dead-time to avoid the leg short-circuit. This choice, however, would imply a bipolar waveform at the output of the bridge and more switching losses. If the devices s_5 and s_6 can be gated independently, shortly before $t = \frac{T_s}{2} - \frac{mT_s}{4}$, s_6 is switched on (the diode in parallel to s_5 prevents the leg short-circuit), so that when s_1 and s_4 are switched off (hard-switching), the current flows through s_6 and the diode of s_5. In the same way, at $t = \frac{T_s}{2} + \frac{mT_s}{4}$ switching off s_5 and s_6 (hard-switching), the diodes s_2 and s_3 carry the current. The devices can be then switched on at zero voltage.

The losses of the various topologies were calculated for different values of the phase-shift and of the voltage ratio only for the primary side converter, since the behavior of the secondary side is not affected. The simplification to use $m = 1 - \frac{nV_2}{V1}$ to guarantee the volt-second balance at primary and secondary sides is done. More complex choices of m can be performed, and they do not affect the equations in Appendix I. Fig. 6 shows switching and conduction losses for the system operating with V_1 = 270 V, V_2= 28 V for unity voltage ratio, f_s = 24 kHz. The selection of the inductance is an important parameter and determines the overall reactive current circulation. To be consistent with the simulations and the experiments, a value of 160 uH was chosen. The thermal characteristics of the SiC MOSFET C2M0040120D by Wolfspeed were taken from the data-sheet of the component. The full-bridge (H4) converter is added for reference.

The loss calculation takes into account the resistive behavior of the MOSFETS, and it is performed by calculating the RMS current through the individual switches and the typical value of the on-state resistance. It is assumed that, during the reverse conduction stage, the MOSFET is still gated, so the current is flowing through the channel. The body-diode of the device is carrying the current only during the dead-times. This choice leads to an underestimation of the conduction losses, especially at low current, since the on-state voltage of the SiC diode is much higher than the channel conduction.

The switching losses are calculated from the off energy taken from the data-sheet (the on-energy is neglected, since it is assumed that the converter operates under soft-switching condition) and are linearly scaled depending on the switching current and voltage.

From the analysis it can be seen that there are points of operation where the switching losses of the bridge devices (for H6) or the AC devices (for HERIC) are very low, because of the particular shape of the current. With a particular choice of the modulation, the switching losses for the DC devices of the H6 could be also set to zero.

Fig. 7 shows the overall losses for the H6 and HERIC topology (H4 losses are theoretically the same as HERIC), showing that H6 is always less efficient than HERIC, however the difference is lower at lower voltage ratios, because of the lower conduction losses of the DC devices. Nevertheless, the

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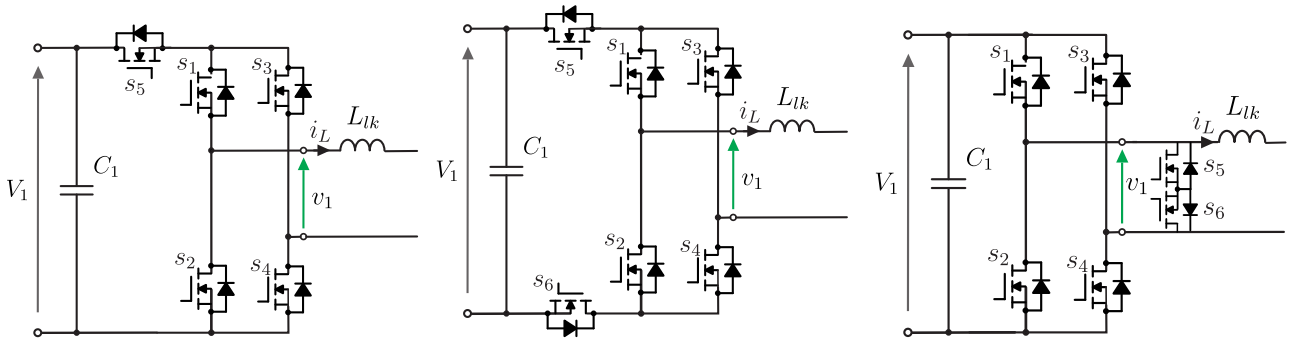

(a) H5 Topology. (b) H6 Topology. (c) HERIC Topology.

Fig. 4: H-bridge topologies with reduced common-mode voltage.

H6 topology presents the important advantage to have two additional switches in series, making it more resilient in the case of a spurious turn-on or device failure. The short-circuit failure is considered to be the most severe, since it must be detected very fast and the current must be interrupted before the converter is destroyed due to DC link short-circuit. A failure in the decoupling devices deteriorates the common-mode performance but keeps the converter operational and the presence of four devices in series increases the chance to interrupt the short-circuit current in the case of a failure in one of the H-bridge devices. This is particularly relevant for aircraft applications, where the components are more exposed to cosmic rays. A charged particle hitting the semiconductor junction can generate enough energy to cause a spurious turn-on or to damage the device. In this context, having a topology that increases the fault handling in case of a short-circuited devices can be the main criterion.

IV. Simulation results

Simulations were carried on with Simulink/PLECS software, with the same parameters as the losses analysis. The goal is to highlight the operation of the reduced common-mode architectures. The H4 will be compared against the HERIC, and the results for different parameters are shown in Fig. 8 and Fig. 9. In Fig. 8 the condition is close to the theoretical minimum losses for the AC switch of the HERIC converter, as can be seen, $i_L\left(\frac{T_s}{2}-\frac{mT_s}{4}\right)$ is close to zero. It is also evident that the common-mode voltage offered by the HERIC solution is constant. Fig. 9 shows a condition where the H-bridge is operated very close to a square wave, even for the H4 converter, the amplitude of the pulses of the common-mode voltage is small. In this condition, because of the almost trapezoidal current of the inductor, the switching losses of the AC switches and of the H-bridge are almost equal.

The losses in all the components of the converter are analyzed to show how they are distributed and which efficiencies could be achieved. For the low-voltage stage, the Silicon MOSFETs IRFP4368PbF are considered. The parameters of the transformer regarding the copper and core losses are taken from the data-sheet of the manufacturer A value of 0.05 Ohm is considered for the external inductor. It is assumed that the copper losses of the transformer are equally shared between primary and secondary windings (primary winding resistance 0.075 Ohm) and that the core losses are constant at 5 W.

Fig. 10 shows the loss breakdown at the different operating points. At low power, the core losses are quite significant. The trend that can be observed is that the losses in the magnetic components and the LV stage contribute to the majority of the losses when the power is increased.

This would lead to an efficiency higher than 97 % in some operating points.

V. Experimental Results

In order to test the capability of the reduced common-mode topology to improve the DAB converter with dual-phase-shift modulation, a prototype of a DAB for aerospace applications [6] was modified with a bi-directional switch to re-configure it as a HERIC converter, see Fig. 11. The devices chosen for the prototype are the same as the ones considered in the simulation results, for the tests, a reduced power up to 650 W was considered.

E-core shape (shell type) or U-core shape (core type) could be adopted for the design. On the one hand, the core type has a better window utilization, reaching higher isolation requirements and reducing the partial discharge issues. On the other hand, the shell type can reach very small leakage inductance, which is very advantageous for the efficiency point of view. Note that Litz wires were used to reduce the skin effect.

For the prototype transformer implementation, the core type was selected, where the U-core (UI 93/104/30) was used. The choice of the U-core is preferred for application with high insulation voltage and low parasitic capacitance, for the low-common-mode converter of this paper an E-shape foil transformer would be preferred . The choice of the U-core is for the sake of simplicity, because the design and optimization of a high-efficiency transformer is outside the scope of this work. The transformer has a leakage inductance of 10 μH (seen by the primary side), an external inductance of 150 uH was added. The transformer turns ratio is $n_{DAB} = 0.1037$ and the switching frequency is 24 kHz, to be consistent with the analysis.

Fig. 12 shows the steady-state waveforms of the HERIC converter under different voltage transfer ration (output 28

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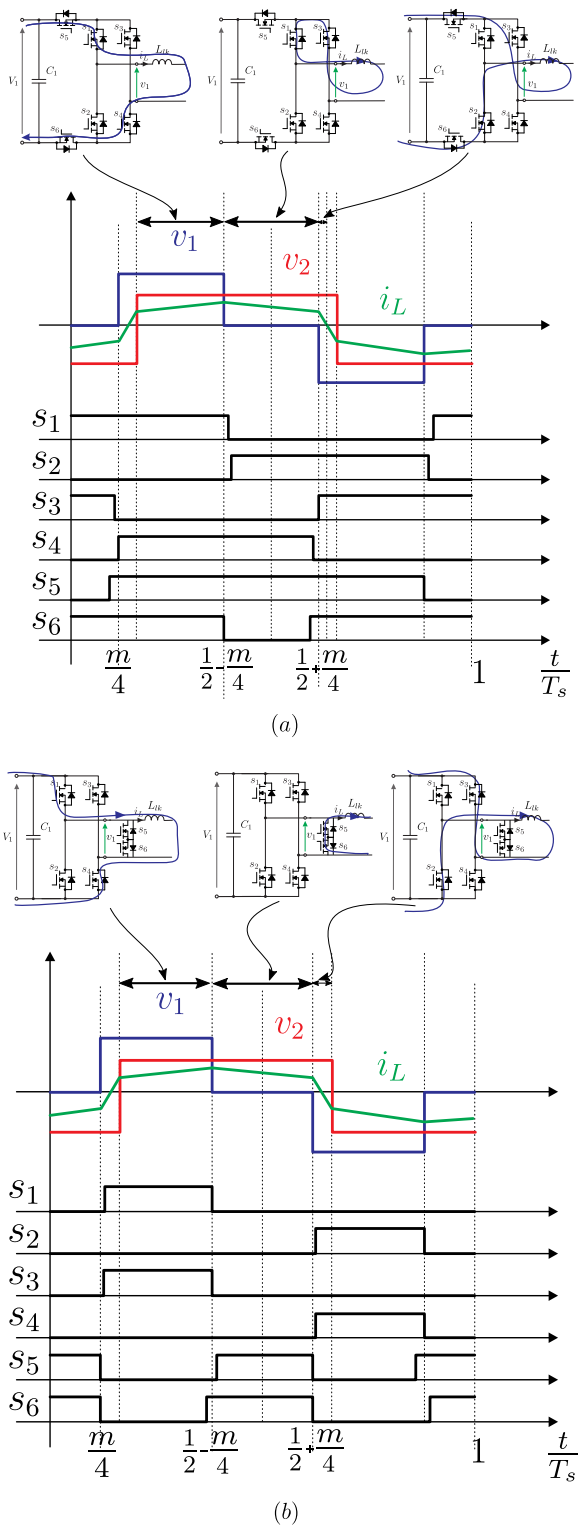

Fig. 5: Commutation sequence for the H6 (a) and HERIC (b) converters.

V (a) and 25V (b)), showing the excellent agreement with the simulations. Fig. 13 shows the output voltages of the H-bridge legs referred to the negative power supply and the common-mode voltage when the HERIC switch is disabled (a) and enabled (b). As expected, the common-mode voltage is basically flat. Differently from the simulations, where the devices performed ideal commutations and presented no parasitic elements, in the experiments a small common-mode voltage variation happens. This phenomenon is the same behavior of a bipolar H-bridge performing non-ideal commutations in a PV inverter: a small common-mode current flows [11]. This problem can be addressed via a careful optimization of the circuit layout and the equalization of the pulse times. In fact, when the signal is transmitted via optic fibers, different propagation times in the turn-on/off of the optic fiber cause a small mismatch of the gate signal. Although it generates common-mode current (and EMI), it does not generate high dv/dt common-mode variations that deteriorate the insulation.

Fig. 14 shows the current of a 1 nF capacitor (C_p in Fig. 3b) connected between primary and secondary side of the transformer recorded with the oscilloscope Lecroy HDO6054. Fig. 14a shows the DAB solution (rms value 160 mA) and Fig. 14b shows the HERIC solution (rms value 72 mA). Although the chosen value may seem high for conventional transformer (where the capacitance is kept in the range 100-500 pF), some very optimized foil transformer can have much higher value, like 3.8 nF like in [22].

Due to limitations of the power circuit used to implement the bidirectional switch, the switches s_5 and s_6 have to be gated simultaneously, causing a bi-polar voltage at the primary side. This is acceptable, since the target of the demonstrator is not to achieve a high efficiency but to show the potential common-mode reduction of the modified DAB. The efficiency of the converter, normalized to the reference power 650 W, is shown in Fig. 15, where several cases are analyzed. The DAB operating with single-phase-shift with m = 0 shows overall very good performance, reaching a peak efficiency of 95.5 % and it is used as benchmark. For the sake of completeness, it is worth noting that the optimized commutation sequence implies changing the turn on/off instants of the devices depending on the expected current polarity. For hard-switching PV converter, the switching frequency is rather low (in the order of 10 kHz) and the current is at the same frequency of the grid. In these conditions, realizing the optimized strategy presents no difficulties. For soft-switching applications, the current changes polarity at each PWM period, meaning that the turn on/off instants must be re-calculated twice each period. Considering that the switching frequency of a DC/DC converter is normally higher than the one of a grid-connected converter, this means that the duty cycle calculation must be performed in the range of 50-100 kHz, implying in a more difficult programming of the microcontroller (multiple interrupts) or the use of dedicated devices (FPGA, CPLD, System on Chip) for the implementation of the modulator.

If the voltage ratio is changed but the DAB is still modulated with the single-phase-shift control, the efficiency is seriously deteriorated, especially at lower output power, because of the increased reactive power circulation. As already demonstrated in literature, the simple dual-phase-shift control by employing m = 0.1 allows improving the efficiency, reaching the values of the single-phase-shift control under unity transfer ratio. The HERIC solution, as expected because of the gate driving limitation, implies additional switching losses, because the impossibility to realize the optimize switching strategy. Nev-

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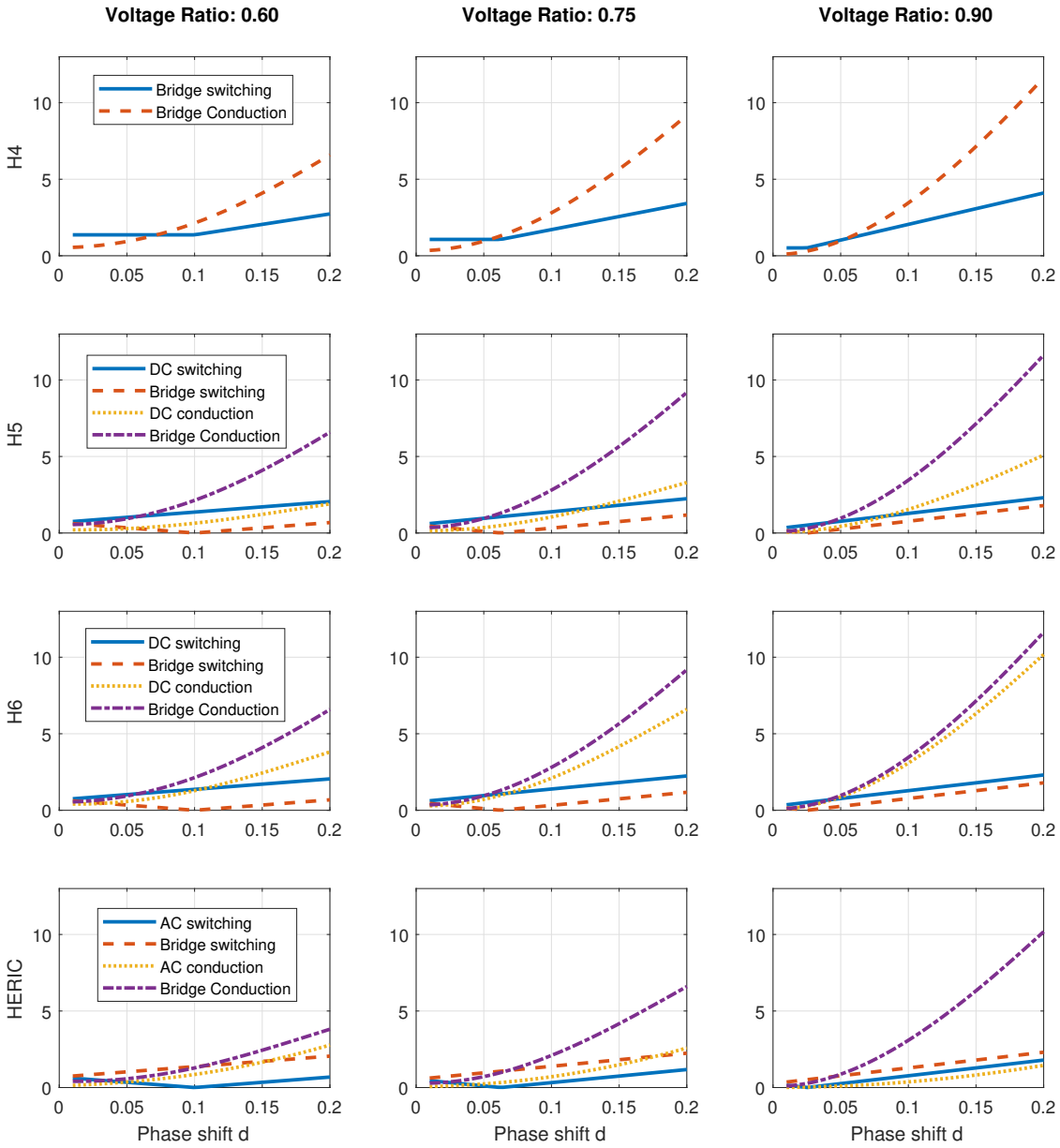

Fig. 6: Switching and conduction losses for the different topologies divided among the switches.

ertheless, the efficiency at lower power is almost unaffected, while for higher power a maximum difference of 0.9 % was noticed.

The discrepancy between the experiments and the theoretical efficiency calculation is due to multiple causes. The first one is the body-diode conduction loss during the dead-time (1 us for the primary side and 2 us for the secondary side), that increases the on-state semiconductor losses. The LV MOSFETS gate resistance was chosen to be 10 Ohm, greater than the 2.7 Ohm used for the tests performed in the data-sheet, this accounts for an increased switching losses in the secondary bridge. When d $<$ m/4, the secondary bridge theoretically commutates at zero current. Difference in the parameters could, however, shift this point, causing the loss of soft-switching in the secondary bridge. A modification of the dual-phase-shift modulation that forces the secondary current to be greater than zero could be implemented to solve this drawback.

The non-optimized layout is anyway responsible for increase turn-off losses because of the voltage overshoot during the commutation process. The capacitor losses are neglected, and they can be relevant especially for the LV side, where the current is higher. The high current ripple in the capacitors is a well-known drawback of the DAB converter. Finally,

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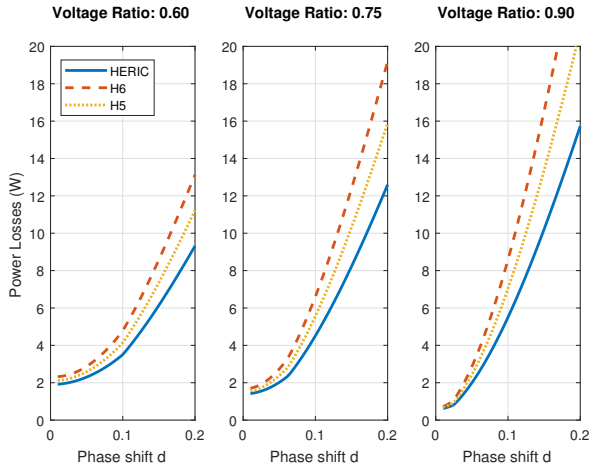


Fig. 7: Overall losses for the primary side comparison for the different topologies.

additional resistive losses in the LV side are present because of the cabling and of the PCB. As typical of HV/LV applications, most of the losses are focused on the LV-stage, improvement in terms of layout and of the LV capacitor banks are envisaged to reach high efficiency. The usage of LV GaN semiconductors can also be improved to boost significantly the efficiency.

VI. Effects of Common-Mode Voltage on the Transformer Lifetime

In this section, the impact on the transformer lifetime due to the common-mode voltage reduction is evaluated based on existing lifetime models. It has been empirically observed that, over a restricted time scale the lifetime t of many dielectrics subjected to high field E varies according to the so called, inverse power law:

$$t = CE^{-n} \tag{1}$$

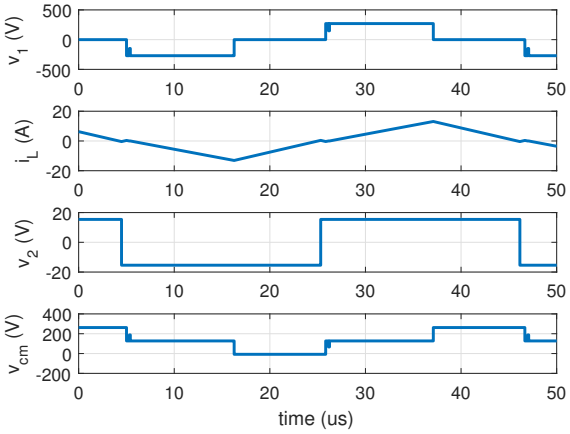
where C and n are adjustable parameters varying with the experimental conditions. In this original form the lifetime of dielectrics seems to be not correlated with the frequency of the applied voltage. Nevertheless, it has also been observed and verified in real applications that transformers or electrical motors subject to high-frequency supply voltage present shorter lifetimes, thus a more comprehensive formulation of the law is given in (2).

$$t = CE^{-n}f^{-x} \tag{2}$$

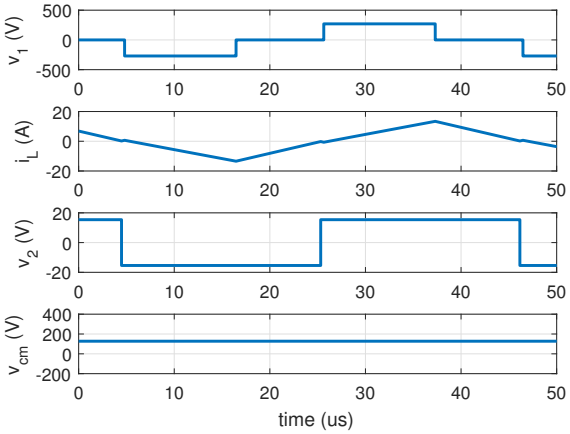
where x is a constant and it is speculated that the failure mechanism does not change with frequency [23]. The expression can be also given by

$$\frac{L_E}{L_0} = \left(\frac{E}{E_0}\right)^{-n} \cdot \left(\frac{f}{f_0}\right)^{-x} \tag{3}$$

where E_0 and f_0 are the values of electrical stress amplitude and frequency below which electrical aging can be neglected and failure is the consequence of aging produced by the other stresses; L_0 is life for $E = E_0$ and $f = f_0$, whereas L_E is the



(a) H4.



(b) HERIC.

Fig. 8: Simulation results: d = 0.1, m = 0.45.

lifetime under the actual conditions. Considering the separated action of the differential and the common-mode voltages, the lifetime can be estimated considering a multi-stress model as in [24]. When simultaneous stress are applied, they normally produce a degradation effect which is far greater than the one obtained by the sum of the single aging rates, but slightly lower than the one derived by a simple multiplicative law. The total lifetime, valid for N simultaneously applied stresses, can be given in (4)

$$\frac{L}{L_0} = \frac{L_1}{L_0}\frac{L_2}{L_0}...\frac{L_N}{L_0}G(S_1, S_2, ...S_N) \tag{4}$$

where L is the multi stress lifetime, $L_1 \ldots L_N$ are single-stress lives for stress $S_1, \ldots S_N$, respectively, L_0 is the reference life in the absence of any stress producing aging, and $G(S_1, S_2, ...S_N)$ is the correction function. Considering the action of the differential common-mode voltage, the law in (4) can be written as in (5)

$$\frac{L}{L_0} = \frac{L_{Ed}}{L_0}\frac{L_{Ecm}}{L_0}G(E_d, E_{cm}) \tag{5}$$

according to the compatibility conditions $L/L_0 = L_{Ed}/L_0$, for $E_{cm} = E_0$ ($L_{Ecm} = L_0$) and $L/L_0 = L_{cm}/L_0$, for $E_d =$

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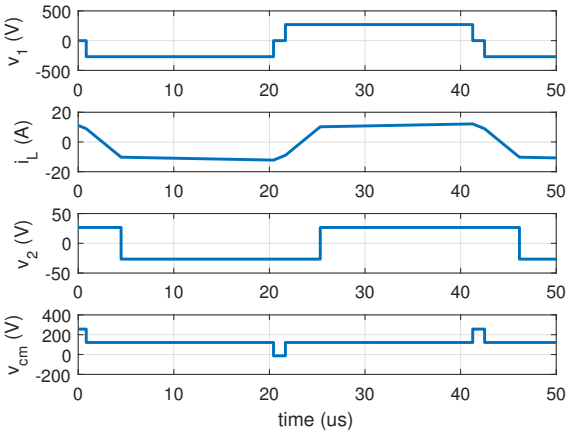
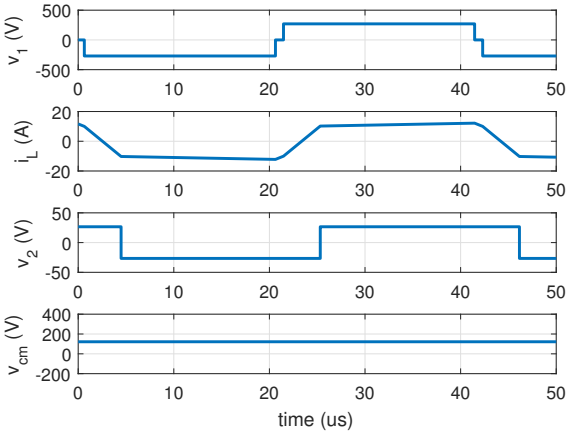


(a) H4.



(b) HERIC.

Fig. 9: Simulation results: d = 0.1, m = 0.05.

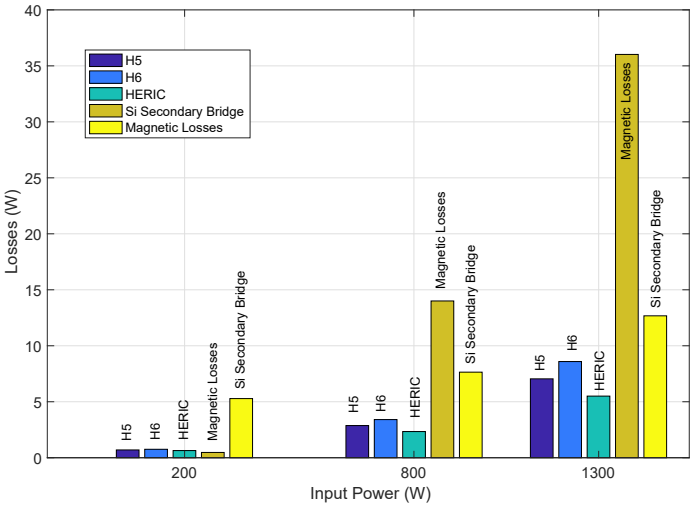


Fig. 10: Loss breakdown for the different solutions when m = 0.1 and V_2 = 25 V.

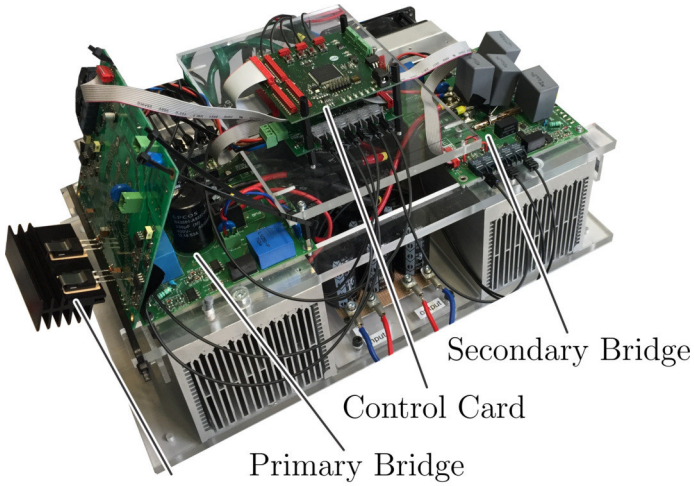


Fig. 11: Picture of the experimental prototype.

E_0, ($L_{Ed} = L_0$); thus, $G = 1$ in both cases. The simplest expression for $G(E_d, E_{cm})$ which satisfy the above conditions is

$$G(E_d, E_{cm}) = \left(\frac{E_d}{E_0}\right)^{b\left(1-\frac{E_0}{E_{cm}}\right)} \tag{6}$$

where b is a constant that depends on the application. Considering a conventional H4 topology, when the converter operates, both differential and common-mode voltage can be measured at the inverter output. Therefore, the lifetime will depend on the joint action of E_d and E_{cm}. Considering E_d and E_{cm} of equal values in amplitude and frequency and combining (3), (5), (6), the expression for L/L_0 is given in (7).

$$\frac{L}{L_0} = \left(\frac{E_d \cdot E_{cm}}{E_0^2}\right)^{-n} \cdot \left(\frac{f_d \cdot f_{cm}}{f_0^2}\right)^{-x} \cdot \left(\frac{E_d}{E_0}\right)^{b\left(1-\frac{E_0}{E_{cm}}\right)} \tag{7}$$

In case of HERIC solution, the action of E_{cm} can be neglected as the aging depends only by the differential field.

$$\frac{L}{L_0} = \left(\frac{E_d}{E_0}\right)^{-n} \cdot \left(\frac{f_d}{f_0}\right)^{-x} \tag{8}$$

Considering for n, x and b the values in [25] it is possible to compare the lifetime improvement estimation of the transformer in case of a constant common-mode voltage during converter operation. From Fig. 16, for a electrical stress with amplitude from E_0 to twice E_0 and frequency from f_0 to $2f_0$, the lifetime improvement of the transformer, due to the adoption of HERIC topology instead conventional H4, reaches a peak of 25% and it is well above 10% for the whole considered interval.

Since the lifetime estimation is strictly dependent on the n and x parameters in (5), a sensitivity analysis is performed. Fig. 17 shows the results in case of $E_{cm}/E_0 = E_d/E_0 = 1.3$ and $f/f_0 = 1.3$, fair values for wide-bandgap device applications. The improvement in the transformer lifetime remains high also in case of a large variation of n and x.

VII. Conclusion

This paper proposes to use a H-bridge modified as done in PV inverters to implement a Dual Active Bridge with

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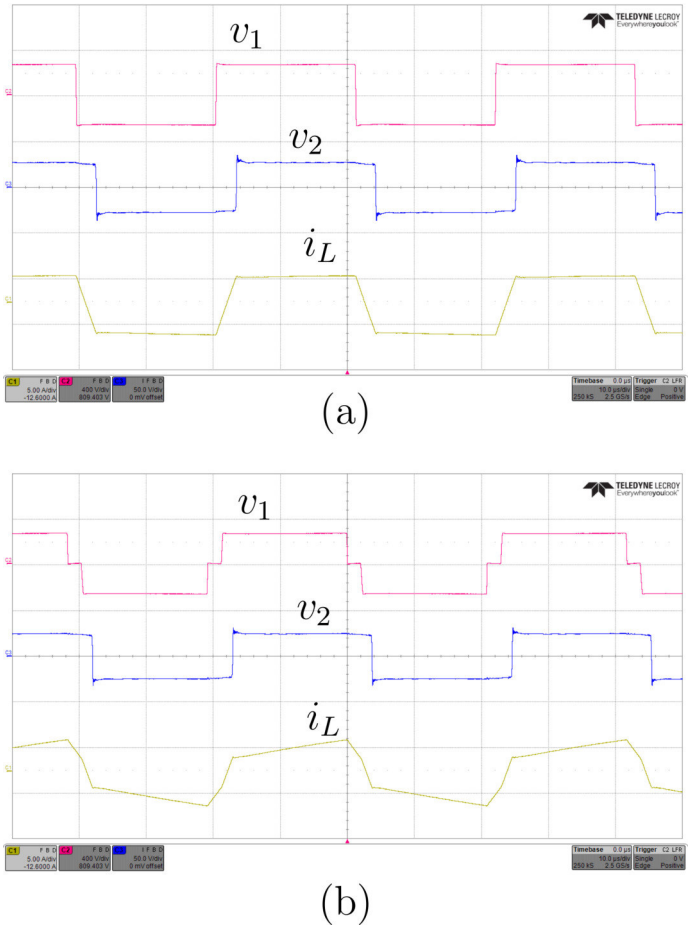

Fig. 12: Operation of the DAB with HERIC topology under single (a) and dual (b) phase-shift modulation. Primary voltage (400 V/div), secondary voltage (50 V/div) and inductor current (5 A/div)).

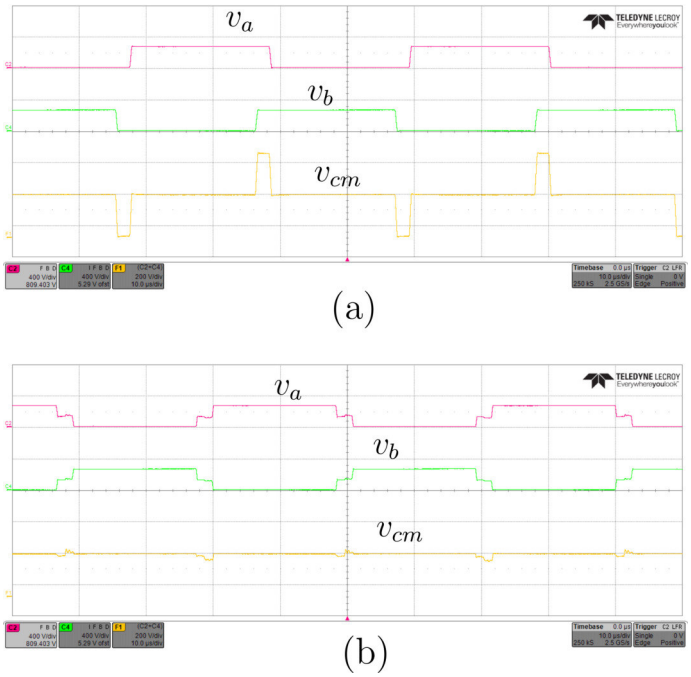

Fig. 13: Common-mode performance for the DAB (a) and HERIC (b) topology. H-bridge output voltages (400 V/div) and common-mode voltage (200 V/div).

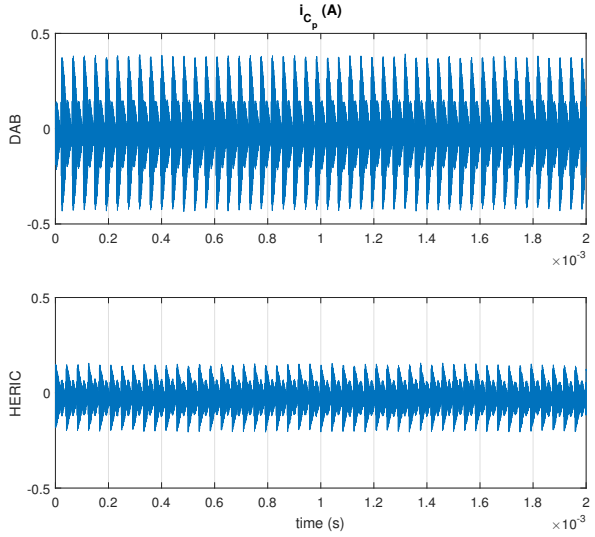

Fig. 14: Comparison of recorded data of the capacitor current for DAB and HERIC topologies with C_p = 1 nF.

low common-mode voltage characteristics. This is particularly interesting for aerospace application, where the chassis of the aircraft constitutes a common return path that allows common-mode current to flow. This is advantageous for the reliability of the insulation and for the possibility to employ transformers with high parasitic capacitance but better magnetic coupling and, as a consequence, higher transformer efficiency. HERIC, H5 and H6, already proposed for photovoltaic DC/AC inverters, are hereby analyzed for the application of soft-switching DC/DC converters. Theoretical analysis shows how the HERIC topology allows for constant common-mode behavior without additional losses for the converter. The theoretical analysis of the commutations also highlights that the different devices experience different switching losses depending on the operating point. This means that an optimization algorithm can be run to minimize the switching losses on the H-bridge or in the decoupling devices at selected operating points. Reliability analysis based on a partial discharge model for the high-frequency transformer showed a potential gain of maximum 25% in the reliability, when adopting a low-common-mode topology. Experiments on a mixed SiC/Si DAB showed an overall good efficiency and confirmed the common-mode current reduction in the case of the HERIC-based DAB.

Appendix I: DAB Equations

Equations (10)-(14) describe the behavior of the inductor current i_L like in Fig. 2a. Equation (15) and (16) are the current values at the time of switching of the primary bridge. Equations (17)-(21) are relative to Fig. 2b.

$$i_L(t) = \frac{nV_2}{L_{lk}T_s}t + i_L(0) \qquad 0 < t < \frac{mT_s}{4} \tag{9}$$

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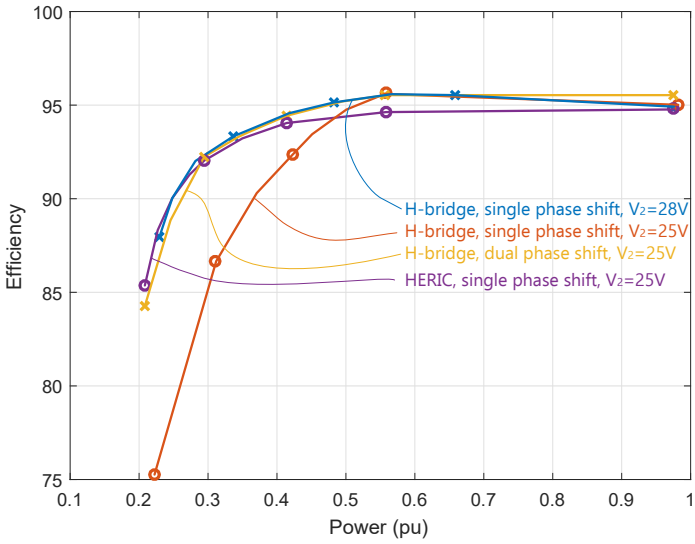

Fig. 15: Efficiency comparison of the different solutions.

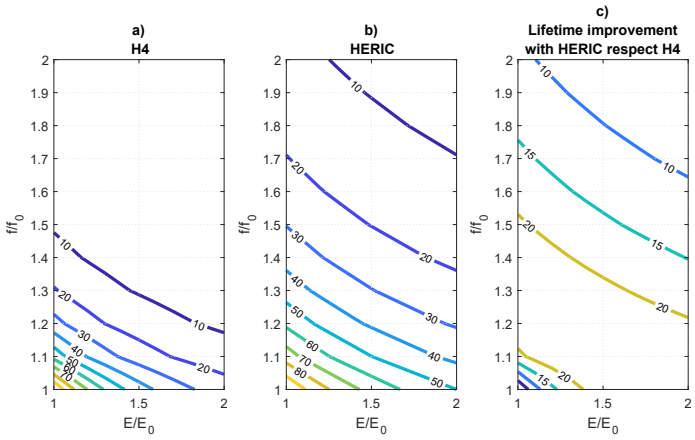

Fig. 16: Lifetime of the transformer in case of H4 converter (a), HERIC converter (b), and lifetime improvement due to the constant common-mode voltage of HERIC converter respect H4 (c). The graph shows L/L_0 in variation of the applied electrical stress amplitude and frequency and with $n = 3$ $x = 1$ and $b = 0.1$.

$$i_L(t) = \frac{V_1 + nV_2}{L_{lk}T_s}\left(t - \frac{mT_s}{4}\right) + i_L\left(\frac{mT_s}{4}\right) \quad \frac{mT_s}{4} < t < d \tag{10}$$

$$i_L(t) = \frac{V_1 - nV_2}{L_{lk}T_s}\left(t - dT_s\right) + i_L\left(dT_s\right) \quad d < t < \frac{T_s}{2} - \frac{mT_s}{4} \tag{11}$$

$$i_L(t) = -\frac{nV_2}{L_{lk}T_s}\left(t - \frac{T_s}{2} + \frac{mT_s}{4}\right) + i_L\left(\frac{T_s}{2} - \frac{mT_s}{4}\right) \quad \frac{T_s}{2} - \frac{mT_s}{4} < t < \frac{T_s}{2} \tag{12}$$

$$i_L\left(0\right) = -\frac{V_1 - nV_2 - mV_1 + 4dnV_2}{4L_{lk}}T_s \tag{13}$$

$$i_L\left(\frac{mT_s}{4}\right) = -\frac{V_1 - nV_2 - mV_1 + 4dnV_2 - mnV_2}{4L_{lk}}T_s \tag{14}$$

$$i_L\left(\frac{T_s}{2} - \frac{mT_s}{4}\right) = \frac{V_1 - nV_2 - mV_1 + mnV_2 + 4dnV_2}{4L_{lk}}T_s \tag{15}$$

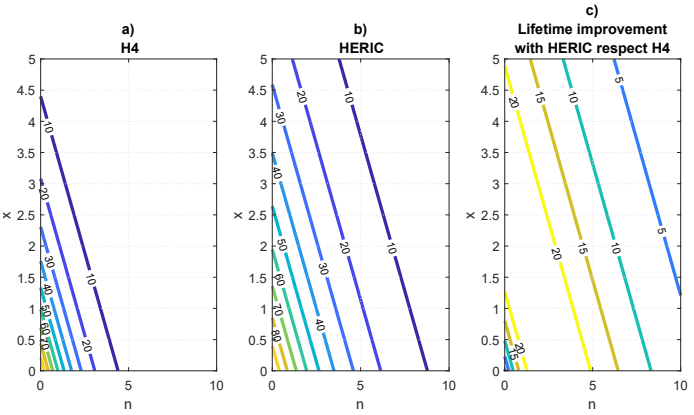

Fig. 17: Lifetime in case of H4 converter (a), HERIC converter (b), and lifetime improvement due to the constant common-mode voltage of HERIC converter respect H4 (c). The grafts show L/L_0 in variation of n and x parameters with $E_{cm}/E_0 = E_d/E_0 = 1.3$ and $f/f_0 = 1.3$.

$$i_L(t) = \frac{nV_2}{L_{lk}T_s}t + i_L(0) \quad 0 < t < d \tag{16}$$

$$i_L(t) = -\frac{nV_2}{L_{lk}T_s}\left(t - d\right) + i_L\left(d\right) \quad d < t < \frac{mT_s}{4} \tag{17}$$

$$i_L(t) = \frac{V_1 - nV_2}{L_{lk}T_s}\left(t - \frac{mT_s}{4}\right) + i_L\left(\frac{mT_s}{4}\right) \quad \frac{mT_s}{4} < t < \frac{T_s}{2} - \frac{mT_s}{4} \tag{18}$$

$$i_L(t) = -\frac{nV_2}{L_{lk}T_s}\left(t - \frac{T_s}{2} + \frac{mT_s}{4}\right) + i_L\left(+\frac{T_s}{2} - \frac{mT_s}{4}\right) \quad \frac{T_s}{2} - \frac{mT_s}{4} < t < \frac{T_s}{2} \tag{19}$$

$$i_L\left(\frac{mT_s}{4}\right) = -\frac{V_1 - nV_2 - mV_1 - 4dnV_2 + mnV_2}{4L_{lk}}T_s \tag{20}$$

VIII. Acknowledgement

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