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CSI7: a Modified Three-phase Current Source Inverter for Modular Photovoltaic Applications

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***Abstract*—This paper analyzes the performance of a grid-tied, wide power range, transformerless, modified three-phase Current Source Inverter (CSI), named CSI7. The CSI7 topology is here analyzed along with a suitable Space Vector Modulation (SVM) strategy able to attenuate the excitation of the output CL filter. The theoretical analysis and simple analytic expressions highlighted the performance and limitations of the topology when employed as a single-stage PV inverter, with particular emphasis on injected grid currents distortion and ground leakage current values. The inverter wide input range allows interfacing PV strings of different module count with a simple closed loop control. The principle of operation and control is described, the viability of the CSI7 topology was assessed with simulations and extensive experiments on a full-size laboratory prototype.**

***Index Terms*—current source inverter, photovoltaic power systems, ground leakage current, renewable energy sources.**

I. Introduction

Solar photovoltaic (PV) market share grew significantly during the last decade, reaching widespread application. Especially in large PV plants with centralized converters, the series/parallel connecting of numerous PV modules in long strings invariably led to MPP mismatch losses, mainly due to manufacturing tolerances or partial shading. To overcome this situation different individual converters can be attached to a string with a reduced number of PV modules, to attain better MPP tracking (MPPT). A more radical approach is to integrate a minaturized dc-ac inverter into each PV module, obtaining a Module Integrated Converter (MIC). In literature, grid-tied PV plants with distributed converters were proposed, either with with common DC Bus or with common AC Bus. A decentralized, modular PV installation with string inverters connected to a common three-phase distribution network has many benefits: the principal one being the use of standard, cost effective components and cables typical of industrial installations. A common DC bus on the contrary would require special switchgear, expensive DC safety disconnectors and fuses, rated for DC voltages greater than 400V.

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Devices currently on the market have shown that conversion efficiency and reliability are the main issues. To avoid maintenance costs and loss of production the expected lifespan of the PV String Inverter (SI) should be equal to that of the PV modules (e.g. 20+ years). This is the most challenging requisite because the electronic circuit is typically installed in a harsh environment with high operating temperature and is subjected to thermal cycling.

In the case of inverter architecture for PV grid interfacing it is possible to identify two main converter topologies: voltage source inverter (VSI) and current source inverter (CSI). The former one is the actual state of the art for module integrated inverters, while the latter one is a well known topology usually employed in medium-voltage high-power electric drives. A comparison of the efficiency of traditional VSI and CSI was presented in [1]. The VSI topology presents higher efficiency and fewer semiconductor devices respect to the CSI, but it presents typically also a reduced lifetime because of the presence of Electrolytic capacitors as power decoupling feature.

The present work concerns the performance analysis of a modified CSI topology applied to three-phase grid-connected converters for PV power generation.

Because the power decoupling component is an inductor, this architecture poses some critical issues during shut-down, as the input current can't be instantaneously set to zero. Care must be taken especially in case of sudden power outages: some countermeasures to avoid dangerous voltage spikes on the DC link are suggested in [2]. Alternatively, in the indicated modular installation, the photovoltaic CSI string inverter can short circuit the PV input indefinitely as close to the PV modules as possible, thus reducing virtually to zero the string voltage. This feature could prove useful in case of emergency, such as in the event of fire: in case of a centralized inverter, opening the DC disconnector located at the inverter input would leave the full generator voltage still active on the DC line between the PV modules and the inverter, posing shock hazard to the emergency response teams.

Apart from this, CSI topology can offer some advantage when employed in PV applications: it is a single stage architecture, thanks to its inherent boost capability; it draws a smooth DC current from the PV modules, reducing their stresses; injected current is directly controlled; the energy storage component is an inductor, characterized by superior ruggedness and longer lifetime, especially when compared to electrolytic capacitors.

The design exploits CSI inherent step-up capability to obtain

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a single stage power interfacing between the low voltage PV input and the high voltage output, fed into the distribution grid. Compared to traditional VSI architecture, the investigated architecture allows for a greater input voltage range in a single stage topology, also allowing for a wide power range operation with given devices.

The use of space vector modulation (SVM) for grid-tied CSI converters was described in [3]. Modeling of CSI converters for PV applications is reported in [4]. The effect of common mode voltage was analyzed in [5], where a solution was presented able to ideally suppress the ground leakage current. The use of a CSI architecture with an additional switch was also employed in single phase architectures [6], [7].

The CSI topology applied to MICs has been previously investigated in [1], [8], suggesting the use in conjunction with dedicated high voltage solar modules, as well as adopting various solutions to overcome undesired common mode voltage variations. The well established method to reduce common-mode voltage variations in traditional CSI topology relies on avoiding the zero vectors at the price of modulation index limitation and presence of output bipolar current pulses. An other solution is a proper selection of the zero vectors [8].

Multilevels current source inverters solutions was recently analized in [9] and [10] and also with the possibility of a FPGA control [11], but the cost and complexity of this solutions do not seem to be adapted for low power applications. In addition to that, no output common-mode voltage variations are taken into account in these works in order to limit the ground leakage current.

The present work describes the implementation of a CSI topology named CSI7, particularly suitable to operate with high step-up voltage ratio, and hence with low-voltage, low-module count strings. A suitable SVM strategy was developed in order to minimize the THD of the injected grid-current and conduction power losses. Moreover a simple loop control was identified to control the PV power converter in MPPT operation. The CSI topology with an additional leg was first introduced in [12] to allow PWM modulation of SCRs converters: the additional GTO switch on the fourth leg was used to switch off the SCRs. The same topology was employed in a AC/DC configuration as a controlled rectifier stage for three phase power converters. In these configurations a Diode is employed as the additional switch together with an optimized switching pattern aimed at minimizing switching losses, ripple values and mains current quality [13]–[15].

Recent works investigated the potential to add a four leg in the traditional CSI topology constituted of a simple series of two reverse blocking switches. In [16], [17] the fourth leg in CSI converters is exploited to provide a fourth switch configuration able to produce a zero vector in order to reduce the common-mode voltage variations. In [18] the mid point of the four leg was connected to the neutral of the three-phase grid and to mid point of a voltage divider made of two capacitors in series. In this way the ground voltage across the PV parasitic capacitance is theoretically constant and no ground leakage current arises. However this solution present some disadvantages, such as the current circulation in the neutral connection wire and therefore an inferior performance in terms of efficiency and THD of the phase currents. In addition, the balancing of the capacitor voltage divider is not guaranteed.

CSI topology with additional switch (CSI7) was also presented in [19] for PV grid-connected converters and in [20] for stand alone applications with particular emphasis on the reduction of switching power losses. With respect to the these previous works, this paper presents an improved description of the CSI7 solution highlighting the ability to operate without the use of the blocking diode on the additional switch and the impact on reducing ground leakage current. In particular the experimental validation assesses the CSI7 architecture and associated adopted SVM in terms of injected currents distortion and ground leakage current mitigation.

The following sections detail the research work and the experimental assessment that was carried out for the CSI7 topology with the selected SVM. After a brief recall of the standard SVM for CSI converters, Section II presents the CSI7 topology and associated PWM switching strategy together with the simple power converter control. Section III reports the simulation results for the CSI7 topology in Matlab/Simulink environment, with different SVM. Section IV details the experimental setup and the results obtained on a full-size laboratory prototype during grid-tied operation. The same section shows a comparison between simulations and experiments in order to validate the theoretical assumptions. Section V reports a brief comparison between different SVM, followed by Conclusion.

II. Current Source Inverter for PV grid-connected systems

A. CSI Topology

Figure 1 shows the CSI7 topology for the three phase CSI for PV String Converter applications. With respect to the classic CSI topology, in the CSI7 topology there is an additional power switch: S_7. This additional power switch, together with a suitable PWM strategy, allows to strongly decrease the conduction power losses of the main power switches and also limit the distortion due to commutation glitches, as it will be explained in the following. In the meantime also the ground leakage current can be reduced thanks to the presence of this additional switch.

The CSI topology is characterized by higher semiconductor power losses with respect to VSI topologies [21], especially in the case of high step-up voltage operation. In fact the six power switches (made by series connected mosfets + diodes, Fig. 1) constituting the classic CSI topology must withstand both the DC output current of the PV Panel and the high voltage of the grid. The resulting conduction power losses are quite high since at any given time the input DC Link current flows always through 2 power switches and 2 diodes. Therefore efficiency of the CSI improves as the DC input voltage increase. Semiconductor power losses remain virtually unchanged in presence of a very large variation of the input DC voltage, depending only on the DC input current value.

Since in this work the CSI is used in a PV String Converter application, the conduction power losses would be intrinsically

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very high. The introduction of the power switch S_7 allows to reduce the number of power semiconductors in series during the short circuit of the input DC inductance from four devices to only one. If a high step-up voltage ratio is required, this short-circuit time is a very large fraction of the total PWM period.

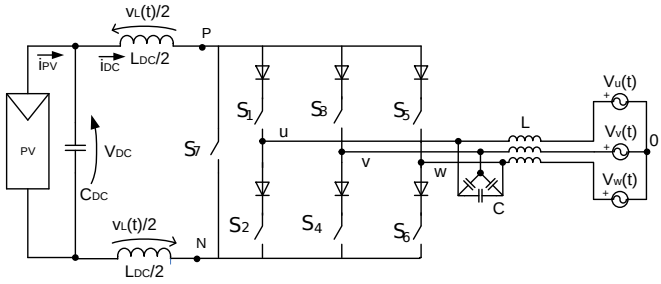

Fig. 1. Three-phase CSI7 topology.

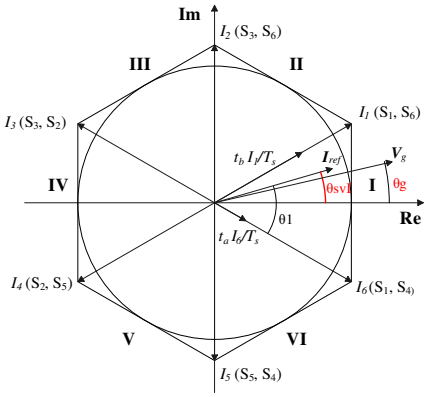

Fig. 2. Space vector representation.

With reference to the space (state) vector representation of Fig. 2, the six power switches $S_1 - S_6$ can be driven as in a classic CSI solution when the converter apply the six active (non-zero) space vectors (SV), $I_1 - I_6$, see [22].

Null vectors are traditionally obtained by short-circuiting the DC-link through a leg short-circuit. In the CSI7 solution these null vectors are not employed: the null state vector is created by switching on the additional power switch S_7. All the active space vectors are defined by the switches configuration $S_1 - S_6$ of the bridge (where 1 = conducting).

With reference to the same figure, any given current reference vector I_{ref} is obtained as a time weighted linear combination of the switching vectors of the corresponding sector (or sextant): t_a and t_b for the two active space vectors and t_z for the null state vector (d_a and d_b represent simply the normalized time intervals with respect to the switching period T_s).

$$\begin{cases} t_a = d_a T_s \\ t_b = d_b T_s \\ t_z = T_S - (t_a + t_b) \end{cases} \quad (1)$$

The angle $\theta 1$ is used for the computation of the dwell time intervals t_a and t_b, while θ_{SVI} is the angle of the current space vector I_{ref} which is used to compare it with the angle of grid voltage space vector $\vec{V_g}$, named θ_g.

The space vector of the grid voltage can be represented as $\vec{V_g} = V_g e^{j\omega t = j\theta_g}$, while the space vector of the injected current is $\vec{I_{ref}} = I_{ref}^{j\theta_{SVI}}$. When the converter works in unity power factor operation $\theta_g = \theta_{SVI}$.

In the CSI7 topology, shown in Fig. 1, a simple power switch (Mosfet or IGBT) without a diode in series for S7 can be adopted only if the voltage across it is always positive from drain (collector) to source (emitter). Figure 3 shows the instantaneous phase voltages and the respective SV sectors of current space vector when the the CSI7 operates at unity power factor.Figure 4 details the instantaneous values of the line-to-line voltages, v_{uv} e v_{uw} for sector I. The following analysis is conducted for sector I, but the assumptions are valid also for the others SV sectors. The evolution of line-to-line voltages during sector I of the space vector current is fundamental in order to understand the circumstances leading to a negative voltage applied across switch S7, whereas a diode must be inserted in series.

During the sector I, with PF=1, the two active vectors applied are I1 (S1 and S6 ON) and I6 (S1 and S4 ON). During the application of these two switches configuration, the voltage across the switch S7 is respectively equal to voltages v_{uv} (I1) e v_{uw} (I6) plus two voltage drops across the inductive part (L) of the output filter. It is important to point out that during the active vectors the inductive voltage drops determine a positive incremental contribution of the voltage across S7 and therefore neglecting these voltage drops represents a worst case scenario in order to find the operating condition range in which this condition is satisfied.

Figure 4 not only shows that the line-to-line voltages v_{uv} e v_{uw} are positive in case of unity power factor but also that there is a phase margin equal to $+\pi/6$ and $-\pi/6$ between the space vector of the grid voltage and the injected grid current, $\phi = \theta_g - \theta_{SVI}$, in which the voltage across S7 is still positive. This implies that the CSI7 converter can operate with a simple switch for S7 (without the diode in series) with a PF that can decrease down to 0.866, thus giving the capability for a reasonable amount of inductive and capacitive reactive power injection.

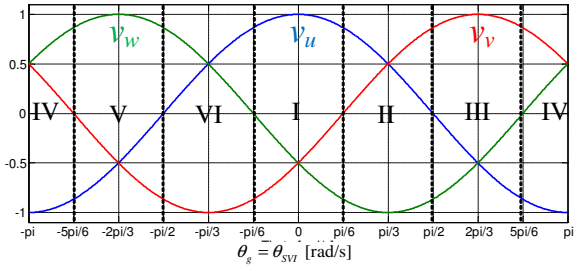

Fig. 3. Grid phase voltages with sector numbers of the space vector current in case of unity power factor.

B. Current Space Vector Modulation

To maintain linearity, the SV space of Fig. 2 is limited to the inner circle of the hexagon, hence the modulation index value

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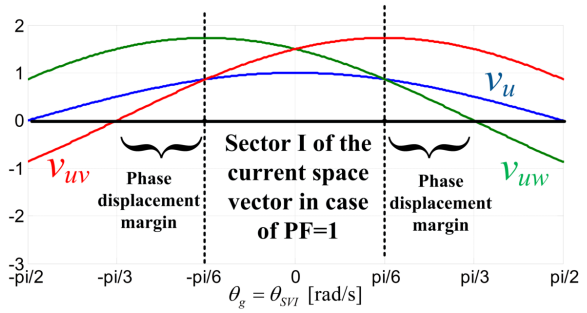

Fig. 4. Power factor operation range to guarantee a positive voltage across S7 during the I sector.

($m = |I_{ref}|/I_{DC}$) is restricted to $0 \leq m \leq \sqrt{3}/2$. Different SV sequences are available, from basic ones [23], to more sophisticated ones, aiming at minimizing switch commutations and switching lossess or at reducing distortion in supply current [24]. The PWM strategy to be implemented should:

- guarantee overlap times between CSI commutations to avoid voltage spikes on the DC link
- avoid glitch generation by the PWM strategy during sextants changes
- minimize THD of the injected current
- minimize ground leakage current caused by common mode voltage on the input terminal
- minimize power losses

Because the output filter is an CL-type filter which has a lightly damped second-order characteristic, it shows a lightly damped resonant behavior: output glitches and spectral components at the resonant frequency can cause the output filter to ring. This glitch effect can be attenuated using an active damping as presented in [25], [26]. In the present work, instead of implementig passive or active damping solutions for CL resonance of the output filter, the modulation that was identified aims at minimizing the excitation of the output CL filter by avoiding glitches generation. Glitches can be caused during the transition of the current space vector from one SV sextant to the adjacent or by an undesired path of the output current of CSI due to the introduction of overlap times.

The first cause of glitch generation can be eliminated with an accurate choice of SV sequence for every sextant in order to avoid the consecutive application of the same active state vector at end of one sextant and at the beginning of the next as well as avoiding transition between two active state vectors that are more than $\pi/3$ apart.

The second cause is eliminated with the introduction of the power switch S_7 since the overlap time between an active state vector and a null state vector is obtained by widening its ON-time: i.e. leading and lagging the ON state with respect to the other active states transitions. The overlap time in CSI inverter modulation is required in order to avoid momentary DC input inductor open circuit, a condition symmetrical to dead time introduction in VSI inverter modulation.

In CSI operation an overlap time, t_{ov}, is needed for safe commutations between current space vectors. This overlap time causes distortion in the injected current waveforms if it is not accurately compensated. Since the application described in this paper requires a high boost factor, the modulation index m is so low (this assumption will be detailed in the following section) that it makes difficult any finer subdivision of the active times t_a and t_b.

An effective overlap time compensation can be obtained only if every active state vector is separated from the others by the null state vector which represents the dominant state vector during overlapping. The SV sequence which satisfy these requirements is described in Fig. 5 and was named Alternated Sequence. The figure shows two different SV sequences, one for odd and one for even sextants. The change in commutation order is required to eliminate glitches during sextant transitions, as explained earlier.

The power switch S_7, besides ensuring a strong reduction of conduction power losses, also helps to avoid glitches generation since it is the only contributor to null state vector generation, because of S_7 conduction voltage drop is lower than the other reverse-blocking switches (transistor with series connected diode). By using S_7 together with the alternate commutation sequence, the overlap time ensures that S_7 is active during every turn-on and turn-off transient of the reverse-blocking switches (S_1 to S_6). This ensures that all the commutations of S_1 to S_6 happen under zero current (ZCS), as all the input DC current flows on S_7. Under these operating conditions S_7 is the only device operating with hard switching.

Figure 6 shows the effect of overlap time t_{ov} on the commutation strategy. The overlap time is introduced as the firing signal of power switch S_7. Because the null state is dominant with respect to other active states, the effective active vector times for the alternated sequence are:

$$\begin{cases} t_a' = t_a - 2t_{ov} \\ t_b' = t_b - 2t_{ov} \end{cases} \tag{2}$$

The SV modulation times t_a, t_b were compensated accordingly, by adding $2t_{ov}$ to them.

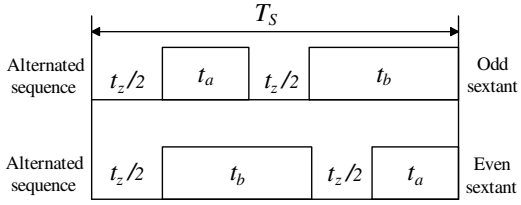

Fig. 5. Alternated Sequence, details of commutation sequence for even and odd sextants to avoid glitch generation.

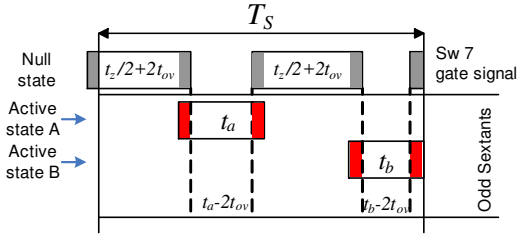

Fig. 6. Alternated sequence - overlap time t_{ov} effect (scale exaggerated for demonstration purpose).

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Another important issue that has to be taken into account in PV transfomerless topologies is the ground leakage current, that is mainly caused by the part of common-mode voltage variation introduced by the power converter operation [27].

With respect to traditional topologies, the CSI7 solution is able also to reduce the ground leakage current flowing through the parasitic capacitance between the PV panels and the ground.

In the CSI7 topology, shown in Fig. 1, the common-mode voltage can be computed using the neutral connection of the three-phase grid voltage as voltage reference, see (3).

$$v_{cm} = \frac{V_{P0} + V_{N0}}{2} \tag{3}$$

This way the instant values of the common-mode voltage during every active switches configuration can be easily computed and results respectively: $-v_v/2$ for vector I1,$-v_u/2$ for vector I2, $-v_w/2$ for vector I3, and so on. These instantaneous values are the same both in case of traditional CSI topology and the CSI7 solution. The advantage of the latter is that, with the introduction of the additional switch S7, the null vector can be applied by S7 alone, while all the other transistors are turned Off. On the other hand, in case of traditional CSI during the application of the three different null vectors, the instantaneous v_{cm} assumes the following voltage values: $v_u/2$,$v_v/2$ and $v_w/2$. In case of the CSI7 solution, during the null vector configuration, the instantaneous v_{cm} is 0 thanks to the disconnection of the PV panels from the grid at the price of an increased number of commutation per cycle.

C. CSI control strategy

In order to extract the maximum available energy from the PV source, the output voltage of the PV string is controlled by a MPP tracker. Therefore the first goal for assessing the performance of a PV CSI concerns its capability to operate in steady state conditions under a large input DC voltage variation. A steady state condition with an almost constant input DC current, i_{DC}, can be obtained when the mean value of the voltage across the input inductor L_{DC} of the CSI is null. Since the injected grid current is always at the same frequency of the grid voltage and thanks to the symmetry of the grid generator the evolution of the voltage across L_{DC} is the same for every SV sextant. The integral of $v_L(t)$ over a switching period, T_s in the sextant I of the SVM is shown in eq. (4).

$$\int_t^{t+Ts} v_L(t)\mathrm{d}t = \int_t^{t+Ts} ((V_{DC} - v_{wu}(t))t_a + \\ +(V_{DC} - v_{vu}(t))t_b + V_{DC}t_z)\mathrm{d}t = 0 \tag{4}$$

It is then possible to compute the voltage V_{DC} which satisfies eq. (4) obtaining a linear relationship between output voltage and the modulation index, as reported in [19].

This property is very important in order to limit the current ripple of I_{DC}, which shows only an harmonic at the switching frequency. Figure 7 shows the relationship between the modulation index m and the V_{DC} at different power factor operation.

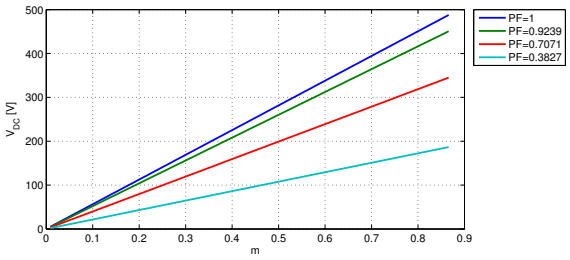

Fig. 7. Relation between modulation index and V_{DC} of the PV module.

The CSI performance presented previously indicates the feasibility of the CSI to operate with a photovoltaic source as the output voltage of the PV panel can be properly controlled by a MPPT algorithm.

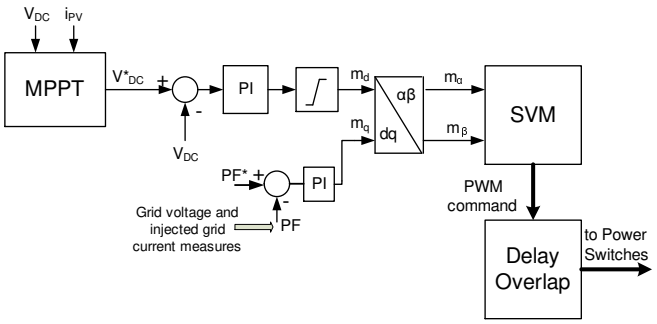

Fig. 8. Schematic of the proposed control.

Figure 8 shows the proposed CSI control. The input voltage control loop employs a PI regulator which provides the modulation index m_d, proportional to the active current injected into the grid. In other words, the amplitude of the ideal active current can be obtained as $I_d = m_d * I_{DC}$. The modulation index m_q can be fixed to zero or varied to futher fine-tune the power factor of the CSI: in fact the presence of the capacitance-inductive output filter determines reactive power absorption. However, the power factor control capability of the CSI7 converter is beyond the scope of the present paper. The modulation indexes m_α m_β are computed by Park's transform and used as input of the SVM. The two indexes are used to determine the polar coordination of the current space vector: module $m = \sqrt{m_\alpha^2 + m_\beta^2}$ and angle $\theta = arctg\frac{m_\beta}{m_\alpha}$. Equation 5 shows the calculation of the normalized time intervals of the two active states which border the current space vector, where θ_1 is the angle of the current space vector referred to the active state vector placed in clockwise respect to it (see Fig. 2).

$$\begin{cases} d_a = 2/\sqrt{(3)}m\sin(\frac{\pi}{6} - \theta_1) \\ d_b = 2/\sqrt{(3)}m\sin(\frac{\pi}{6} + \theta_1) \end{cases} \tag{5}$$

III. Numerical simulations

The CSI7 topology and modulation control strategy was numerically modeled in Matlab Simulink environment, employing Plecs plugin for the power converter stage. The simulated system incorporated a PV array and the power

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converter architecture shown in Fig. 1. The control of the CSI7 converter was implemented as shown in Fig. 8, for simplicity m_q was fixed to zero. The simulations were carried out in order to verify the effectiveness of the adopted SVM in terms of injected grid current distortion without the insertion of the parasitic equivalent capacitance C_{PV}. Table I summarizes the parameters used for simulations and following experimental results.

Figure 9 shows the phase injected grid current and voltage in case of base PWM and traditional CSI solution. Figures 10 and 11 show the waveforms of the injected grid currents with the Alternated switch sequence respectively without the overlap compensation and without the change in the SV sequence for odd and even sextants. The lack of this sequence inversion determines an excitation of the output CL filter that involves an unacceptable injected current distortion. Figure 12 shows the phase injected grid current with the adopted SVM strategy: in this case the waveform distortion is drastically reduced. It is important to stress that no active damping techniques were used neither in simulations nor in following experiments.

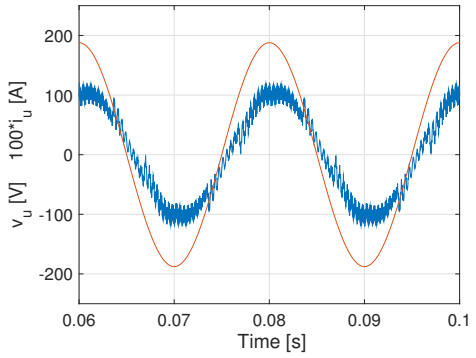

Fig. 9. Simulation results. Phase grid voltage and injected current, THD 11.88%) in case of base PWM for traditional CSI topology.

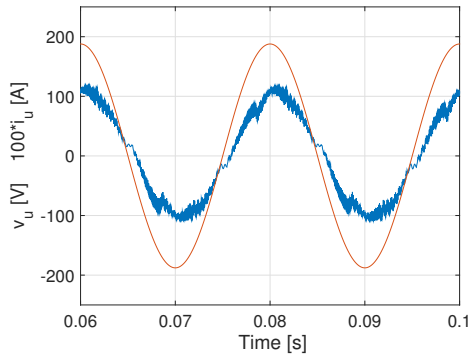

Fig. 10. Simulation results. Phase grid voltage and injected current , THD 8.2%) in case of adopted SVM for CSI7 topology without overlap compensation.

As stated before, by introducing the overlap time with S_7 in the alternate commutation sequence, S_7 is active during every turn-on and turn-off transient of the reverse-blocking switches (S_1 to S_6). As a consequence, all the commutations of S_1 to S_6 happen under zero current (ZCS), as the input DC

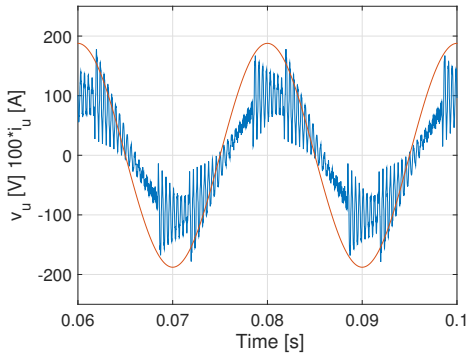

Fig. 11. Simulation results. Phase grid voltage and injected current , THD 25%) in case of adopted SVM for CSI7 topology without the inversion sequence.

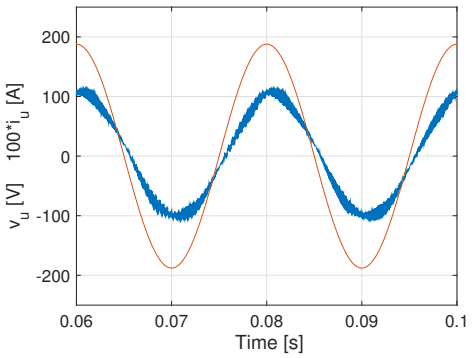

Fig. 12. Simulation results. Phase grid voltage and injected current , THD 4.4%) in case of adopted SVM for CSI7 topology.

current flows on S_7. Figure 13 shows switches commutations inside the first sextant: as it can be seen S_7 is the only device operating with hard switching. The same considerations apply for all the other sextants. Furthermore, in order to avoid useless commutations, S1 is kept constantly on in the sextant, even during null state (S7 on).

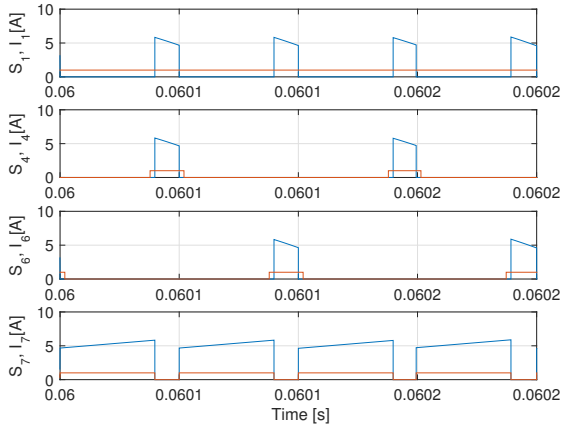

Fig. 13. First sextant operation: switching sequence and device currents of S_1, S_4, S_6 and S_7.

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IV. Experimental Results

A laboratory prototype was built to evaluate all the theoretical assumptions. A TMS320F28069 controller was used to implement the space vectors modulations of the traditional CSI and of the CSI7. In addition to this, all the algorithms for the injection of electric power into the grid were implemented, only the MPPT algorithm was not developed since is out of the scope of the paper.

The experimental setup is shown in Figure 14. The CSI7 was connected to a variable DC Voltage Source. A three-phase transformer was connected between the grid and the outputs of CSI7. The neutral of the transformer secondary winding was connected to earth through the resistance R_g, which simulate the ground resistance of a three-phase grid. An equivalent capacitor simulates the parasitic capacitance to earth of PV panels and it was connected between the ground and the negative pole of the DC voltage source. Through this equivalent capacitor and R_g flows the ground leakage current of the PV system. A Digital Power Analyzer PPA 5530 was used for harmonic analysis and efficiency measurements: THD was measured by the same instrument and was computed from the series of the first 100 harmonics.

Table I summarizes the conditions of the experimental tests. The power switches used in the converter prototype are the commercial IGBT IHY15N120R3 1200V 15A. To further reduce conduction power losses, a SiC Mosfet can be used for S7. It is important to put in evidence that the power semiconductors were not chosen in order to maximize the efficiency. The measure of the efficiency should be mainly considered only as performance comparison of different modulation strategies running on the same hardware.

Figure 15 shows a picture of the power board of the laboratory prototype. The input inductor L_{DC} was split in two input inductors in order to obtain a better performance in terms of output common-mode voltage and therefore lower ground leakage current [1].

The first set of experiments was conducted in order to verify the effectiveness of the adopted SVM for CSI7 topology, in particular the overlap compensation and the alternated sequence in the odd and even sextants. In these first experiments the equivalent parasitic capacitance C_{PV} that was not inserted. The performance of the CSI7 solution was compared to the classic CSI topology driven by the base SVM: this represents the reference case. Figure 16 shows the grid voltage and current corresponding to 348 W of injected electric power. The THD of the injected current was measured equal to 11%.

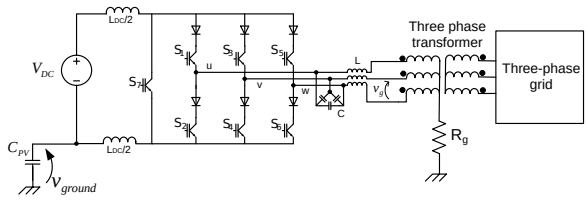

Fig. 14. Experimental test setup.

The effectiveness of the adopted SVM for the CSI7 topology was assessed through the following tests. For a fair comparison

TABLE I
Experimental and Simulation parameters.

Name	Description	Value	Units
V_{DC}	DC voltage source	60	V
V_g	rms line-to line grid voltage	230	V
f_g	grid frequency	50	Hz
f_s	switching frequency	10	kHz
t_{ov}	overlap time	2	μs
L_{DC}	input inductance	2	mH
L	AC Filter inductance	1.4	mH
C	AC Filter capacitance	1	μF
R_g	ground resistance	4.7	Ω

TABLE II
Equivalent PV parasitic capacitance values for different sets of simulations and experiments.

C_{PV} value	Description
$0nF$	simulations, first set of experiments (SVM comparison)
$220nF$	second set of experiments for CSI7 solution
$22nF$	second set of experiments for traditional CSI solution

with respect to the previous reference case, the same value of injected electric power was used, i.e. 348 W. Figure 17 shows SVM performance when the overlap compensation was not applied, while in Fig. 18 the inversion sequence was not applied. The THD of the injected currents result 8.9% and 11.5% respectively. Figure 19 shows the performance of the complete SVM reaching a THD=4.5%.

Eventually table III compares the THD of simulation and experimental results in the same operating conditions. The only significant difference in the comparison is related to the use of adopted $(0A0B)$ PWM strategy without the inversion sequence; in this case the presence of distributed/parasitic resistances in the system allows to realize a passive damping for the output CL filter. Passive damping that is not present in the simulation environment.

Figure 20 shows the good dynamic response of CSI7 in case of step variation of the injected grid current, obtained with a step variation of the modulation index m_d. With reference to Fig. 8 the test was conducted without the outer MPPT and V_{DC} control loop.

The second set of experiments was aimed at evaluating the ground leakage current issues, by comparing the CSI7 solution

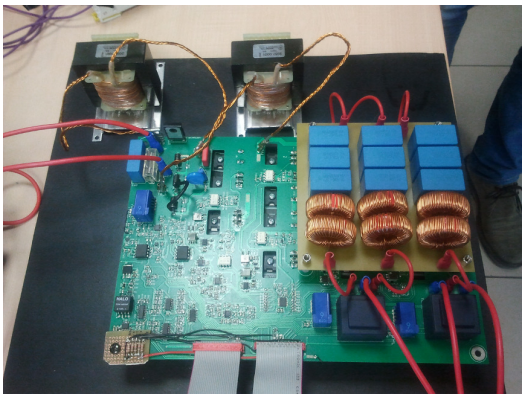

Fig. 15. Power board of CSI7 laboratory prototype

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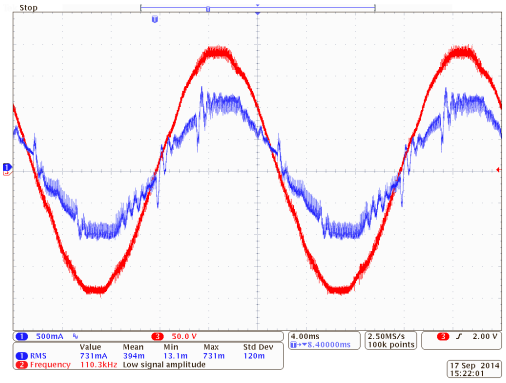

Fig. 16. Experimental results. Phase grid voltage (red trace, 50V/div) and injected current (blue trace, 0.5 A/div, THD 11%) in case of base SVM.

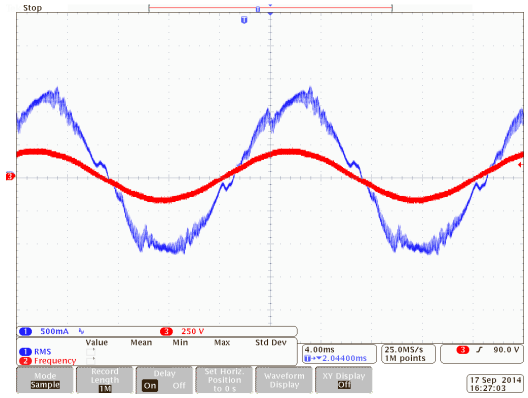

Fig. 17. Experimental results. Phase grid voltage (red trace, 250V/div) and injected current (blue trace, 0.5 A/div, THD 8.9%) in case of adopted SVM for CSI7 topology without overlap compensation.

TABLE III
SIMULATIONS AND EXPERIMENTAL THD COMPARISON

SVM Name	Simulation THD	Experimental THD
CSI 0AB	11.8%	11%
CSI7 0A0B no OV.	8.2%	8.9%
CSI7 0A0B no inv. seq.	25%	11.5%
CSI7 0A0B	4.4%	4.5%

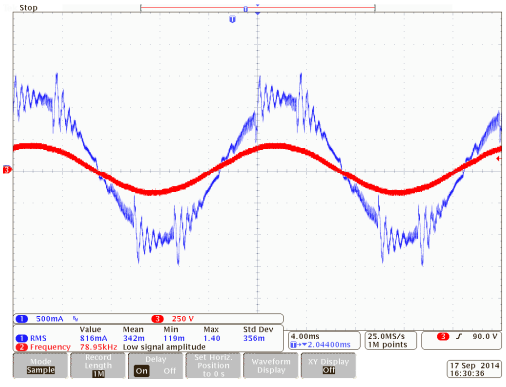

Fig. 18. Experimental results. Phase grid voltage (red trace, 250V/div) and injected current (blue trace, 0.5 A/div, THD 11.5%) in case of adopted SVM for CSI7 topology without the inversion sequence.

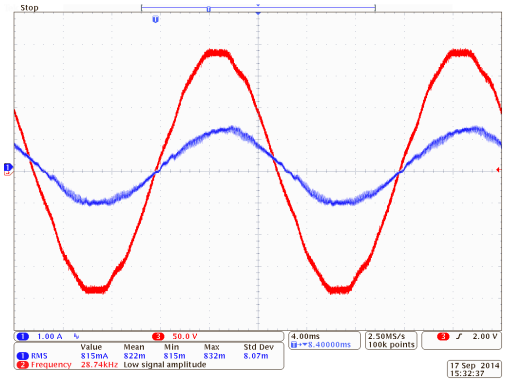

Fig. 19. Experimental results. Phase grid voltage (red trace, 50V/div) and injected current (blue trace, 1 A/div, THD= 4.5%) in case of the complete adopted SVM for the CSI7 topology.

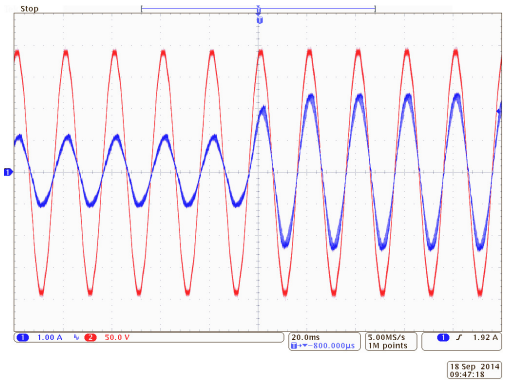

Fig. 20. Experimental results. Step variation of the injected grid current (blue trace, 1A/div). The figure shows only one phase current and grid voltage.

against the traditional CSI topology. Table II shows the three different values for the equivalent parasitic capacitance C_{PV} used in simulation and experiments.

Figure 21 shows the ground leakage current and ground voltage across a $220nF$ equivalent PV parasitic capacitance in case of the CSI7 solution. Under these operating conditions the resulting rms value of the ground leakage current is about $26mA$. Figure 22 shows the ground leakage current and ground voltage across a $22nF$ equivalent PV parasitic capacitance in case of traditional CSI solution. As it can be seen, even by reducing the parasitic equivalent capacitance by an order of magnitude the resulting rms value of the ground leakage current exceeds $150mA$. In order to avoid damage to the converter prototype due to very high ground leakage current values, it was not possible to conduct this experiment with the same $220nF$ equivalent PV parasitic capacitance.

Figure 23 shows the experimental comparison efficiency of the CSI7 solution and traditional CSI. This behavior was expected since in case of a relatively small DC input voltage (see Table I) the time interval in which one leg is short circuited is predominant during every PWM period. The same figure shows also the efficiency of the CSI7 solution with an higher DC input voltage, $V_{DC} = 210V$. Despite the power semiconductor devices were not chosen for efficiency maximization, the overall efficiency results almost acceptable

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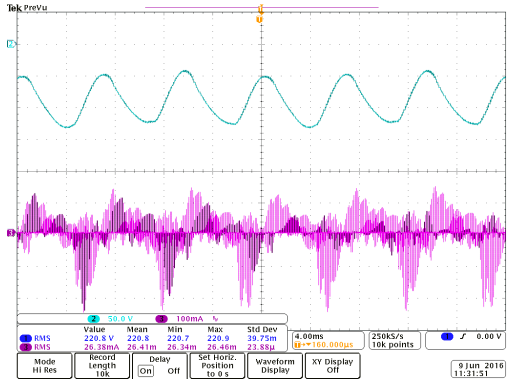

Fig. 21. Experimental results. Ground voltage (50V/div) and ground leakage current (100mA/div) in case of CSI7 solution.

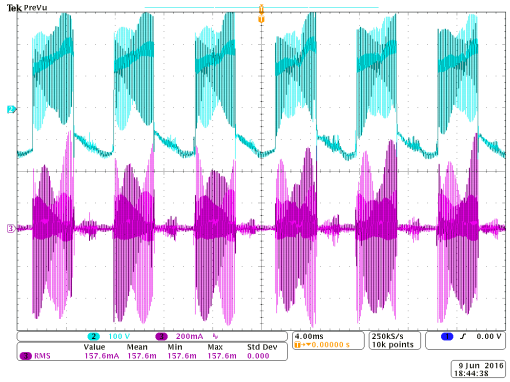

Fig. 22. Experimental results. Ground voltage (100V/div) and ground leakage current (200mA/div) in case of base SVM for traditional CSI topology.

for actual PV systems in this last case.

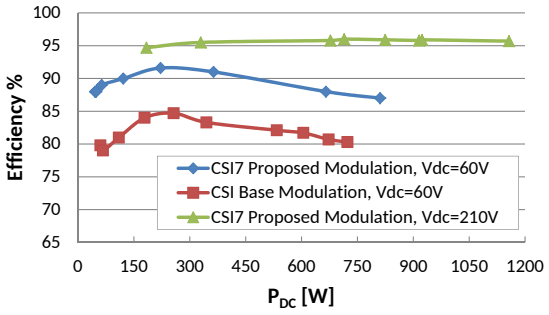

Fig. 23. Experimental results. Efficiency comparison between CSI7 solution and traditional CSI solution.

V. Evaluation of PWM Strategies

A theoretical analysis of the switching losses was carried out by comparing three different SVM control strategies during one PWM cycle. Only a subset of the SVM control strategies were chosen among the ones available in literature. The present work was focused on the alternated modulation sequence ($0A0B$) because of the benefits on output glitches elimination. Other high efficiency commutation strategies exist, such as ($AB0BA$) that are aimed at reducing switching losses (e.g. in [14]). Table IV summarizes a comparison among different SVM strategies: basic CSI topology with basic SVM $0AB$, CSI7 topology with basic SVM $0AB$, CSI7 topology with the proposed SVM $0A0B$ and CSI7 topology with $AB0BA$ SVM. As it can be seen, the introduction of S7 obviously increases the converter efficiency for all the modulation strategies, because of the beneficial effect on the conduction losses during null state.

TABLE IV
Comparison among SVM strategies

SVM	Conduction (null state)	Conduction (active state)	Hard Switch Commutations	Comm. ZCS
0AB (Basic CSI)	2 Transistors 2 Diodes	2 Transistors 2 Diodes	3	3
0AB (CSI7)	1 Transistor	2 Transistors 2 Diodes	3 (2xS7)	3
AB0BA (CSI7)	1 Transistor	2 Transistors 2 Diodes	4 (2xS7)	4
0A0B * (CSI7)	1 Transistor	2 Transistors 2 Diodes	4 (4xS7)	4

Referring to Table IV some observations can be made concerning commutation conditions during one PWM cycle. In particular, the presence of the overlap time, combined with the reverse blocking diodes characteristics of the CSI topology ensure certain conditions.

- During a PWM period, when the SVM strategy involves the direct transition between two active states (-AB- or -BA-), one of the commutation happens under ZCS and the other is hard switching. This happens for all the SVM.
- For the basic CSI architecture (no S7 present) the same applies when transitioning between a null state and an active state (or vice versa).
- For the CSI7 architectures, all the transitions between a null state and an active state (and vice versa) happen with the reverse blocking switches (S_1-S_6) commutating under ZCS.

As it can be seen from Table IV the switching count is the same for $0A0B$ and $AB0BA$ sequences. With the adopted modulation ($0A0B$), switching losses are all allocated on S7. This can be disadvantageous if all the switches are identical. On the other hand, this can be advantageous to reduce switching losses if a SiC Mosfet is used for S7 (as presented in [20]).

VI. Conclusion

This paper analyzed the performance of the modified three-phase CSI solution based on the introduction of a seventh switch along with the comparison of different SVM strategies. The effectiveness of the CSI7 topology and adopted SVM was compared against the traditional CSI solution by means of simulations and experiments.

This paper puts in evidence the benefits and the critical issues of CSI7 topology, which presents an additional power switch with respect to the traditional CSI solution. The additional switch S7 can be a simple Mosfet or Igbt (without reverse blocking capability) if the power factor operation is

reasonably close to unity. In the adopted SVM the null output vector is obtained by switching on S7: the higher commutation count is counterbalanced by the benefits obtained. In fact the CSI7 topology applied to DC/AC grid connected systems with the proposed SVM is able to:

- Attenuate the excitation of the output CL filter of the CSI without the use of any passive or active damping solutions (reduction of injected grid current distortion).
- Reduce the common mode voltage variations with respect to ground (leakage current reduction).
- Reduce the conduction power losses respect to traditional 6 switches CSI.
- Allow the commutations of S_1 to S_6 to happen under zero current (ZCS).

The experiments proved that the topology is feasible in wide power range String Converter applications, all the way down to single-module converter. It is however more versed to high power applications, as shown by measured efficiencies.

The experimental results showed the improvements of the CSI7 solution in terms of injected current THD, while obviously the conversion efficiency is higher thanks to seven switch. Finally the lower excitation of the common-mode resonant circuit caused by the parasitic capacitance of PV panels with respect to traditional CSI solution was demonstrated. This implies that under the same operating conditions and as shown in the experiments, the CSI7 architecture and adopted SVM are characterized by a lower ground leakage current. The power factor control capability of the CSI and its experimental validation will be the subject of a future work.

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