# Impact of Scattering on Graphene Geometric Diodes: A Comparative Analysis Between Simulations and Experiments

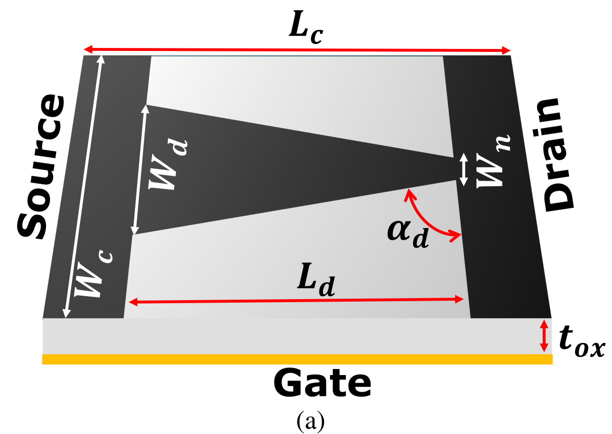
D. Truccolo, A. Hemmetter, P. Palestri, A. Abramo, S. Boscolo, Z. Wang, M. C. Lemme, and M. Midrio

***Abstract*— This work presents a comparative analysis between simulations and experiments aimed at elucidating the origin of the limited asymmetry observed in graphene geometric diodes grown by chemical vapor deposition. Using self-consistent Monte Carlo simulations, we investigate how the effect of various scattering mechanisms progressively suppresses asymmetric transport in geometric diodes. The simulation results highlight that the key parameter governing device performance is the ratio between carriers' mean free path and device length and geometry. Comparison with experiments reveals that for micrometer-scale structures, achieving nonlinear transport in the low-bias regime would require extremely high carrier mobilities.**

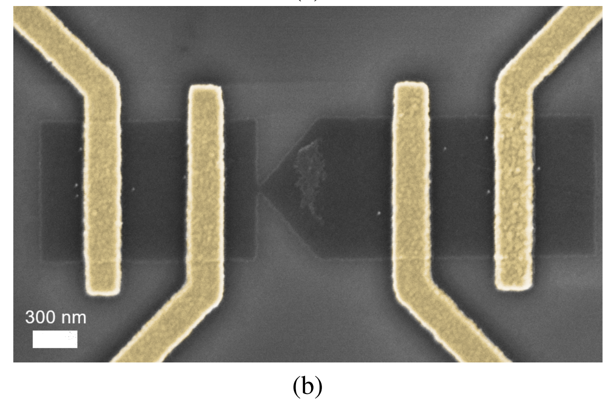
***Index Terms*— Ballistic transport, geometric diode, graphene, Monte Carlo.**

## I. Introduction

GRAPHENE geometric diodes are a novel class of two-terminal rectifiers which have attracted significant interest from the scientific community since their first experimental demonstration [1], [2]. The operating principle of these devices is based on the ratchet effect [3], which appears when the carrier mean free path (MFP) exceeds device dimensions, leading to a "billiard-ball"-like transport regime [4]. Under these conditions, carrier trajectories can be strongly influenced by the device geometry. For the device sketched in Fig. 1(a), the trapezoidal shape of the channel enables an electron flux that is higher when carriers are injected from source (S) to drain (D) and lower in the opposite direction. In fact, in the latter case, most of the injected electrons are backscattered by the long, vertical boundaries, while only a small fraction of them can cross the constriction left open by the short neck




(a)




(b)

Fig. 1. (a) Schematics of the geometric diode. (b) Scanning electron microscope (SEM) image of a fabricated geometric diode. The graphene diode appears darker than the $Si/SiO_2$ substrate. The four contacts (colorized in yellow for clarity) were fabricated with Ti/Au (5/35 nm) to enable the four-probe characterization of the device currents to cancel the role of contact series resistance.

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of width $W_n$. This directional preference is quantified by the asymmetry $A$ of the device current, defined as [1] and [2]

$$A = \frac{I_{DS}(+V_{DS})}{I_{DS}(-V_{DS})} \tag{1}$$

and such asymmetric behavior has been experimentally observed in several studies [1], [2], [5], [6], [7], [8]. Owing to their distinctive operating principle, this kind of graphene diode is free from any sort of built-in potential and is therefore suitable for the rectification of very low-amplitude signals. Furthermore, their parasitic capacitance is extremely small—estimated to be in the order of a few attofarads [2]—thereby allowing them to operate at terahertz (THz) frequencies [9], a regime totally inaccessible to conventional p-n junction diodes. According to models previously developed for ballistic transport in III–V devices with 2-D electron gases [3], to preserve asymmetric behavior, the device dimensions should be maintained lower than the mean free path length of the charge carriers. Typical MFPs in exfoliated graphene samples range between 40 and 70 nm, thus necessitating high-resolution and costly lithography techniques for the fabrication of geometric diodes. Considerable experimental efforts have been devoted to enhancing the mobility of the channel material, usually obtained through the encapsulation of single-crystal exfoliated graphene flakes with hexagonal boronitride (hBN). Despite these efforts, only a few demonstrations of rectification have been reported in micrometer-scale devices under low bias conditions ($I_{DS} < 40\ \mu$A) [5], [7]. In these works, rectification was achieved through exceptional carrier mobilities, ranging between $1 \times 10^5$ and $1.8 \times 10^5$ cm$^2$V$^{-1}$s$^{-1}$ and corresponding to mean free paths between 700 and 900 nm, respectively.

In devices realized using graphene grown by chemical vapor deposition (CVD) and transferred on $SiO_2$ substrates, experimental results [6], [8] have shown asymmetric *I–V* characteristics only for current levels exceeding 100 $\mu$A, with reported MFPs around 70 nm [6]. However, the experimental evidence remains insufficient to develop a comprehensive understanding of the underlying device physics.

Although previous theoretical studies [10], [11], [12], [13], [14], [15], [16] explored the operation principles and proposed optimal geometric designs to enhance the asymmetry factor $A$, systematic investigation of its dependence on key parameters such as carrier mobility $\mu$, applied current $I_{DS}$, and device length $L_d$ is still lacking. The aim of this work is to bridge this gap.

Using self-consistent Monte Carlo simulations, we investigate how different scattering mechanisms, bias conditions, and device dimensions influence the asymmetric transport behavior. Comparison with experimental data allows us to identify the tradeoffs among these parameters and outline the necessary conditions for achieving effective device operations. The remainder of this article is organized as follows.

Section II outlines the simulation framework that was adopted in this study. Section III presents the numerical results obtained, highlighting the impact of scattering on the reduction of the asymmetry, together with a comparison with experimental data. Finally, Section IV draws the conclusions of the work.

## II. Monte Carlo Simulator

The simulator used for this study consists of two main components: a Monte Carlo algorithm that solves the semi-classical Boltzmann transport equation by moving an ensemble of simulated particles along their subsequent free flights and a 3-D Poisson solver that, when coupled self-consistently with the Monte Carlo simulator, provides the electrostatic profile of the entire simulated structure. The simulator we used has already been described in [13], where a detailed description of the carrier transport algorithm and the 3-D Poisson solver was reported. In the following sections, we detail the model extensions introduced in the current implementation, specifically the inclusion of mixed electron–hole transport, additional scattering mechanisms, and a new rejection algorithm to enforce Pauli's exclusion principle.

### A. Mixed Electron–Hole Transport

In this study, electrons and holes are treated as identical particles, differing solely in the sign of their electric charge. Carriers are first attracted to the graphene layer by a positive or negative $V_{GS}$ bias. They are then injected from the $S$ and $D$ contacts as detailed in [13] and moved according to the applied $V_{DS}$ bias. Each injected particle is assigned a statistical weight proportional to its injection current. Electron injection currents are denoted by $\tilde{I}^{el}$ and $\tilde{I}^{ho}$, defined by

$$\tilde{I}^{el}_{\mathcal{C}} = \frac{4qW_c}{\pi}\int_0^{+\infty} d\varepsilon\, DOS(\varepsilon)\, v_f\, f_{\mathcal{C}}(\varepsilon) \tag{2a}$$

$$\tilde{I}^{ho}_{\mathcal{C}} = \frac{4qW_c}{\pi}\int_{-\infty}^{0} d\varepsilon\, DOS(\varepsilon)\, v_f\, (1 - f_{\mathcal{C}}(\varepsilon)) \tag{2b}$$

where $\mathcal{C} = \{D, S\}$ indicates the drain or source contact; $q$ is the elementary charge; $DOS(\varepsilon) = |\varepsilon|/(2\pi v_f^2 \hbar^2)$ is the graphene density of state for single spin and valley; $v_f$ is the Fermi velocity; and $f_{\mathcal{C}}(\varepsilon) = 1/(1 + \exp((\varepsilon - \varepsilon_{f\mathcal{C}})/k_bT))$ is the Fermi–Dirac distribution, with $\varepsilon_{f\mathcal{C}}$ being the Fermi level of the contact $\mathcal{C}$ (that is set to the applied voltages, while the electrostatic potential of the device is adjusted by the 3-D Poisson solver [13]). At each time step, a fixed number of carriers is injected per contact. The type of carrier to be injected is determined probabilistically by evaluating the ratio $\tilde{I}^{ho}_{\mathcal{C}}/(\tilde{I}^{ho}_{\mathcal{C}} + \tilde{I}^{el}_{\mathcal{C}})$ against a uniformly distributed random number $r \in [0, 1]$. If the ratio exceeds $r$, a hole is injected; otherwise, an electron is injected.

### B. Scattering Mechanisms

The interruption of the particles' free flights is attributed to three main scattering mechanisms: intrinsic phonons, remote phonons, and random potential scattering. Intrinsic phonons account for the effects of lattice vibrations in the graphene layer, whereas remote phonons arise from polar interactions between graphene and the $SiO_2$ substrate. Finally, random scattering encompasses various elastic processes, such as those induced by defects and surface roughness. For intrinsic

phonons, the dominant contribution is associated with the combined phonon mode (LA+LO) [17], [18]. The scattering rate for longitudinal acoustic (LA) phonons is given by [19]

$$S_{LA}(\varepsilon) = \frac{1}{4}\frac{2\pi q D_{acou}^2 k_b T}{\rho v_s^2 \hbar} DOS(\varepsilon) \quad (3)$$

where $\rho = 7.6 \times 10^{-7}$ kg m$^{-2}$ is the density of the material, $v_s = 2 \times 10^4$ m s$^{-1}$ is the velocity of sound, and $D_{acou} = 14$ eV represents the deformation potential in the acoustic phonon scattering. The anisotropy due to spinor was removed and plugged into the factor 1/4 [19]. The scattering rate of longitudinal optical (LO) phonons at energy $E_{LO} = 152$ meV is [19]

$$S_{LO}(\varepsilon) = \frac{D_{LO}^2 \pi\hbar}{\rho E_{LO}}\left(n_{ph}(E_{LO}) + \frac{1}{2} \pm \frac{1}{2}\right) DOS(\varepsilon \mp E_{LO}) \quad (4)$$

where $D_{LO} = 10^{11}$ eV/m is the optical deformation potential and $n_{ph}(\varepsilon) = 1/(\exp((\varepsilon)/k_b T) - 1)$ is the phonon occupancy given by the Bose–Einstein statistic.

Remote phonons originating from the $SiO_2$ substrate constitute one of the primary limiting mechanisms of electron mobility in graphene at room temperature [20]. In this work, we consider the dominant $SiO_2$ mode only at energy $\hbar\omega_{TO} = 55.6$ meV. The corresponding graphene remote phonon has a frequency $\omega_{SO} = \omega_{TO}((\epsilon_1 + \epsilon_2^0)/(\epsilon_1 + \epsilon_2^\infty))^{1/2}$, where $\epsilon_2^0$ and $\epsilon_2^\infty$ represent the static and high frequency dielectric constants of $SiO_2$, respectively, and $\epsilon_1$ denotes the dielectric constant of the medium above the graphene layer (air, in our case). Hence, the remote phonon scattering rate is given by [21]

$$S_{rem}(\varepsilon) = \frac{\varepsilon \pm \hbar\omega_{SO}}{\pi\hbar^3 v_f^2}\int_0^\pi d\theta \frac{(1+cos\theta)}{2} H(Q) \quad (5)$$

where $Q = |\vec{k} - \vec{k'}| = (k^2 - 2kk'cos\theta + k'^2)^{1/2}$, in which $k' = k(\varepsilon \pm \hbar\omega_{SO})$ is the magnitude of the particle wave vector after being scattered by the remote phonon, $\theta$ is the angle between the wave vectors $\vec{k}$ and $\vec{k'}$, and

$$H(Q) = \left(n_{ph} + \frac{1}{2} \mp \frac{1}{2}\right) \times \frac{q^2\hbar\omega_{SO}}{2Q}\left(\frac{1}{\epsilon_1 + \epsilon_2^\infty} - \frac{1}{\epsilon_1 + \epsilon_2^0}\right). \quad (6)$$

Scattering with a random potential was introduced to model roughness-induced scattering at the graphene surface but also to model the cumulative effect of other elastic scattering processes not explicitly treated in the model above. Following the approach presented in [22], [23], these processes were modeled using a Gaussian autocorrelation function, which leads to the following expression for the scattering rate:

$$S_{rnd}(\varepsilon) = \frac{\varepsilon}{\hbar^3 v_f^2}(qV_{rnd}L_{corr})^2 \times \int_0^\pi d\theta\ e^{-L_{corr}\left|\vec{k}(\varepsilon)\right| sin(\theta/2)} \quad (7)$$

where we assumed a fixed correlation length $L_{corr} = 1$ nm and the deformation potential $V_{rnd}$ was tuned to control the impact of this cumulative scattering process on carrier transport.

### C. Enforcing Pauli's Exclusion Principle

In low-DOS materials such as graphene, the Pauli exclusion principle must be taken into account. The standard procedure in MC simulations involves the evaluation of the occupation function $f(\vec{r}, \vec{k}, t)$ on a discretized $k$ space grid at each spatial point. Based on the computed values of $f(\vec{r}, \vec{k}, t)$, the final state after a scattering event can be accepted or rejected [24]. In this framework, several MC methodologies and simulators have been specifically developed to incorporate the Pauli principle in graphene transport modeling [25], [26], [27]. However, all of the aforementioned techniques entail a significant memory and computational burden, making them impractical in the simulation of large-scale structures, such as those considered in this study. To overcome this limitation, we adopted a simplified rejection algorithm based on the assumption that the final-state distribution can still be approximated by a Fermi–Dirac, even though evaluated at a temperature other than room temperature [28], [29]

$$f_{approx}\left(\varepsilon, \mu_{el}(\vec{r}), T_{el}(\vec{r})\right) = \frac{1}{1 + \exp\left(\frac{\varepsilon - \mu_{el}}{k_b T_{el}}\right)} \quad (8)$$

where $\mu_{el}(\vec{r})$ denotes the local quasi-Fermi level, evaluated from the electron density at each spatial mesh point, and $T_{el}(\vec{r})$ represents the corresponding electron temperature. After each scattering event, $f_{approx}$ is evaluated at the position of each particle. If $f_{approx}(\varepsilon, \mu(\vec{r}), T_{el}(\vec{r})) > r$, where $r$ is a uniformly distributed random number in the interval [0, 1], the final state is rejected; otherwise, it is accepted. For holes, a dual approach is adopted by defining the quasi-Fermi level for holes ($\mu_{ho}(\vec{r})$), and the hole temperature ($T_{ho}(\vec{r})$). In this case, the final state is accepted if $(1 - f_{approx}(-\varepsilon, \mu_{ho}(\vec{r}), T_{ho}(\vec{r}))) > r$, otherwise, it is rejected.

## III. Results

This section is organized into two parts. In the first part, we identify the optimal operating conditions of the device and examine how a reduction in mobility progressively reduces its asymmetry, ultimately leading to its complete suppression. The analysis will demonstrate that the ratio between the mean free path and the characteristic length $L_d$ [see Fig. 1(a)], rather than mobility itself, is the fundamental parameter governing the performance of the device.

The second part of this section is devoted to the comparison between the simulated and the experimental $I$–$V$ characteristics of a fabricated geometric diode. This comparison not only serves to validate the proposed simulation framework, but it also provides valuable insights into the possible origins of the limited asymmetry observed in many experimental devices.

### A. Asymmetry Factor Under Different Scattering Configurations

As demonstrated in our previous work [13], the geometrical parameters that mainly govern the asymmetry factor $A$ are the ratio $W_d/W_n$ and the angle $\alpha_d$. In particular, we observed that the asymmetry reaches a maximum for $\alpha_d \approx 80°$. On this basis, the diode investigated in the following simulations

has the following parameters: $W_n = 10$ nm, $W_d = 40$ nm, $L_d = 90$ nm, $L_c = 210$ nm, and an opening angle of $\alpha_d = 80^\circ$ [see Fig. 1(a)]. The graphene is assumed to sit on a $SiO_2$ substrate with oxide thickness $t_{ox} = 100$ nm. Neither surface nor oxide charge is considered and the graphene is assumed to be undoped. The band alignments are such that we have flat-band conditions for $V_{GS} = 0V$.

Since electrons and holes were assumed identical but with opposite charge signs, please note that the behavior of the device, as will be described from now on, is going to be symmetric with respect to the carrier type and to the choice of devised applied bias, $V_{GS}$ and $V_{DS}$, positive or negative, respectively. For this reason and without loss of generality, the analysis that follows will focus on electrons only.

To determine the gate voltage that maximizes the asymmetry, we initially considered a ballistic transport regime, which accentuates geometric effects and allows for a clearer identification of the optimum. The resulting asymmetry as a function of gate voltage is shown in Fig. 2(a) for different source-to-drain bias voltages $V_{DS}$.[1] We note that the asymmetry $A$ goes to 1 as $V_{GS}$ approaches 0 V, because the populations of holes and electrons tend to equalize and this suppresses the asymmetric effects induced by the device geometry. The maximum asymmetry is observed at a gate voltage of approximately $V_{GS} \approx 1$ V, at which the average hole and electron densities are approximately $4 \times 10^{10}$ cm$^{-2}$ and $3 \times 10^{11}$ cm$^{-2}$, respectively. In line with the explanation in [13], again from Fig. 2(a), we observe a decrease in the asymmetry for increasing gate voltage.

As stated above, in this study, we assumed an undoped graphene layer. Qualitatively, the presence of doping would shift the charge neutrality point (CNP) toward higher gate voltages without modifying the overall qualitative trend of Fig. 2(a). This hypothesis is supported by experimental data [5], [6], [7], [8], which exhibit behaviors consistent with the trend shown in Fig. 2(a) in the vicinity of the CNP. Fig. 2(b) reports the *I–V* characteristic of the geometric diode for different transport conditions, while Fig. 2(c) shows the corresponding asymmetry plot, $A(V_{DS})$.In the case of intrinsic phonons only (golden line), the numerical evaluation of the electron mobility[2] provided a value $\mu \approx 10^5$ cm$^2$V$^{-1}$s$^{-1}$, typical for hBN-encapsulated graphene [30]. When both intrinsic and remote phonon scatterings are included (brown line), the electron mobility was numerically estimated to decrease to $\approx 10^4$ cm$^2$V$^{-1}$s$^{-1}$, which is typical for exfoliated graphene on a $SiO_2$ substrate [31], [32]. Finally, in the presence of intrinsic, remote, and random scattering (with $V_{rnd} = 0.5$ eV in this case, purple line), the electron mobility further reduces to $\approx 10^3$ cm$^2$V$^{-1}$s$^{-1}$, reflecting the behavior of CVD-grown graphene on $SiO_2$ substrates, typically affected by scattering with impurities and interaction with a significant amount of surface roughness.

From the analysis of *I–V* characteristics, it can be observed that, at least in the device we simulated, intrinsic phonon scattering has a negligible impact on the degradation of transport asymmetry. The inclusion of remote phonon scattering leads to a further reduction of the asymmetry, but the nonlinear behavior of the device is still preserved. However, when random scattering is introduced, the nonlinearity is almost completely lost, and the device tends to behave as a simple ohmic resistor. A more detailed analysis of the link between electron mobility and asymmetry is shown in Fig. 2(d). The plot reveals that ballistic transport is not strictly required to achieve a functional geometric diode. In fact, asymmetry values that exceed 1.1 can already be obtained, provided that mobility is higher than $10^3$ cm$^2$V$^{-1}$s$^{-1}$. This finding is significant because it indicates that geometric diodes fabricated from CVD-grown graphene—whose mobilities routinely reach this range [33], [34]—can indeed exhibit rectification.

We postulate that the key parameter controlling asymmetry is the ratio between the length $L_d$ and the mean free path of the carriers in graphene (MFP). Recalling that MFP can be directly related to mobility $\mu$ and carrier density $n$ (MFP $\approx \mu(h/2e)(n/\pi)^{1/2}$ [35]), we expect scatterings to have a negligible impact when $L_d$ is comparable to MFP, allowing the device to exhibit its asymmetric response. In contrast, when the ratio between MFP and $L_d$ decreases, scattering probability rises and asymmetry diminishes. This hypothesis was proved numerically by scaling the reference device (which we denote as X1 in Fig. 3 and whose results are shown in Fig. 2) by subsequent factors of 2, 3, and 4 (denoted as X2–X4, respectively) while maintaining identical geometric ratios. To ensure consistency, the bias voltage $V_{DS}$ was chosen to produce comparable electric field profiles in all structures. Under ballistic conditions, all devices exhibit the same asymmetry ($A = 1.22 - 1.24$), as shown in Fig. 3(a). However, when mobility is kept constant, the asymmetry reduces as the ratio of the mean free path to $L_d$ decreases [see Fig. 3(b)] In fact, the ballistic asymmetry is preserved for MFP$/L_d \geq 1$, while it declines for MFP$/L_d < 1$, approaching unity at MFP$/L_d < 10^{-2}$ at which point rectification is fully suppressed. Fig. 3(b) shows that when the MFP is normalized to the length of the device, the trends converge to a universal one, consistent across all devices with identical geometric proportions. This universal behavior becomes particularly evident in larger structures (e.g., X3 and X4), where electrostatics in the neck region play a relatively minor role.

### B. Comparison With Experimental Data

Several geometric diodes were fabricated using commercial CVD-grown monolayer graphene on Si/$SiO_2$ substrates (the thickness of the silicon substrate is 279 $\mu$m with a resistivity of 10 $k\Omega$cm) with a process like the one outlined in [8]. Graphene was transferred from a copper foil growth substrate to the Si/$SiO_2$ substrate using a wet transfer process. The graphene diode channels were defined by electron-beam lithography with an acceleration voltage of 100 kV and patterned using

[1] In this work, the condition $V_{DS} > 0$ V refers to the application of a positive voltage to the D terminal wrt. grounded S, while $V_{DS} < 0$ V corresponds to the opposite configuration.

[2] The electron mobility value was estimated by simulating a stripe of infinite length along the $x$-direction, with a constant electric field $E_x$. In the low-voltage regime, the electron mobility is determined as $v_x = \mu_{el} E_x$, where $v_x$ is the average drift velocity of electrons in the $x$-direction, as numerically evaluated in the simulation.

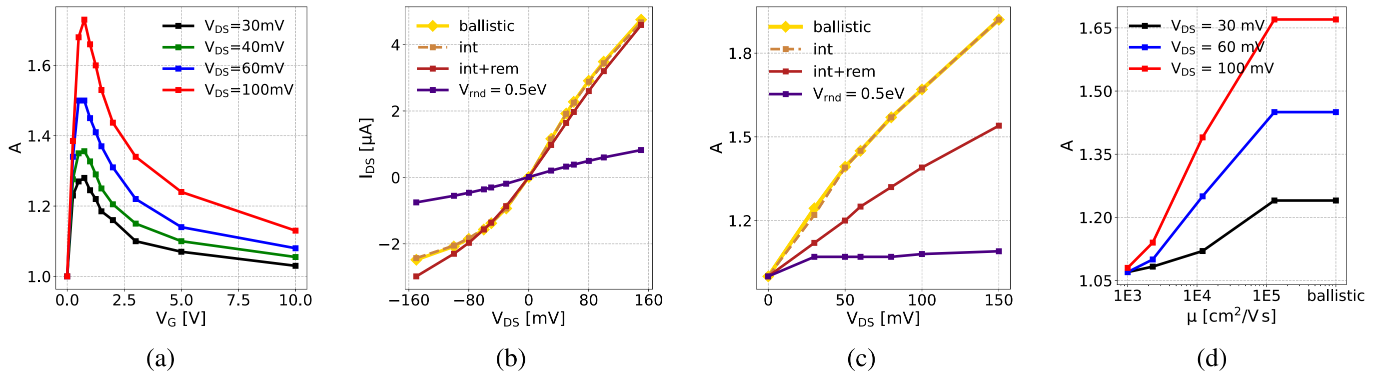


Fig. 2. (a) Behavior of the current asymmetry $A$ as a function of gate voltage $V_{GS}$ for various applied voltages $V_{DS}$ under ballistic regime conditions. (b) $I$–$V$ characteristic and the corresponding asymmetry plot (c) for different transport conditions. Yellow line: ballistic transport, gold line: transport with intrinsic phonons, brown line: transport with intrinsic and remote phonons, and purple line: transport with intrinsic and remote phonons with the addition of random scattering ($V_{rnd}$ = 0.5 eV). The gate voltage considered is $V_{GS}$ = 1 V. (d) Behavior of the asymmetry $A$ as a function of the electron mobility. The results were obtained for a device with a length of $L_d$ = 90 nm.

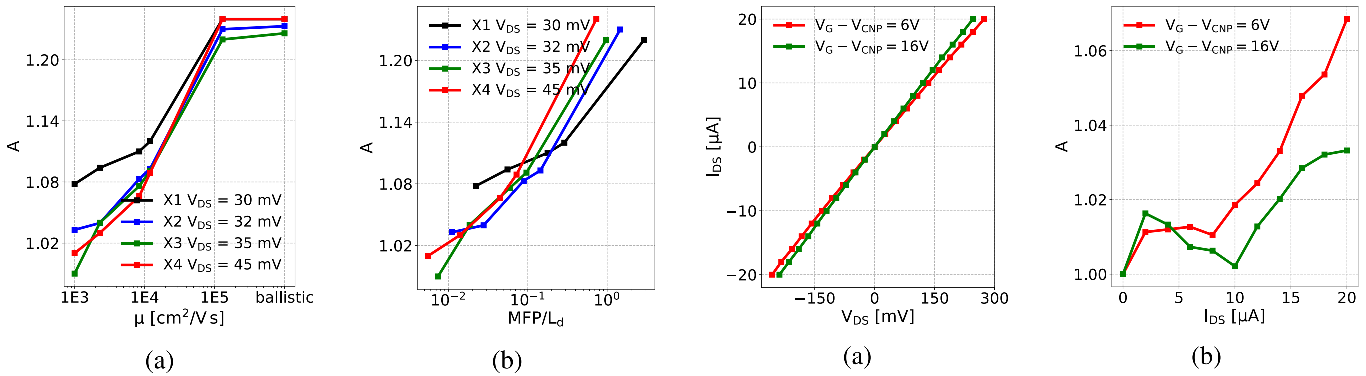


Fig. 3. (a) Asymmetry $A$ as a function of electron mobility $\mu$ for various device dimensions. (b) Asymmetry $A$ as a function of the ratio MFP/$L_d$. The black lines correspond to a reference device with parameters $W_n$ = 10 nm, $W_d$ = 40 nm, $L_d$ = 90 nm, and $\alpha_d$ = 80° (denoted as X1). The blue, green, and red lines represent scaled devices with dimensions 2× (X2), 3× (X3), and 4× (X4) larger than the reference device, respectively. The applied $V_{DS}$ has been chosen to maintain a similar electric field 2-D profile along the different devices.

Fig. 4. (a) Measured $I$–$V$ characteristics and (b) corresponding asymmetry plot $A(I_{DS})$ of the fabricated geometric diode at various gate voltages $V_{GS}$.

dry etching with oxygen plasma. For each diode, four Ti/Au (5/35 nm) top contacts were deposited by evaporation, followed by a lift-off step. A scanning electron microscope (SEM) image of a finished graphene geometric diode is shown in Fig. 1(b), with its metallic contacts colored in yellow for clarity. In this study, we focus on a representative fabricated device characterized by the following geometric parameters: $W_n$ = 50 nm, $W_d$ = 1 $\mu$m, $L_d$ = 400 nm, $L_c$ = 1 $\mu$m, $\alpha_d$ = 40°, and oxide thickness $t_{ox}$ = 300 nm. Although this device does not represent the optimal configuration ($\alpha_d$ = 40° corresponds to a weak rectification effect; see [13]), it was selected for the shortest $L_d$, leading to a larger MFP/$L_d$ ratio.

The device was characterized by four-probe DC measurements, with a global back gate voltage $V_{GS}$ applied to the substrate. The charge neutrality point was identified at approximately $V_{CNP}$ = 24 V, obtained by transfer measurements from the minimum of the $I_{DS}(V_{GS})$ curve. In this method, a $I_{DS}$ current sweep from −20 to 20 $\mu$A (in steps of 2 $\mu$A) is applied at the outer terminals, while the voltage drop, $V_{DS}$, across the inner terminals is recorded. The four-probe setup effectively eliminates the contribution of the graphene-metal contact resistance, and the low current reduces the undesired contribution of the Seebeck effect to the rectification. In this case, the rectification asymmetry was quantified as $A = V_{DS}(+I_{DS})/V_{DS}(-I_{DS})$, where $V_{DS}$ is the voltage measured between the inner terminals [see Fig. 1(b)].

The $I_{DS}(V_{DS})$ characteristics and corresponding asymmetry plots at different gate voltages are presented in Fig. 4(a) and (b). Curves are seen to be nearly linear for all gate voltages. Consistently, Fig. 4(b) shows low values of $A$, with a modest increase as $I_{DS}$ increases.

To investigate the origin of the limited asymmetry observed in the fabricated device, simulations were performed under different transport conditions, as reported in Fig. 5. Specifically, Fig. 5(a) presents the $I$–$V$ characteristic, while Fig. 5(b) shows the corresponding asymmetry trend at a gate voltage of $V_{GS}$ = 6 V. Simulations show that if the transport regime were ideally ballistic (yellow lines), a maximum asymmetry $A$ = 1.20 at $V_{DS}$ ≈ 200 mV could be reached with the fabricated geometry. When intrinsic phonon scattering is added to the mode (gold lines), the numerically estimated value for MFP/$L_d$ is approximately equal to 0.7. This, in turn, causes

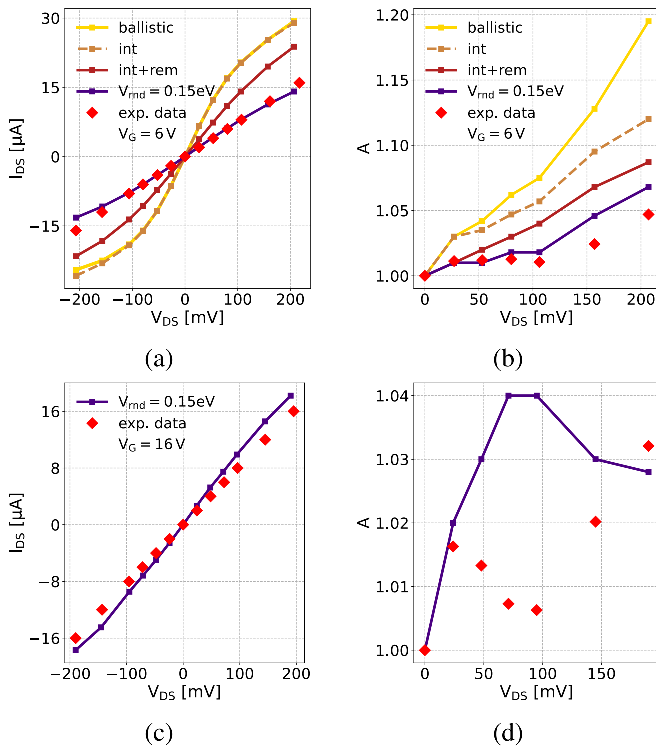


Fig. 5. Comparison between simulations under different transport conditions and experimental data of the fabricated device. (a) Current–voltage characteristics and (b) asymmetry plot at a gate voltage of $V_{GS}$ = 6 V ($V_{GS} - V_{CNP}$ = 6 V for the experimental data). (c) and (d) Corresponding plots at $V_{GS}$ = 16 V. In both figures, red dots represent experimental measurements, while purple lines denote simulations that include all scattering mechanisms and $V_{rnd}$ = 0.15 eV, reproducing the experimental conditions.

the asymmetry to decrease to $A = 1.12$. The further inclusion of remote phonon scattering (brown lines) reduces the ratio to MFP/$L_d \approx 0.1$, leading to a further suppression of the asymmetry to $A = 1.08$. Finally, purple curves represent the simulation conditions in which all scattering mechanisms are activated to reproduce the experimental situation. The random potential $V_{rnd}$ was used as a fit parameter. The best agreement with the experiments was obtained for $V_{rnd} = 0.15$ eV. In this case, the estimated mobility is about 3000 cm$^2$V$^{-1}$s$^{-1}$, resulting in a ratio MFP/$L_d \approx 10^{-2}$. The comparison between simulations and experiments in Fig. 5(a) shows good mutual agreement, although the simulations slightly overestimate the current for $V_{DS} > 100$ mV. The discrepancy is more pronounced at higher gate voltages. Fig. 5(c) and (d) ($V_{GS}$ = 16 V) shows that the deviation increases with $V_{DS}$. The trend is due to intrinsic model limitations, mainly the approximation adopted for carrier rejection under a Fermi–Dirac distribution. The assumption is accurate for $V_{DS} \to 0$ V, which explains the overestimation of simulations at larger biases.

## IV. Conclusion

In this work, we investigated how different scattering processes diminish the asymmetry of graphene-based geometric diodes. Using Monte Carlo simulations, we identified the optimal operating conditions in the mixed electron–hole transport regime and examined how the cumulative effect of different scattering mechanisms progressively drives the device toward ohmic behavior. Comparison between simulations and experimental data complemented our analysis, allowing us to validate the model and quantify its range of validity. We established that achieving proper diode functionality requires MFP/$L_d > 0.1$. This condition sets stringent requirements for graphene quality, fabrication, and geometry, all of which must be carefully optimized to realize consistent rectification.

## References

[1] G. Moddel, Z. Zhu, S. Grover, and S. Joshi, "Ultrahigh speed graphene diode with reversible polarity," *Solid State Commun.*, vol. 152, no. 19, pp. 1842–1845, Oct. 2012.

[2] Z. Zhu, S. Joshi, S. Grover, and G. Moddel, "Graphene geometric diodes for terahertz rectennas," *J. Phys. D, Appl. Phys.*, vol. 46, no. 18, Apr. 2013, Art. no. 185101, doi: 10.1088/0022-3727/46/18/185101.

[3] A. Song, "Electron ratchet effect in semiconductor devices and artificial materials with broken centrosymmetry," *Appl. Phys. A, Solids Surf.*, vol. 75, no. 2, pp. 229–235, 2002.

[4] C. W. J. Beenakker and H. van Houten, "Billiard model of a ballistic multiprobe conductor," *Phys. Rev. Lett.*, vol. 63, no. 17, pp. 1857–1860, Oct. 1989, doi: 10.1103/physrevlett.63.1857.

[5] V. H. Nguyen et al., "Optimum design for the ballistic diode based on graphene field-effect transistors," *NPJ 2D Mater. Appl.*, vol. 5, no. 1, p. 89, 2021.

[6] H. Wang et al., "CVD-grown monolayer graphene-based geometric diode for THz rectennas," *Nanomaterials*, vol. 11, no. 8, p. 1986, Aug. 2021. [Online]. Available: https://www.mdpi.com/2079-4991/11/8/1986

[7] H. Wang et al., "A graphene geometric diode with the highest asymmetry ratio and three states gate-tunable rectification ability," *Adv. Electron. Mater.*, vol. 10, no. 4, 2023, Art. no. 2300695.

[8] V. Passi, A. Gahoi, and M. C. Lemme, "Enhanced asymmetry in monolayer graphene geometric diodes," in *Proc. Silicon Nanoelectronics Workshop (SNW)*, Jun. 2017, pp. 137–138.

[9] Z. Zhu, S. Joshi, and G. Moddel, "High performance room temperature rectenna IR detectors using graphene geometric diodes," *IEEE J. Sel. Topics Quantum Electron.*, vol. 20, no. 6, pp. 70–78, Nov. 2014.

[10] D. Dragoman and M. Dragoman, "Geometrically induced rectification in two-dimensional ballistic nanodevices," *J. Phys. D, Appl. Phys.*, vol. 46, no. 5, Jan. 2013, Art. no. 055306, doi: 10.1088/0022-3727/46/5/055306.

[11] J. Stearns and G. Moddel, "Simulation of Z-shaped graphene geometric diodes using particle-in-cell Monte Carlo method in the quasi-ballistic regime," *Nanomaterials*, vol. 11, no. 9, p. 2361, Sep. 2021. [Online]. Available: https://www.mdpi.com/2079-4991/11/9/2361

[12] D. Mencarelli, G. M. Zampa, and L. Pierantoni, "Current-voltage characterization of multi-port graphene based geometric diodes for high-frequency electromagnetic harvesting," *IEEE Access*, vol. 10, pp. 123251–123258, 2022.

[13] D. Truccolo, P. Palestri, D. Esseni, S. Boscolo, and M. Midrio, "Comprehensive analysis of graphene geometric diodes: Role of geometrical asymmetry and electrostatic effects," *IEEE Trans. Electron Devices*, vol. 71, no. 2, pp. 1294–1301, Feb. 2024.

[14] E. Mohebbi et al., "Towards graphene-based asymmetric diodes: A density functional tight-binding study," *Nanosc. Adv.*, vol. 6, no. 5, pp. 1548–1555, 2024, doi: 10.1039/d3na00603d.

[15] K. Y. Rakhimov, H. T. Yusupov, S. R. Nurmatov, A. Chaves, and G. R. Berdiyorov, "Wave-packet rectification in graphene with alternating circular electrostatic potential barriers," *J. Appl. Phys.*, vol. 137, no. 14, Apr. 2025, Art. no. 144302, doi: 10.1063/5.0250401.

[16] D. Mencarelli et al., "Large-area geometric diodes based on asymmetric and nonlinear transport in patterned graphene," *IEEE J. Multiscale Multiphys. Comput. Techn.*, vol. 10, pp. 315–323, 2025.

[17] R. S. Shishir and D. K. Ferry, "Velocity saturation in intrinsic graphene," *J. Phys., Condens. Matter*, vol. 21, no. 34, Jul. 2009, Art. no. 344201, doi: 10.1088/0953-8984/21/34/344201.

[18] R. S. Shishir, F. Chen, J. Xia, N. J. Tao, and D. K. Ferry, "Room temperature carrier transport in graphene," *J. Comput. Electron.*, vol. 8, no. 2, pp. 43–50, Jun. 2009.

[19] M. Bresciani, P. Palestri, D. Esseni, and L. Selmi, "Simple and efficient modeling of the E–k relationship and low-field mobility in graphene nano-ribbons," *Solid-State Electron.*, vol. 54, no. 9, pp. 1015–1021, 2010. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0038110110001553

[20] S. Fratini and F. Guinea, "Substrate-limited electron dynamics in graphene," *Phys. Rev. B, Condens. Matter*, vol. 77, no. 19, May 2008, Art. no. 195415. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.77.195415

[21] M. Bresciani, P. Palestri, D. Esseni, L. Selmi, B. Szafranek, and D. Neumaier, "Interpretation of graphene mobility data by means of a semiclassical Monte Carlo transport model," *Solid-State Electron.*, vol. 89, pp. 161–166, Nov. 2013. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0038110113002773

[22] S. M. Goodnick, D. K. Ferry, C. W. Wilmsen, Z. Liliental, D. Fathy, and O. L. Krivanek, "Surface roughness at the Si(100)-$SiO_2$ interface," *Phys. Rev. B, Condens. Matter*, vol. 32, pp. 8171–8186, Dec. 1985. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.32.8171

[23] D. Esseni, P. Palestri, and L. Selmi, *Nanoscale MOS Transistors: Semi-Classical Transport and Applications*. Cambridge, U.K.: Cambridge Univ. Press, 2011.

[24] P. Lugli and D. K. Ferry, "Degeneracy in the ensemble Monte Carlo method for high-field transport in semiconductors," *IEEE Trans. Electron Devices*, vol. ED-32, no. 11, pp. 2431–2437, Nov. 1985.

[25] V. Romano, A. Majorana, and M. Coco, "DSMC method consistent with the Pauli exclusion principle and comparison with deterministic solutions for charge transport in graphene," *J. Comput. Phys.*, vol. 302, pp. 267–284, Dec. 2015. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0021999115005768

[26] M. Coco, P. Bordone, L. Demeio, and V. Romano, "Pauli principle and the Monte Carlo method for charge transport in graphene," *Phys. Rev. B, Condens. Matter*, vol. 104, no. 20, Nov. 2021, Art. no. 205410. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.104.205410

[27] A. Paussa et al., "Simulation of the performance of graphene FETs with a semiclassical model, including band-to-band tunneling," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1567–1574, May 2014.

[28] M. V. Fischetti and S. E. Laux, "Monte Carlo analysis of electron transport in small semiconductor devices including band-structure and space-charge effects," *Phys. Rev. B, Condens. Matter*, vol. 38, no. 14, pp. 9721–9745, Nov. 1988. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.38.9721

[29] M. Zebarjadi, C. Bulutay, K. Esfarjani, and A. Shakouri, "Monte Carlo simulation of electron transport in degenerate and inhomogeneous semiconductors," *Appl. Phys. Lett.*, vol. 90, no. 9, Feb. 2007, Art. no. 092111, doi: 10.1063/1.2709999.

[30] L. Banszerus et al., "Ballistic transport exceeding 28 $\mu$m in cvd grown graphene," *Nano Lett.*, vol. 16, no. 2, pp. 1387–1391, 2016.

[31] V. E. Dorgan, M.-H. Bae, and E. Pop, "Mobility and saturation velocity in graphene on $SiO_2$," *Appl. Phys. Lett.*, vol. 97, no. 8, Aug. 2010, Art. no. 082112, doi: 10.1063/1.3483130.

[32] K. Nagashio, T. Yamashita, J. Fujita, T. Nishimura, K. Kita, and A. Toriumi, "Impacts of graphene/$SiO_2$ interaction on FET mobility and Raman spectra in mechanically exfoliated graphene films," in *IEDM Tech. Dig.*, Dec. 2010, pp. 1–4.

[33] B. Canto et al., "Multi-project wafer runs for electronic graphene devices in the European 2D-experimental pilot line project," *Nature Commun.*, vol. 16, no. 1, p. 1417, Feb. 2025.

[34] X. Gao et al., "Integrated wafer-scale ultra-flat graphene by gradient surface energy modulation," *Nature Commun.*, vol. 13, no. 1, p. 5410, Sep. 2022.

[35] G. Auton et al., "Graphene ballistic nano-rectifier with very high responsivity," *Nature Commun.*, vol. 7, no. 1, p. 11670, 2016.

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