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Defects in polysilicon channel: Insight from first principles and multi-scale modelling

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ABSTRACT

With increasing demand for essential components in the field of electronic devices, enabling advancements in display technology, flexible electronics, and various industrial applications, thin-film transistors (TFTs) are significant. Their versatility and compatibility with low-temperature fabrication processes make them a vital element in advanced electronic systems. The use of polycrystalline silicon (Poly-Si) as the channel material is specific to TFT applications unlike single-crystal/epitaxial Si in high-performance integrated circuit transistors. Poly-Si is characterized by the presence of defects such as voids, grain boundaries (GBs), and dislocations, that exert detrimental influence on electrical conductivity and then on device performance. Understanding of these would help engineer the novel TFT devices with superior reliability. In this context, Fundamental properties of the GBs are calculated using density functional theory (DFT) and their impact on poly-Si TFTs performance and figures of merit is assessed using the Ginestra® simulation platform. To account the process contaminations, the impact of known lighter impurities on GBs is comprehensively studied. In this paper we show how material properties from DFT can be effectively virtualized to predict electronic device performance, enable fast and reliable evaluation of device sensitivity to material changes, and how outputs of this multi-scale modelling process agree with experiments.

1. Introduction

In recent time, for advanced display technology, particularly for high-resolution and flexible displays, thin-film transistors (TFTs) serve as the essential elements. TFT-based displays offer fast response times, and excellent image quality, making them widely used in televisions, computer monitors, smartphones, tablets, and other portable devices. In addition, TFTs show significant importance in various electronic applications, such as flexible and wearable electronics, large-area electronics (e.g., photovoltaic devices, and sensors) [1–4], and also, they are suitable for portable and battery-operated devices [5–7]. Overall, TFTs are essential components in the field of electronic devices, hence it has become necessary to develop high-performance ones with superior reliability.

One of the key components of TFTs is the semiconducting channel [6,7–9], which can be fabricated using various materials and the choice of channel material depends on the specific requirements of the application. Some commonly used channel materials in TFTs include polycrystalline or amorphous Silicon (poly-Si/a-Si), Indium Gallium Zinc Oxide (IGZO) and organic semiconductors. Moreover, to evaluate the potential of emerging channel materials [5,10] such as organic semiconductors based on small molecule or polymer materials, transition metal dichalcogenides (TMDCs), and carbon based nanomaterials, like carbon nanotubes and graphene are part of ongoing research. Over the past decades a-Si, or hydrogenated a-Si, is became a widely used channel material in TFTs, especially in active-matrix liquid crystal displays [7,8].

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It offers good uniformity, stability, and low OFF state leakage current. However, its carrier mobility is relatively low, limiting its performance in high-speed applications and large drive currents. Therefore, to realize the potential of new generation displays, and to overcome the challenges with performance and reliability issues of hydrogenated a-Si, low-temperature poly-Si have partly replaced these channel materials. Poly-Si has higher carrier mobility compared to a-Si, making it suitable for faster switching speeds and higher ON/OFF current ratios. Poly-Si TFTs provide flexibility in terms of device design and integration where the thin-film nature of poly-Si enables the fabrication of large-area devices, as well as the compatibility with flexible substrates, making it suitable for applications like flexible displays. However, the fabrication of poly-Si TFTs typically involves more complex and costly processes, such as laser crystallization or sequential lateral solidification [5].

For a prior understanding of such devices entangled with material properties and physical mechanism behind, TCAD (Technology Computer-Aided Design) [11,12] modelling serves as a powerful tool that allows to predict the performance of semiconductor devices before fabrication. TCAD tools utilize mathematical and physical models and workflows to gain insights into the underlying physical principles and mechanisms governing device operation. It also facilitates the optimization of device structures and parameters to achieve desired performance targets, optimize designs, and accelerate the development of electronic devices. Recent works focus on various aspects of TCAD simulation and analysis of poly-Si TFTs, including the effects of interface states [9,13], the use of 2D/3D simulations, the application to organic TFTs, and the comparison with amorphous silicon TFTs [12]. They highlight recent advancements and provide insights into the modelling and characterization of poly-Si TFTs using TCAD techniques.

TCAD requires a set of parameters [14]to accurately represent the behavior and the characteristics of the device being modeled. The specific parameters needed may vary depending on the type of device and on the level of information required by the models. In general, parameters are obtained gathering experimental data, or optimized theoretical model based on physical phenomena. Moreover, in a multiscale modelling platform connecting the material properties to the electrical device performance, the atomistic details are crucial. First-principles methods are utilized to calculate the electronic properties that link to material defects.

Despite several advantages that make poly-Si TFTs important in various electronic applications, poly-Si itself, that consists of grains and GBs of various sizes, affects the electrical properties of the material, such as carrier scattering and leakage currents. Many efforts have been made to improve the quality of the poly-Si [5,9,15] via grain boundary engineering and doping optimization [16] to minimize the impact of grain boundaries that are the main limiting factors to high ON current, switching speed and are significantly contributing to the device's variability. In addition, poly-Si, are susceptible to degradation when interstitial impurities are present during the manufacturing processes and conditions.

In this work, we report the impact of the most probable interstitial impurities (that can be incorporated intentionally or unintentionally during the processing) on the performance of the device properties of poly-Si TFTs, considering a combined effort from atomistic simulations and multiscale modelling with three dimensional TCAD analysis. This work is organized as follows: in the first part (sec.2.1) we discuss atomistic details of poly-Si material and DFT computational details, followed by device design with multiscale modelling methodology (sec. 2.2). Sec. 3 is devoted to results and discussion, where sec 3.1 discuss about the device benchmark, afterwards the aspects of GB's intrinsic characteristics and influence of defects are discussed (sec. 3.2 and 3.3). Finally, the conclusions are provided in section 4.

2. Methodology

2.1. Materials description

Grain boundaries (GBs) are the extended defect that appears along the interface between two grains and depending on crystal orientation and atomic arrangement there are different types of GBs in poly-Si material. Experimental studies on poly-Si show that about 50 % of the high angle GBs observed are the $\sum 3$ type and its second and third twin order, $\sum 9$ and $\sum 27$ respectively [17]. Among them, $\sum 3$ (111) plane has the highest stability [18,19]. GBs are known as preferential segregation sites, hence presence of foreign interstitial impurities, as considered for this study, like oxygen, carbon, nitrogen, and hydrogen further affect the electronic properties of the materials [20,21]. The presence of defects and localized states near grain boundaries generates trap states within the band gap, which can trap charge carriers and affect their mobility and recombination behavior. Trap-assisted recombination near grain boundaries can lead to increased recombination rates and reduced device performance [17]. Additionally trapping on those states can also impact the device electrostatically resulting in barriers in the conduction band and scattering mechanism [22,23] which hamper the electron transport.

To assess the discrete properties discussed above, DFT calculations were performed using Vienna Ab-initio Simulation Package (VASP) [24,25]. We employed the hybrid DFT with HSE06 functional [26] and projector augmented wave (PAW) potentials with a cutoff of 400 eV. For the structural optimization, force threshold of 10^{-2} eV/ Å per atom was used. The 192-atoms supercell of $\sum 3$ (111) Si-GB was used to simulate the Si monovacancy in pristine GB and with different (H, C, N, O) interstitial impurity.

We considered three charge states (q = +1, 0, −1) of Si monovacancy for the thermal (E_{th}) ionization to the conduction band calculation by the formula [27,28],

$$E_{th} = E_{opt} - E_{rel} \tag{1}$$

where E_{rel}, E_{opt} is the lattice relaxation energy and optical ionization energy respectively. From total energies of the system, optical and thermal ionization energies for different charge states can be calculated as,

$$E_{opt}(V^q) = E_q\left(V^{q+1}\right) - E_q(V^q) + E^- - E^0 \tag{2}$$

$$E_{rel}\left(V^{q+1}\right) = E_{q+1}\left(V^{q+1}\right) - E_q\left(V^{q+1}\right) \tag{3}$$

E^0 is the total energy of the pristine Si-GB, E^- is the total energy of the pristine Si-GB with an additional electron at the bottom of the conduction band. E_q (V^q) and E_{q+1} (V^{q+1}) is the total energy of Si-GB supercell with a vacancy (V) in charge state q and $q + 1$ respectively in the optimized geometry. E_q (V^{q+1}) is the total energy with a vacancy in the charge state $q + 1$ but at the equilibrium geometry corresponding to the vacancy in the charge state q.

To study the role of H, C, N, O segregation, with vacancy defect in Si-GB (111), different configurations were found, and in Fig. 1 we reported only the lowest energy structures. From Fig. 1 it is clear that Si vacancy interact differently with segregated atomic impurities. These can alter the electronic properties. Due to the diverse segregated variability of different impurities and their varying effects on electronic properties, it is challenging to identify consistent trends. Here we focus on a set of such defect related structures of the poly-Si material for further analysis.

2.2. Construction of device model

The Ginestra® modelling framework [29,30] is a commercially available multiscale platform with various functionalities. It can simulate the operation and reliability of RRAM, FTJ, and 3D-NAND devices used as artificial neurons/synapses [31], as well as understand the

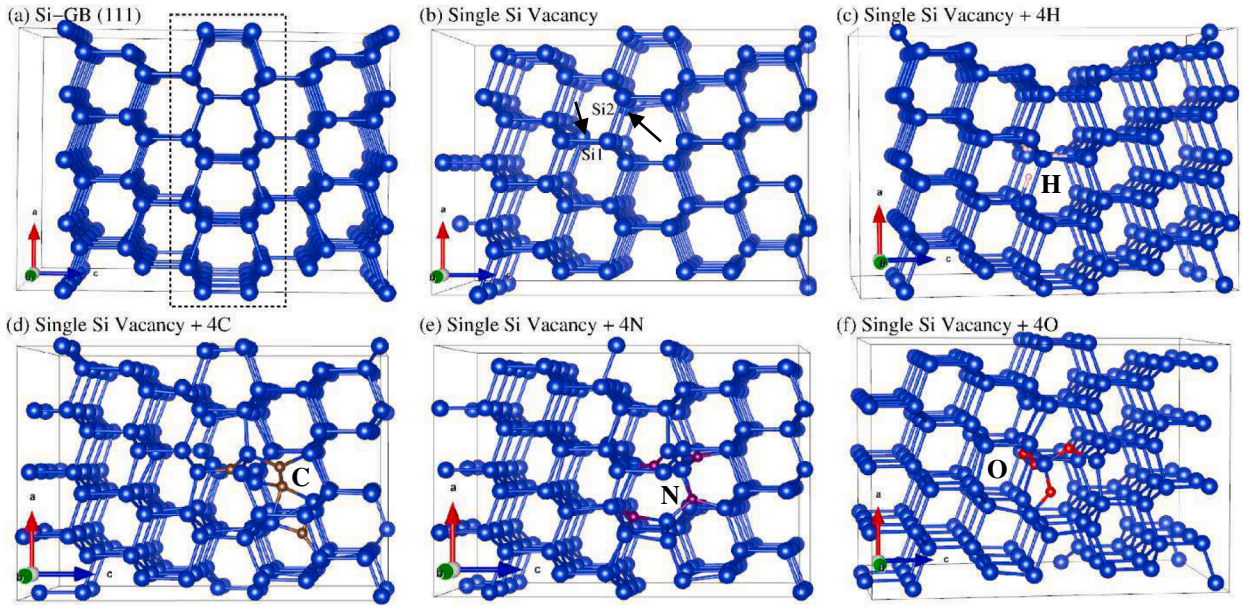

Fig. 1. Polysilicon supercell geometry from atomistic simulations: (a) Pristine Si-GB ∑3 (111), (b) with Si monovacancy (Vac), and interstitial impurity complexes with (c) 4H, (d) 4C, (e) 4 N, (f) 4O. Dashed black box in (a) marked the grain boundary region interfaced with two Si grain on either side. Si1, Si2 (marked by arrow) are the three-fold coordinated Si due to single Si vacancy site at GB. All other elements (H, C, N, O) are marked accordingly in each structure.

reliability challenges and physical mechanisms of ferroelectric-based devices [32], and more [33–35]. The capability of Ginestra® consists of two interconnected parts. It accounts for physical phenomena such as charge transport, charge trapping, material changes (stress-induced or related to specific material properties), and other complex physical mechanisms involved in different operations. It can manage discrete contributions of charge, atomic species, and defects (interstitial ions and vacancies), as well as simulate their diffusion and generation processes. Secondly, the device modelling platform can reproduce electrical device response in DC and pulse conditions, from pristine to degraded stages reached after extensive cycling. This allows identification of key mechanisms controlling the switching and degradation processes in different devices and material stacks. However, a more detailed comparison is beyond the scope of this work, as we focus on the relevance mechanism used for device simulations only.

We utilized Ginestra® TCAD simulation for the poly-Si channel based TFT device. This tool allows us to profile defects, extracting both location and energy within the material stack. It captures the physics of relevant charge-transport and structural material modification phenomena occurring during device operations and aging. This is achieved through a kinetic Monte-Carlo description of individual contributions of atomic defects on the electrical characteristics and degradation processes affecting the long-term device reliability. The model accounts for charge trapping and transport through the device, considering multi-phonon trap-assisted tunnelling (TAT) enabled by the atomic defects in the band gap, along with the drift–diffusion model. Since trap-assisted-tunnelling is related to the presence of defects, it is straightforward to understand that the properties of defects have a strong influence on the TAT itself. Thus, the most relevant parameters that leverage TAT mechanisms are E_{th} and E_{rel} of each defect that is attributed according to the normal distribution with a mean (μ) and standard deviation (σ). These inputs (E_{th} and E_{rel}) are specific to host material (poly-Si) and type of impurities, as calculated from DFT (section 2.1). In the case of TCAD, we modelled the granular structure (Grain/Grain Boundary) of the poly-Si channel as a sequence of adjacent regions with different material and defect properties. In particular, the grain boundaries are characterized by a high concentration of defects, whose properties are inherited by atomistic analysis, while the grains are described as crystalline regions. In Fig. 1, multiple supercell structures of polysilicon with different impurity species are reported: these consist of grain boundary (marked by black dotted box in (a)) and grain (each side of that box), which are used to describe the channel region of the final device, bridging the defect/trap related properties from atomistic to multi-scale modelling platform.

Finally, since the tunnelling path depends on the space position of the defects, as a distinctive features of Ginestra® distribution of a species allows as a volumetric or interface with a peak density that sets the maximum density of the defect distribution. In this paper, we model the drain current through a TFT device as a function of applied gate and drain voltages. Each calculation begins with a randomized distribution of pre-existing defects in the channel layer.

The transfer curve in Fig. 2 illustrates the typical behaviour of p-

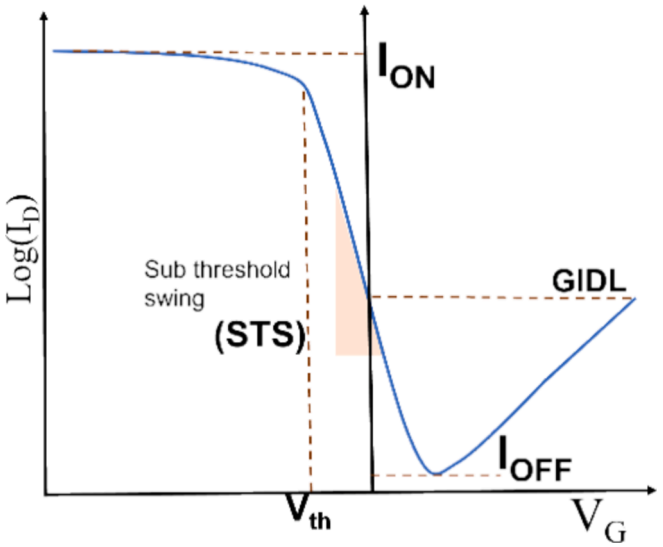

Fig. 2. Sketch of a typical transfer curve for p-TFTs. I_D represent the drain current, V_G is the gate voltage, I_{OFF} is the minimum current. All figure of merits: ON current, threshold voltage, subthreshold swing and gate induced leakage current (GIDL) are marked here. The typical gate-voltage range used to operate a p-TFT is [-25, 5] V with a drain voltage that is around –1 V.

TFTs. In this curve, ON current (I_{ON}) and OFF current (I_{OFF}) are defined as the maximum and minimum currents that can be obtained by applying a gate bias (V_G). Subthreshold swing (STS) is defined as the gate voltage necessary to increase the drain current by a factor of 10 in the sub-threshold region. Gate induced drain leakage (GIDL) is defined as the tunnelling-based leakage currents in an over driven OFF state of the TFT. Threshold voltage (V_{th}) is the minimum gate voltage necessary to allow ON current to flow in the TFT. These are the figures of merit employed hereafter to characterize device performance and they can be all derived once the V_{th} value is defined. Several V_{th} extraction methods are available [36], the constant current method (M1) is one of the most popular, and it defines the threshold voltage V_{th} as the gate voltage needed to observe a predetermined and constant I_D.

3. Results and discussions

3.1. Device benchmark

First, we conducted a TCAD simulation and analysed characteristics of a pristine poly-Si p type TFT (p-TFT) [Fig. 3(a)]. To efficiently simulate in Ginestra leakage characteristics, a modified version of the Generation/Recombination Hurkx model [37] was used to mimic band-to-band tunnelling phenomena. Here the device parameters, such as poly-Si channel length, width of the device, dielectric material (SiO_2), gate electrode (Al) and relative applied voltages at drain (V_D) and gate (V_G) are scaled to calibrate the device. Fig. 3(b) represents results from the analysis of the poly-Si p-TFT with TCAD compared with experimental [5] I_D-V_G characteristic curve, where log scale shows well established calibration. During the device calibration, channels with four grain boundaries are considered. Substrate effect not taken into consideration.

3.2. Impact of poly-Si material properties

- **Grain/GB properties**

Calibrated device fully reproduced the experiment behaviour which allowed us to obtain the band diagram of the channel [Fig. 3(c)] and thus further explored for analysis. In the first step intrinsic properties of the poly-Si, such as electron affinity (χ), defect density (Nt), band gap (Eg), mobility (μ_e) and position (Pos) of four GBs across the channel region Y [Fig. 3(c)] were used to assess variability trends as well as the most impacting parameters on the main figures of merit of the transistor. For this assessment the defect density, mobility was adopted independently for both the poly-Si grain and GBs to fit the experimental I_D-V_G data. Otherwise, for the gap and affinity the ranges are set according to ones calculated from DFT. The summary for simulation parameters is shown in Table 1.

Fig. 4 shows the variability of FOM from simulated transfer characteristics of the p-TFT considering range of all intrinsic parameters as mentioned in the Table 1 on the calibrated device.

Statistical variations of affinity and gap amplitude are, as expected, having a significant impact on all FOMs, in fact, they produce local perturbations of the bands, which affect flow of carriers along transport direction, impacting the electrostatics of the entire device (V_{th} shift and STS degradation). A significant repercussion on the transport is also given by the position of GBs along the channel, suggesting that GB distance from electrodes is relevant as well.

Table 1
Poly-Si properties used in TCAD simulation.

Grain properties		Grain boundary properties	
Electron Affinity	4.05 eV	Electron Affinity	3.82–4.0 eV
Band Gap	1.16 eV	Band Gap	0.9–1.2 eV
Relative permittivity	11.68	Relative permittivity	11.68
Mobility μ_e	300 cm^2/Vs	Mobility μ_e	100–250 cm^2/Vs
Density	1×10^{17} /cm^3	Defect density	2×10^{19}–2×10^{20} /cm^3
		Defect energy $\mu(\sigma)$	0.3 (0.25) [eV] 0.9 (0.1) [eV]

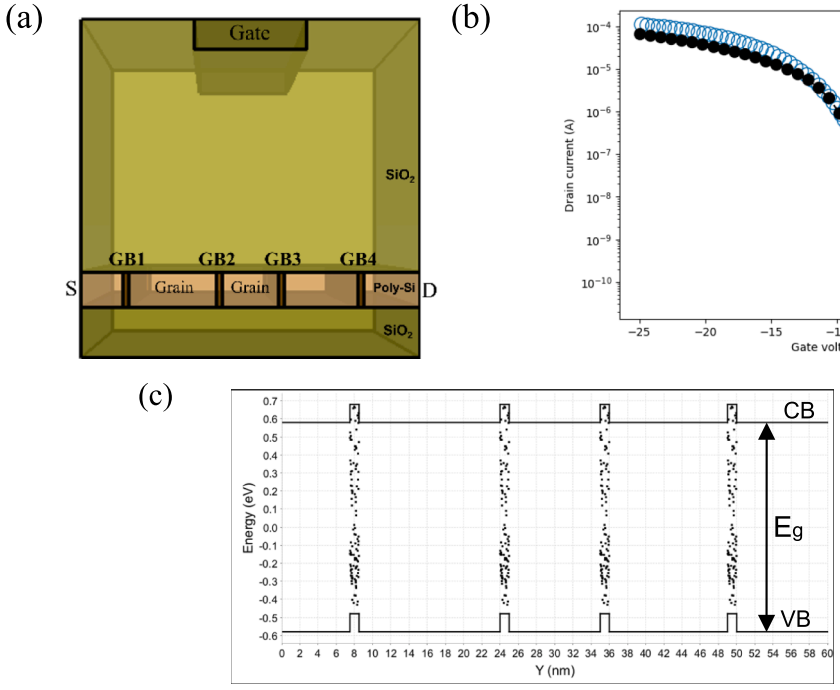

Fig. 3. (a) Schematic view of the TFT device used in TCAD simulation. Poly-Si channel is described with grain and four grain boundary regions (GB1, GB2, GB3, GB4). S, D corresponds to source and drain positions, controlled with top gate. (b) Calibrated Poly-Si p-TFT I_D-V_G with experimental device [9]. (c) Band diagram with valence band (VB), conduction band (CB), band gap (Eg) and, defect distribution along the channel length as considered for calibration. Here, gate oxide = 50 nm, channel width = 10 μm, thickness of the channel = 7 nm, and length = 60 nm.

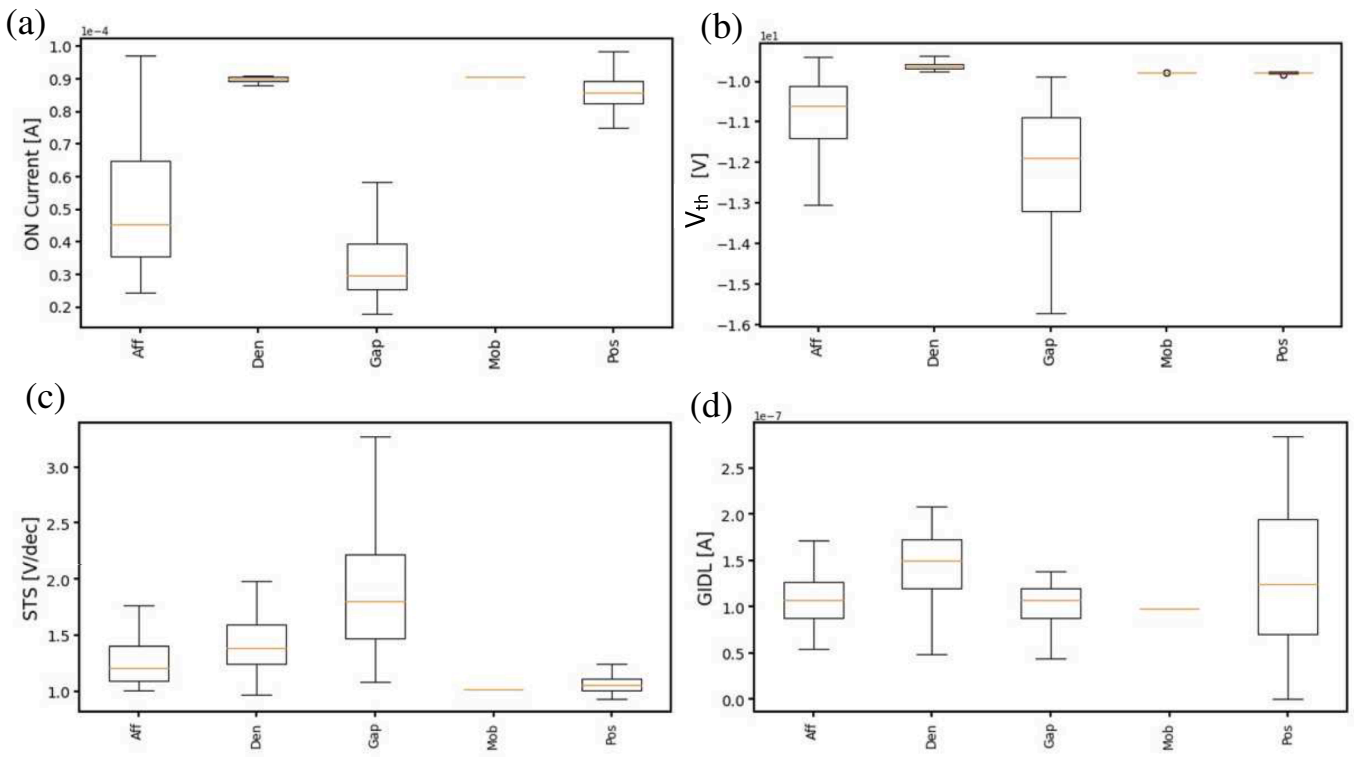

Fig. 4. Material related variability sources and their impact on the four figures of merit (FOM): (a) ON current, (b) V_{th}, (c) STS and (d) GIDL. This is based on four GBs model. Boxplot showing the quartiles and the median following whiskers along with other components.

Results indicate that a defect density increase is highly degrading the STS due to the thermal energy of the distributions employed as defect levels are positioned in the energy gap so that trap and de-trap phenomena are happening during ON-OFF transitions. Notably, mobility variations are producing negligible effect on FOMs as its impact on the drift–diffusion is screened by the other degradation mechanisms.

Following the above analysis, for exploring the impact of the sensitive intrinsic parameters as discussed above, more variability has been explored with increased defectivity of poly-Si (different number of GBs). This analysis is summarized by results in Fig. 5, where it appears evident that, the increasing number of GB regions is directly correlated with the overall degradation of all device properties, as expected. Therefore, the increased defectivity of the channel deteriorates the overall FOMs, suppressing transport (reduction of the ON current, producing a drift in the V_{th} (increase of the V_{th}) and an increase of GIDL and STS. It is important to note that the trends here are consistent with the previous ones, reported in Fig. 4.

- **Grain/GB properties in presence of defects**

To correlate the variability of FOMs due to impurities on poly-Si channel, we investigated vacancy defect and vacancy − interstitial impurity (H/C/N/O) complexes [sec. 2.1]. Defect energy states calculated with DFT, are summarized in Fig. 6 for different charge states and variety of defects are labelled accordingly in the figure as V_{Si}, $4H + V_{Si}$, $4C + V_{Si}$, $4\,N + V_{Si}$ and $4O + V_{Si}$ for Si-vacancy defect in pristine GB and in presence of other segregated impurities.

Generally, defect levels in the mid gap create trap states that significantly affect the carrier transport, hence more detrimental for TFTs' performance. Moreover, the charge transition of the defect levels has an added impact on the transport mechanism and carrier mobility, depending on whether the traps are occupied (charged) or empty (neutral). The density of defect states is equally crucial, as higher defect density increases the likelihood of carrier trapping, recombination, and electrostatic impact on the channel properties in turn affecting the scattering and electron and hole mobility. An impact of the energy levels and defect density [38–45], is studied on transfer characteristics of p-TFT and variability on FOM is shown in Fig. 7. For p-TFT, typically, the acceptor like defects would play the leading role by capturing electrons and creating holes as the dominant carrier. Therefore, the impact on FOM is relatively dominant for vacancy defects [Fig. 7], as expected from the available defect energy levels [Fig. 6]. Moreover, different depth and number of defect levels offered by different defect complexes affect differently the electric FOMs, as clear from Fig. 7.

For N defect, because of poor variability, influence of associated defect levels is not clear from this analysis and the reason is the low defect density is considered. The solid solubility of N in Si is low in equilibrium conditions, within a range of $4.5–6.5 \times 10^{15}$ atoms/cm^3 near the melting point, compared to other common impurities (C, O) [42]. Generally, N interacts with self-interstitials and other impurities, but its interaction with vacancies is determinate due to low concentration. However, under non-equilibrium conditions due to supersaturation of vacancies it led to a significant enhancement of nitrogen-vacancy defects [42,43]. Thus, an increased defect density (same as considered for C) shows a clear impact on all FOMs, in particular on the GIDL.

It is important to note that there is a direct correlation between the degradation trends of each FOM and the defect properties, in particular with the trap thermal ionization energy in the bandgap and its charge state. In fact, the trapping and the de-trapping phenomena depend on defect alignment with the Fermi level during the biasing as well as their electrostatics (empty- or filled-state charge).

Defects positioned very close to carrier's bands (valence band for p-TFT) can be considered as tails of bands, which have a limited impact on the transport, if the associated trap density is small and the positive and/or neutral charge state would not produce strong perturbations. On the other hand, the presence of states in the upper or lower half of the bandgap, depending on the nature of the channel doping, affect more heavily the transport and the transition between the off-state and the on-

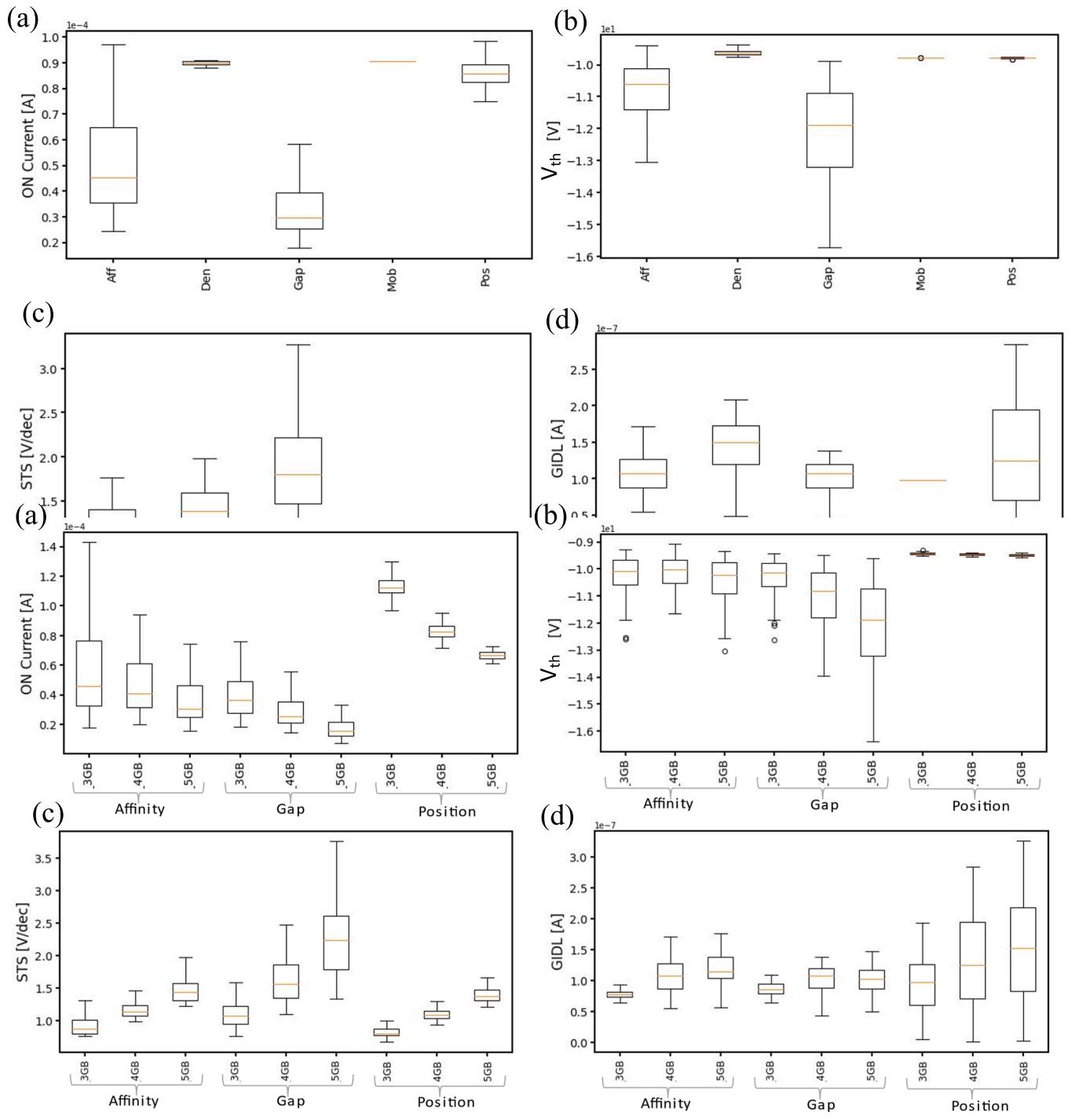

Fig. 5. Poly-Si related variability (affinity, gap, and position of GBs) sources and their impact with increasing number of GBs on the poly-Si channel on the four figures of merit (FOM): (a) ON current, (b) V_{th}, (c) STS and (d) GIDL. Boxplot showing the quartiles and the median following whiskers along with other components.

state (i.e., the STS), as evident in the presence of negative charge state defect for H and Si-vacancy in addition with relative high defect densities compared to C. Moreover, the negative charge state in mid-gap states leads to enhanced leakage (N) compared to others (C and O) irrespective of the low defect density. It is worth noting that the presence of negative defect states near the conduction band is not directly responsible for leakage but can influence overall device performance in combination with the perturbation of the valence band.

Therefore, based on local coordination of differently segregated contaminants (Fig. 1), the defect energy levels, associated charge state and density of defect states within the gap of channel, collectively shows a profound impact on carrier transport.

4. Conclusion

We studied the effects of poly-Si channel on the electrical performance of p-TFTs with modelling by Ginestra® TCAD software. Modelling parameter related to grain boundaries and associated impurities are calculated from first-principles calculations. The position of acceptor and donor-like defect states within the bandgap is a crucial factor in deciding the material's electrical properties. However, the charge transition of mid-gap defect levels as well as density of defect states, all

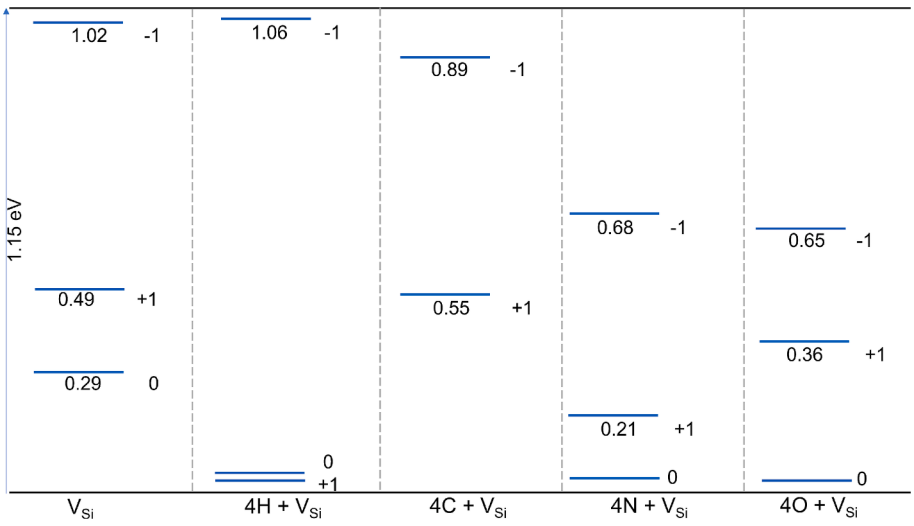

Fig. 6. Defect energy diagram for different charge states with monovacancy (V_{Si}) and with associated different interstitial impurity (4H/4C/4N/4O) complexes in the $\sum$3 (111) Si-GB with respect to the valence band edges.

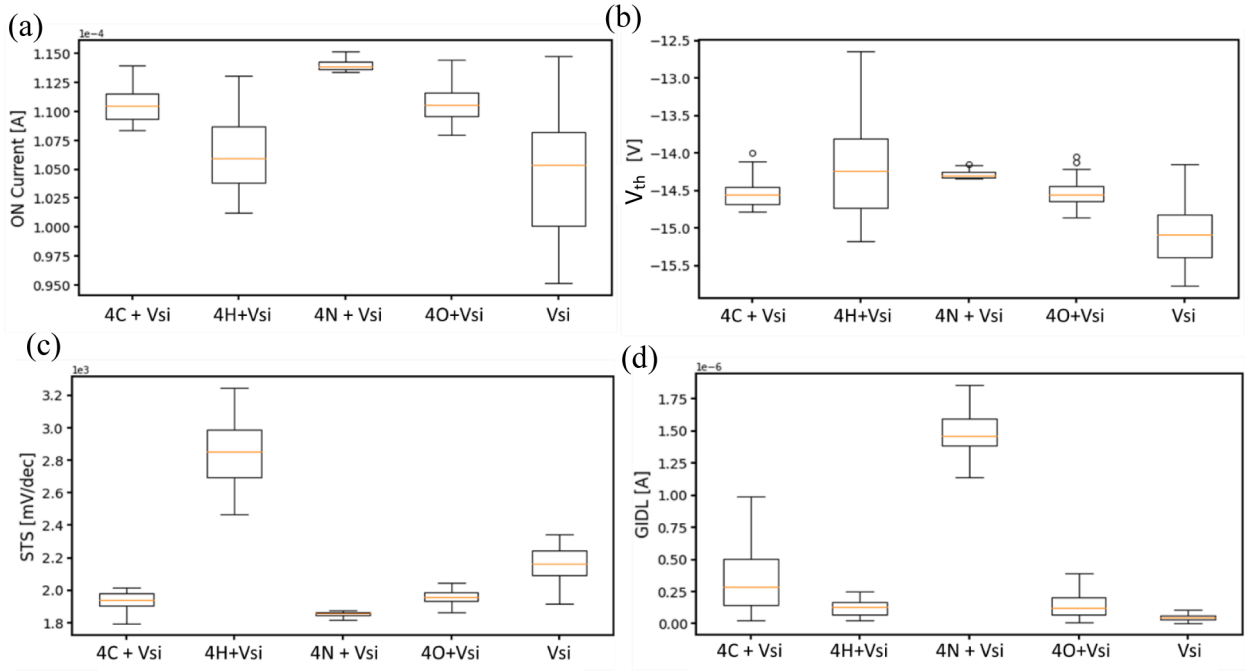

Fig. 7. Impurity related variability for p-TFT (4GBs model) on the four figures of merit (FOM): (a) ON current, (b) V_{th}, (c) STS and (d) GIDL. Boxplot showing the quartiles and the median following whiskers along with other components.

are correlated to have a profound impact on carrier transport. In our study theses influence is clearly distinguishable. Based on impurities present in the poly-Si channel, the combined effect of energy levels and density dictates the overall performance of the channel quality. This can introduce variations in carrier concentration, mobility, and recombination rates. These variations can lead to threshold voltage shifts, changes in the current voltage characteristics, as evident from the detail analysis of the variability on figure of merit.

In this study, for modelling of poly-Si, we have considered only $\sum$3 (111) GB, however there are other variety of Si-GBs available, which have different band gap and based on interfaces and variety of impurities, they would have different defect energy levels and associated charge transition levels. A more detailed analysis is however beyond the scope of this study and could be future part of extension.

In summary, based on impurities present in the poly-Si channel, the charge transition of mid-gap defect levels, or traps, can introduce variations in carrier concentration, mobility, and recombination rates. These variations can lead to threshold voltage shifts, changes in the current–voltage characteristics, and, in some cases, instability in the performance of semiconductor devices like TFTs. Therefore, minimizing the presence and effects of mid-gap defect levels is essential for optimizing the transport properties of semiconductors in electronic devices.

CRediT authorship contribution statement

R. Maji: Writing – original draft, Investigation, Formal analysis, Data curation, Conceptualization. **T. Rollo:** Writing – review & editing, Validation, Investigation, Conceptualization. **S. Gangopadhyay:** Writing – review & editing. **E. Luppi:** Writing – review & editing. **E. Degoli:** Writing – review & editing, Supervision, Project administration,

Funding acquisition. **F. Nardi:** Supervision, Project administration. **L. Larcher:** Supervision, Project administration. **M. Pešić:** Writing – review & editing, Supervision, Project administration, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

References

[1] Ana Claudia Arias, J. Devin MacKenzie, Iain McCulloch, Jonathan Rivnay, and Alberto Salleo, Materials and Applications for Large Area Electronics: Solution-Based Approaches, Chem. Rev., 110, 1, 3–24 (2010).
[2] Fortunato E, Barquinha P, Martins R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. Adv Mater 2012;24:2945–86.
[3] Hosseini M, Javad M, Nawrocki RA. A review of the progress of thin-film transistors and their technologies for flexible electronics. Micromachines 2021;12, 6:655.
[4] Geng D, Wang K, Li L, et al. Thin-film transistors for large-area electronics. Nat Electron 2023;6:963–72.
[5] Tixier-Mita A, Ihida Satoshi, et al. Review on thin-film transistor technology, its applications, and possible new applications to biological cells. Jpn J Appl Phys 2016;55 04EA08.
[6] Paterson Alexandra F, Anthopoulos Thomas D. Enabling thin-film transistor technologies and the device metrics that matter. Nat. Commun. 2018;9:5264.
[7] Yue Kuo. Thin Film Transistor Technology—Past, Present, and Future, Electrochem. Soc. Interface, 22 (2013) 55.
[8] Shim Gi Woong, Hong Woonggi, Cha Jun-Hwe, Park Jung Hwan, Lee Keon Jae, Choi Sung-Yool. TFT Channel Materials for Display Applications: From Amorphous Silicon to Transition Metal Dichalcogenides. Adv Mater 2020;32:1907166.
[9] Chen R, Zhou W, Deng S, Zhang M, Wong M, Kwok HS. Passivation of Poly-Si Thin Film Employing Si Self-Implantation and Its Application to TFTs. IEEE J Electron Devices Soc 2018;6:240–4.
[10] Wang C, Cheng R, Liao L, Duan X. High performance thin film electronics based on inorganic nanostructures and composites. Nano Today 2013;8(5):514–30.
[11] Sporea RdA, Wheeler LJ, Stolojan V, Ravi S, Silva P. Towards manufacturing high uniformity polysilicon circuits through TFT contact barrier engineering. Sci Rep 2018;8:17558.
[12] Tai Y-H, Tu C-C, Yuan Y-C, Chang Y-J, Wang P-C, Kuo Y-W. The Photosensitive Mechanism of Gap-Type Amorphous Silicon TFT. IEEE Trans Electron Devices 2021;68(12):6177–81.
[13] Saurabh Jaiswal, Rupam Goswami, Manish Goswami & Kavindra Kandpal, Impact of Interface Trap Distribution on the Performance of LTPS TFT, Silicon (2023).
[14] Singh Abhishek, Singh Manish Kumar. TCAD based study of parameters affecting the electrical performance of organic thin-film transistors. J Phys: Conf Ser 2020; 1706:012074.
[15] Cheng H-C, Wang F-S, Huang C-Y. Effects of NH3 plasma passivation on N-channel polycrystalline silicon thin-film transistors. IEEE Trans Electron Devices 1997;44 (1):64–8.
[16] Chern HN, Lee CL, Lei TF. The effects of fluorine passivation on polysilicon thin-film transistors. IEEE Trans Electron Devices 1994;41(5):698–702.
[17] Chen J, Sekiguchi T. Carrier Recombination Activity and Structural Properties of Small-Angle Grain Boundaries in Multicrystalline Silicon. Jpn J Appl Phys 2007;46: 6489.
[18] Chen B, Chen J, Sekiguchi T, Saito M, Kimoto K. Structural characterization and iron detection at Σ3 grain boundaries in multi crystalline silicon. J Appl Phys 2009; 105:113502.
[19] Matsuki N, Ishihara R, Baiano A, Beenakker K. Investigation of local electrical properties of coincidence-site-lattice boundaries in location-controlled silicon islands using scanning capacitance microscopy. Appl Phys Lett 2008;93:062102.
[20] Maji R, Contreras-Garcia J, Capron N, Degoli E. and Eleonora Luppi the role of Si vacancies in the segregation of O, C, and N at silicon grain boundaries: An ab initio study. J Chem Phys 2021;155:174704.
[21] Maji R, Luppi E, Capron N, Degoli E. Ab initio study of oxygen segregation in silicon grain boundaries: the role of strain and vacancies. Acta Mater 2021;204: 116477.
[22] Lu N-C-C, Gerzberg L, Chih-Yuan Lu, Meindl JD. A conduction model for semiconductor-grain-boundary-semiconductor barriers in polycrystalline-silicon films. IEEE Trans Electron Devices 1983;30(2):137–49.
[23] Chen Y, Zhang S, Li Z, et al. Carrier transport across grain boundaries in polycrystalline silicon thin film transistors. J Wuhan Univ Technol-Mat Sci Edit 2016;31:87–92.
[24] Kresse G, Hafner J. Ab initio molecular dynamics for liquid metals. Phys Rev B 1993;47:558.
[25] Kresse G, Furthmüller J. Efficient iterative schemes for ab initio total-energy calculations using a plane-wave basis set. Phys Rev B 1996;54:11169.
[26] Seidl A, Görling A, Vogl P, Majewski JA, Levy M. Generalized Kohn-Sham schemes and the band-gap problem. Phys Rev B 1996;53:3764.
[27] Muñoz Ramo D, Gavartin JL, Shluger AL, Bersuker G. Spectroscopic properties of oxygen vacancies in monoclinic HfO2 calculated with periodic and embedded cluster density functional theory. Phys Rev B 2007;75:205336.
[28] Perevalov TV, Islamov DR. Atomic and electronic structure of oxygen polyvacancies in ZrO2. Microelectron Eng 2017;178:275–8.
[29] Applied Materials Ginestra®. [Online]. Available: http://www.appliedmaterials.com/products/applied-mdlx-ginestra simulation-software.
[30] Vandelli L, Larcher L, Veksler D, Padovani A, Bersuker G, Matthews K. A charge-trapping model for the fast component of positive bias temperature instability (PBTI) in high-k gate-stacks. IEEE Trans Electron Dev 2014;61:2287–93.
[31] Padovani A, Pešić M, Nardi F, Milo V, Larcher L, et al. Reliability of Non-Volatile Memory Devices for Neuromorphic Applications: A Modelling Perspective (Invited). In: 2022 IEEE International Reliability Physics Symposium (IRPS); 2022. p. 1–10.
[32] M. Pešić, Bastien Beltrando, Andrea Padovani et al., Variability sources and reliability of 3D — FeFETs, 2021 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, , pp. 1-7 (2021).
[33] Pešić M, Fengler FPG, Larcher L, Padovani A, Schenk T, Grimley ED, et al. Physical Mechanisms behind the Field-Cycling Behaviour of HfO_2-Based Ferroelectric Capacitors. Adv Funct Mater 2016;26:4601–12.
[34] Larcher L, Nardi F, Milo V, et al. A Multiscale-Multiphysics simulation platform for technology virtualization: from process chamber modelling to device electrical prediction. In: 2023 IEEE Nanotechnology Materials and Devices Conference (NMDC); 2023. p. 805–9.
[35] M. Pešić, Bastien Beltrando, Tommaso Rollo, Cristian Zambelli et al., Insights into device and material origins and physical mechanisms behind cross temperature in 3D NAND, 2023 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 1-8 (2023).
[36] Ortiz-Conde A, García-Sánchez FJ, Muci J. Alberto Terán Barrios, Juin. J Liou, Ching-Sung Ho, Revisiting MOSFET threshold voltage extraction methods, Microelectronics Reliability 2013;53:1.
[37] Wong H-Y, Dolgos D, Smith L, Mickevicius RV. Modified Hurkx band-to-band-tunneling model for accurate and robust TCAD simulations. Microelectron Reliab 2020;104:113552.
[38] Lombos BA, Yee S, Pietrantonio M, Averous M. Grain boundaries introduced deep levels in polysilicon. J Phys Colloques 1982;43:C1-199–1-206.
[39] Hollemann C, Folchert N, Harvey SP, Stradins P, Young DL, Salles CL, et al. Changes in hydrogen concentration and defect state density at the poly-Si/SiOx/c-Si interface due to firing. Sol Energy Mater Sol Cells 2021;231:111297.
[40] Kang Di, Sio Hang Cheong, Stuckelberger Josua, Liu Rong, Yan Di, Zhang Xinyu, Macdonald Daniel. Optimum Hydrogen Injection in Phosphorus-Doped Polysilicon Passivating Contacts. ACS Appl Mater Interfaces 2021;13(46):55164–71.
[41] Kolbesen BO, Mühlbauer A. Carbon in silicon: Properties and impact on devices. Solid State Electron 1982;25:8.
[42] Lin Y, Yang Z, Liu Z, Zheng J, Feng M, et al. Dual-functional carbon-doped polysilicon films for passivating contact solar cells: regulating physical contacts while promoting photoelectrical properties. Energy Environ Sci 2021;14:6406–18.
[43] Potsidi MS, Kuganathan N, Christopoulos S-R-G, Sarlis NV, Chroneos A, Londos CA. Theoretical investigation of nitrogen-vacancy defects in silicon. AIP Adv 2022;12: 025112.
[44] Taguchi A, Kageshima H, Wada K. First-principles investigations of nitrogen-doping effects on defect aggregation processes in Czochralski Si. J Appl Phys 2005; 97:053514.
[45] Murphy JD, Al-Amin M, Bothe K, Olmo M, Voronkov VV, Falster RJ. The effect of oxide precipitates on minority carrier lifetime in *n*-type silicon. J Appl Phys 2015; 118:215706.