# Highlights

## Characterization of DC Performance and Low-Frequency Noise of an Array of nMOS Forksheets from 300 K to 4 K

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- Characterization of DC performance and low-frequency noise of 800 parallel Forksheet devices over a wide temperature range;
- 1/f noise at cryogenic temperatures does not follow the expected linear scaling with temperature;
- 1/f noise at cryogenic temperatures does not depend on the MOSFET architecture but rather on the physical structure of the semiconductor/dielectric interface.

# Characterization of DC Performance and Low-Frequency Noise of an Array of nMOS Forksheets from 300 K to 4 K

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ARTICLE INFO

*Keywords*:
Forksheet
cryogenic electronics
1/f noise

ABSTRACT

The DC and low-frequency noise performance of an array of 800 parallel Forksheet MOSFETs were investigated by performing measurements over a wide temperature range from 300 K to 4 K. The array structure allowed to measure a representative average performance of the devices and provided a large effective area for 1/f noise analysis. Results showed an improvement in the saturation drain current when going from room temperature to cryogenic temperatures, with the subthreshold swing saturating around 100 K and the threshold voltage shifting by approximately 150 mV, following similar trends observed in Silicon cryogenic electronics. Additionally, the study confirms that the noise at cryogenic temperatures does not follow the commonly assumed linear scaling with temperature. This deviation from the linear scaling has been associated with the presence of tail states at the interface in bulk and silicon-on-insulator (SOI) devices. These results suggest that the excess 1/f noise in this advanced device architecture is not related to the device architecture but rather to the microscopic material properties of semiconductor/dielectric interfaces.

## 1. Introduction

The ongoing trend of downscaling CMOS technology has led to the development of gate-all-around (GAA) devices [1; 2]. The Forksheet architecture is a particularly promising solution for further reducing the area footprint by bringing n-type and p-type devices closer to each other [3; 4]. Moreover, the recent interest in the development of quantum computing and high-performance computing has driven the need for more energy-efficient electronic devices that can operate at cryogenic temperatures [5; 6; 7]. Cryogenic electronics have been shown to offer a significant advantage over room temperature electronics due to their ability to operate at lower power and higher speeds [8].

In this study, we investigate the DC and low-frequency noise performance of an array of 800 parallel Forksheet devices from room temperature down to cryogenic temperatures. The array configuration provides the average performance of the Forksheet devices and a large effective area for 1/f noise analysis. Our results offer insights into the potential use of Forksheet at cryogenic temperatures (e.g., high-performance computing and quantum computing applications). Moreover, we compare the dependence of 1/f noise against temperature to previous measurements on 28nm bulk devices [9; 10]. The high levels of 1/f noise observed at low temperatures in this study confirm the non-ideal temperature dependence previously reported for commercial bulk CMOS and SOI MOSFETs [9; 10; 11], which are in contrast with the theoretical expectation that 1/f noise should scale linearly with $T$ [12].

## 2. Measurements setup

A single Forksheet (Fig. 1, [4]) of the array considered in this work has an effective channel width ($W$) and length ($L$) of 51.5 nm and 28 nm, respectively. Therefore, the array of 800 nMOS Forksheet in parallel corresponds to an effective $W = 41.2$ µm and $L = 0.028$ µm. To perform noise measurement across different temperatures we used a Lakeshore cryogenic probe station and a Keysight A-LFNA low-frequency noise analyzer applying $V_{DS}$=50 mV and different gate voltage overdrives ($V_{ov} = V_{GS} - V_T$, where $V_T$ is extrapolated from the linear $I_D - V_{GS}$ curve at the point of maximum transconductance [13]).

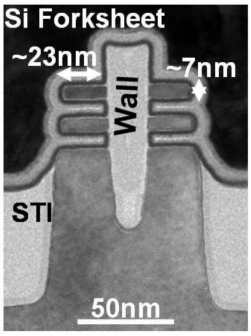


**Figure 1:** End-of-process TEM image perpendicular to the gate of the Forksheet [4].

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## 3. Measurements and discussion

Fig. 2 shows the drain current ($I_D$) versus gate-source voltage ($V_{GS}$) at low $V_{DS}$ over a temperature range from 300 K down to 4 K. It is observed that the drain current at high $V_{ov}$ and low $V_{DS}$ does not increase much at low temperature (see inset of Fig. 2). This deviates from the typical behavior observed in bulk MOSFETs and might be attributed to the suboptimal access resistance of the experimental devices and to a contact resistance that varies with temperature.

Fig. 3 shows the $I_D$ versus $V_{DS}$ for different $V_{ov}$ at 300 K, 100 K, and 4 K. We notice that the drain current improvement at low temperatures becomes visible when the $V_{DS}$ is above few tens of mV. This can be explained by the fact that parasitic series resistance has less impact when the $V_{DS}$ increases.

Fig. 4 summarizes the key temperature-dependent trends observed in the device. Fig. 4a shows that the shift in threshold voltage from 300 K to 4 K is approximately 150 mV. Fig. 4b illustrates how the $I_{ON}$ (defined as $I_D$ at $V_{ov}$= 0.3 V and $V_{DS}$ = 0.7 V) increases going toward low temperatures due to the increased mobility. Fig. 4c shows that the gate leakage current remains relatively constant over temperature. Finally, Fig. 4d plots the subthreshold swing (SS) versus temperature, revealing that it saturates below ≈100 K at a value of ≈ 25 mV/dec. The threshold voltage shift and the temperature at which the SS saturates are in line with published results for Silicon cryogenic electronics [9; 10; 8].

The input-referred 1/f noise ($S_{vg}$) of MOSFETs is commonly modeled as [12]

$$S_{vg} = \frac{qkTN_{BT}}{WLC_{ox}^2\alpha} \cdot \frac{1}{f} \cdot \left(1 + \Omega\frac{I_D}{g_m}\right)^2 , \qquad (1)$$

where $N_{BT}$ is an effective dielectric trap density per unit volume and unit energy, $\alpha$ is a tunneling coefficient routinely estimated through the WKB approximation, $C_{ox}$ is the effective gate dielectric capacitance per unit area, $q$ is the elementary charge, $T$ is the temperature, $f$ is the frequency and $\Omega$ is a parameter related to mobility fluctuations (MF).

To analyze the data, we implement a moving window methodology with a frequency range of 1/2 decade and evaluate the degree to which $S_{vg}$ follows the 1/f dependence by computing the $R^2$ parameter. The window exhibiting $R^2$ value closest to unity is employed to extract a $S_{vg} \cdot f$ value. This approach effectively removes from the analysis the noise components that are not associated with 1/f noise, such as Lorentzian contributions. Fig. 5 shows the product $S_{vg} \cdot f$ versus $I_D$ for $T$=300 K and $T$=4 K, demonstrating that 1/f noise follows the $(I_D/g_m)^2$ trend associated to MF only at high currents. The first two data points for each temperature correspond to $V_{ov}$ values of 0 V and 0.1 V, respectively. Those data points have a weak dependence on the drain current, therefore we can assume they fall in the carrier-number-fluctuations (CNF) regime ($\Omega I_D/g_m \ll 1$).

Fig. 6 plots $S_{vg}$ versus frequency at 4 K and 300 K for $V_{ov}$=0 V. As previously reported for CMOS, Ge bulk devices [9; 10] and for SOI devices [11], the noise at cryogenic temperature does not follow Eq. 1 and is even higher than

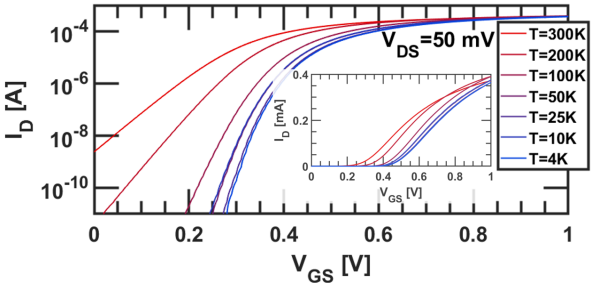


**Figure 2:** Plot of the drain current versus gate voltage for temperatures going from 300 K to 4 K and $V_{DS}$= 50 mV.

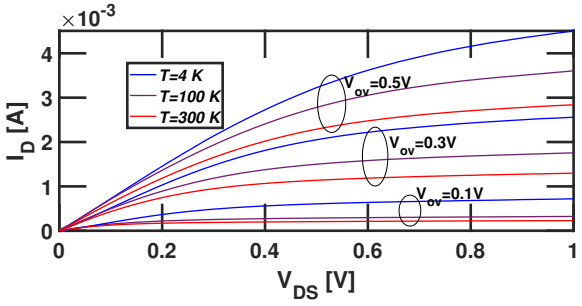


**Figure 3:** Plot of the drain current versus drain voltage at 300 K, 100 K, and 4 K.

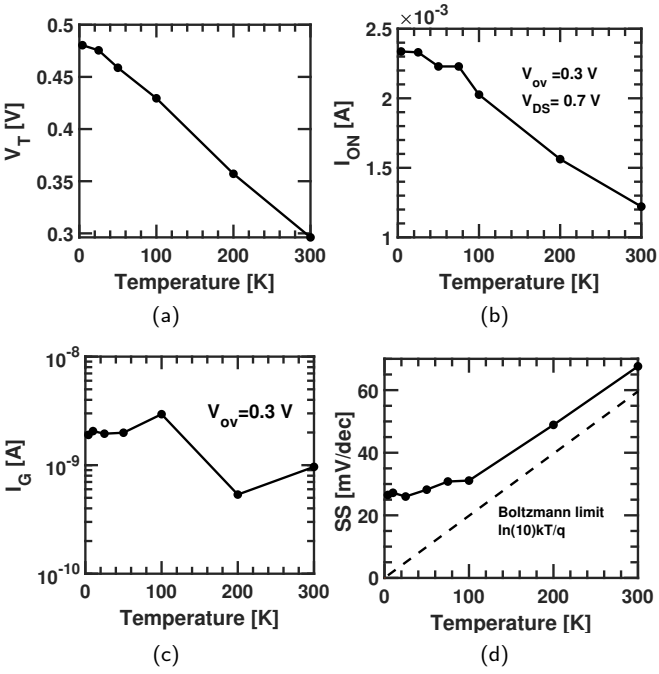


**Figure 4:** Temperature scaling of (a) $V_T$ (extracted with the maximum transconductance method), (b) $I_{ON}$ (defined as $I_D$ at $V_{ov}$=0.3 V and $V_{DS}$=0.7 V), (c) $I_G$ at $V_{ov}$=0.3 V and the (d) SS (extracted in the 10-100 nA drain current range).

at room temperature. By plotting $S_{vg} \cdot f/T$ versus $V_{ov}$ for different temperatures (Fig.7), we can see that the noise scales approximately as Eq. 1 only down to 100 K (the curves almost fall on top of each other above 100K). This is further highlighted when $S_{vg} \cdot f/T$ is plotted against $T$ for fixed gate voltage overdrives, see Fig. 8: the $S_{vg}$ does not follow the $T$ scaling below 100 K. It is noteworthy that SS saturates around 100 K (see again Fig.4d), suggesting a strong correlation between the two phenomena.

Previous studies in bulk and SOI MOSFETs at cryogenic

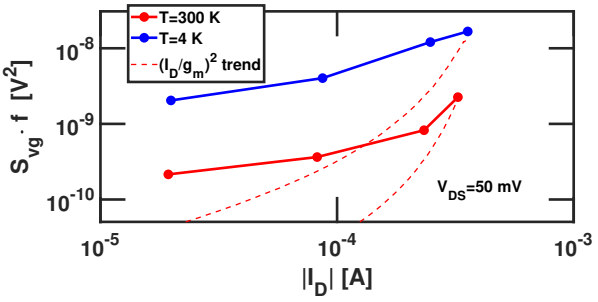


**Figure 5:** Plot of $S_{vg} \cdot f$ (solid) and normalized $(I_D/g_m)^2$ (dashed) as a function of $I_D$ at $T$ = 300 K and $T$ = 4 K. CNF seems to dominate at lower currents (see Eq. 1).

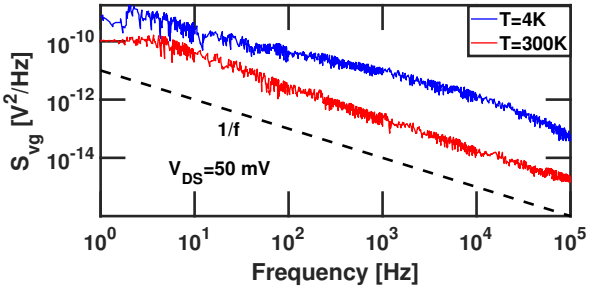


**Figure 6:** $S_{vg}$ measured at 300 K and 4 K for $V_{ov}$ = 0 V and $V_{DS}$ = 50 mV. The noise amplitude at 4 K is higher than the one at 300 K contrary to the prediction of Eq. 1. The $S_{vg}$ at 4 K goes as 1/f up to 100 Hz (frequency range in which the data is fitted and analyzed), while above 100 Hz some Lorentzian components show up.

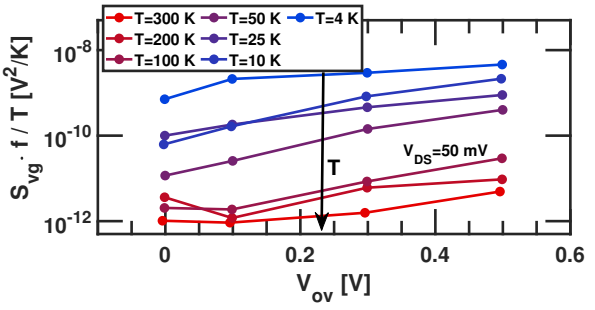


**Figure 7:** Plot of $S_vg \cdot f/T$ as a function of $V_{ov}$ at different temperatures for $V_{DS}$= 50 mV.

temperatures [9; 10; 11] attributed the high values of 1/f

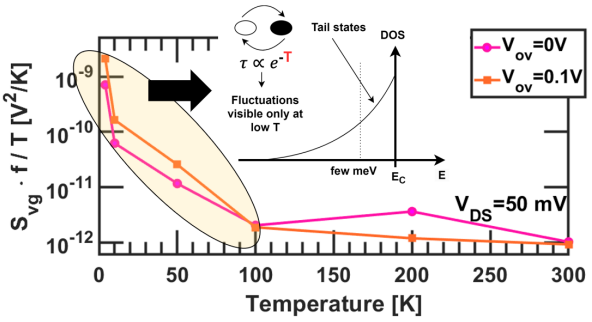


**Figure 8:** Plot of $S_{vg} \cdot f/T$ versus temperature at $V_{DS}$= 50 mV and two different $V_{ov}$. $S_{vg}$ scales according to Eq. 1 down to approximately 100 K and then it increases abruptly due to the fluctuation of band tail states.

noise to the fluctuations of shallow localized states at the channel/dielectric interface, commonly referred to as "band tail states". Notably, these fluctuations and the related high 1/f noise were observed only at cryogenic temperatures, emphasizing the temperature-dependent nature of the phenomenon.

It has been previously shown that the presence of a dielectric wall between Forksheets (see Fig. 1) does not have an impact on the 1/f noise at room temperature [4]. To see whether the dielectric wall plays a role in the 1/f noise at cryogenic temperatures, we compare the temperature scaling of the noise by plotting the $S_{vg} \cdot f$ normalized by the temperature and the area (to eliminate the area dependence of Eq. 1) for commercial bulk MOSFETs and the prototype Forksheet MOSFETs in Fig. 9. *We see that the behavior in temperature of the 1/f noise of Forksheets closely matches the one of bulk devices*. Therefore, these new experimental results provide further confirmation of these previous studies, emphasizing that the high 1/f noise at cryogenic temperatures is not specific to the architecture of the MOS device, but rather stems from fundamental physical characteristics such as the presence of a semiconductor/dielectric interface giving rise to band tail states in the channel.

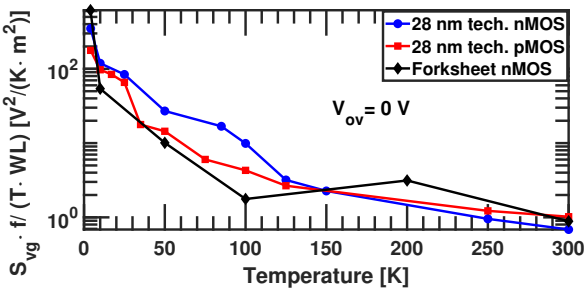


**Figure 9:** Plot of $S_{vg} \cdot f/(T \cdot WL)$ versus temperature at $V_{DS}$= 50 mV and $V_{ov}$=0 V for 28 nm technology bulk MOSFETs [9; 10] and the Forksheet array measured in this study.

## 4. Conclusions

We investigated the DC performance and low-frequency noise of an array of n-type Forksheet over a temperature range going from 300 K to 4 K. We measured an improvement in the on-current for high $V_{DS}$ when going from 300 K to 4 K, as expected due to mobility enhancement at low temperatures. The threshold voltage increases approximately by 150 mV, while the SS scaling saturates below 100 K, following the trends reported from other Silicon cryogenic electronic devices. 1/f noise measurements show that CNF dominates the noise in the explored $V_{ov}$ range. The noise at cryogenic temperatures does not follow the linear temperature scaling predicted by the commonly used 1/f models. This behavior has been previously observed in bulk and SOI devices as well and is associated with the presence of tail states at the interface. The results presented here confirm that the excess 1/f noise at cryogenic $T$ is not related to the device architecture, but rather to the material properties of semiconductor/dielectric interfaces.

## Acknowledgments

This work is funded in part by imec's Industrial Affiliation Program on CMOS technology, Quantum Computing, and Cryoelectronics.

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