Negative Capacitors and Applications

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List of Abbreviations

6T-SRAM Six Transistors SRAM 25, 26

AFE Anti-Ferroelectric Layer 15

AOI AND-OR-INVERT 25

CAM Content Addressable Access Memory 28

CMC Capacitance Matching Condition 13, 14, 15

CMOS Complementary Metal-Oxide-Semiconductor 23, 25, 27, 30, 31, 32

DGFET Dual(or Double)-Gate FET 19

DRAM Dynamic Random Access Memory 26, 27

FE Ferroelectric Layer 12, 13, 15, 22, 26, 27, 28, 30, 32, 33, 34, 52, 53, 56

Fe-GNWFET Ferroelectric Germanium NanoWire FET 33

FeFET Ferroelectric MOSFET 15, 16, 17, 22, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 53, 54, 55, 56, 57

FeRAM FE-Capacitor RAM 27

FET Field Effect Transistor 9, 30, 47, 53, 54

FinFET Fin(or Tri-Gate) FET 16, 19

GAAFET Gate-All-Around FET 19

HAD Hot Atom Damage 16, 17

HRS High Resistive State 27, 34

HZO Zirconium-doped Hafnium Oxide 33, 34

IF Integrate and Fire 33, 34

IFET Impact Ionization FET 10

IMT Insulator-To-Metal Transition 20, 21, 24, 25, 26, 29, 31, 34

JLFET Junctionless FET 19

KVL Kirchhoff Voltage Law 13, 48

Landau FET Landau FET 10, 13, 15, 16, 17

LIF Leaky Integrate and Fire 33, 34

LKE Landau-Khalatnikov Equation 13, 19, 49

LRS Low Resistive State 27, 34

MD Multiple Domain 32, 56

MD-FeFET Multi Domain FeFET 28, 32, 33, 56

MFIS Metal-Ferroelectric-Insulator-Semiconductor 12, 27, 28, 47

MFMIS Metal-Ferroelectric-Metal-Insulator-Semiconductor 12, 27, 47

MIT Metal-To-Insulator Transition 20, 21, 24, 25, 26, 29, 31

MOSFET Metal-Oxide-Semicondcutor FET 11, 12, 13, 14, 16, 17, 19, 20, 23, 24, 25, 26, 27, 28, 32, 34, 35, 48, 51

MottFET Mott FET 9, 10, 21, 47

MRAM Magnetic Random Access Memory 28, 35

MTJ Magnetic Tunnel Junction Memory 28, 29, 54

NAND NOT-AND 24

NBTI Negative Bias Temperature Instability 16, 17

NC Negative Capacitance 11, 12, 13, 14, 15, 16, 18, 19, 22, 23

NC-TFET Negative Capacitance Tunnel FET 10

NCFET Negative Capacitance FET 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 23, 24, 25, 26, 29, 30, 31, 34, 35, 47, 48, 49, 50, 52, 53, 55

NDIBL Negative Drain-Induced Barrier Lowering 19

NDR Negative Differential Resistance 19, 23, 25, 30, 31

NEMFET Nano Electro-Mechanical FET 10

NEMS Nano-Electro-Mechanical System 15

NVM Non-Volatile Memory 26, 27, 28, 29, 34, 35, 54

PC-TFET Phase Change Tunnel FET 10

PhaseFET Phase FET 8, 9, 10, 11, 19, 20, 21, 22, 24, 25, 26, 28, 29, 30, 31, 32, 34, 35, 47, 51, 52, 53, 54, 55, 57

PT Pass Transistor 31, 55

PTM Phase Transition Material 10, 11, 20, 21, 24, 25, 26, 28, 29, 30, 31, 34, 51, 53, 55, 57

PZT Lead Zirconium Titanate 33, 51

QL Quasi Leaky 34

QLIF Quasi-Leaky-Integration-Fire 34

R-FeFET Reconfigurable FeFET 28

SGFET Suspended-Gate FET 10, 16

SNM Static Noise Margin 53

SNN Spiking Neural Network 33, 34

SRAM Static Random Access Memory 25, 26, 35, 53

STDP Spike Time-Dependent Plasticity 33, 56

TDDB Time Dependent Dielectric Breakdown 16, 17

TFET Tunnel FET 9, 10

TG Transmission Gate 31, 55

TS Threshold Selector 20

VTC Voltage Transfer Characteristic 22, 23, 24, 31, 52

List of Symbols

k_B Boltzmann Constant (1.3807×10^{-23} J/K)

T Semiconductor Temperature (300 K)

SS Sub-threshold Swing (mV/dec)

I_D Drain Current (A/μm)

V_{GS} Gate-to-Source Voltage (V)

ψ_s Surface Potential (V)

m Body Factor

n Transport Factor

q Elementary Charge (1.602×10^{-19} C)

U Gibb's Free Energy Density (J.cm^{-3})

α Landau 1$^{\text{st}}$-Order Parameter (m.F^{-1})

β Landau 3$^{\text{rd}}$-Order Parameter (m^5.F^{-1}C^{-2})

γ Landau 5$^{\text{th}}$-Order Parameter (m^9.F^{-1}C^{-4})

E Electric Field (V.cm^{-1})

P Polarization Charge Density (C.cm^{-2})

T_c Critical Temperature (K)

C_{NC} Negative Capacitance (F.cm^{-2})

C_{ox} Gate Oxide Capacitance (F.cm^{-2})

C_s Semiconductor Capacitance (F.cm^{-2})

V_T Threshold Voltage (V)

I_{ON} On-State Current (A/μm)

I_{OFF} Off-State Current (A/μm)

ρ Landau Damping Parameter (Ω.cm)

V_{FE} Ferroelectric Potential (V)

V_{ox} Gate Oxide Potential (V)

V_{FB} Flat-Band Potential (V)

Q_s Semiconductor Charge Density (C.cm^{-2})

$V_{GS,MOS}$ Effective Gate Voltage (V)

A_V Voltage Gain

C_{FE} Ferroelectric Capacitance (F.cm^{-2})

C_{MOS} MOSFET Capacitance (F.cm^{-2})

T_{FE} Ferroelectric Layer Thickness (nm)

V_{DS} Drain-to-Source Voltage (V)

V_{DD} Supply Voltage (V)

E_G Energy Bandgap (eV)

κ Thermal Conductivity (W.K$^{-1}\mu$m^{-1})

R_{LRS} Resistance in the Low-Resistive-State ($\Omega.\mu$m)

R_{HRS} Resistance in the High-Resistive-State ($\Omega.\mu$m)

T_x Empirical Temperature Parameter (K)

C_{th} Thermal Capacitance (J.K$^{-1}\mu$m^{-1})

R_{th} Thermal Resistance (Kμm.W^{-1})

T_0 Ambient Temperature (K)

V_{PTM} PTM Potential (V)

I_{PTM} PTM Current Density (A/μm)

a Mott Insulator Parameter

b Mott Insulator Parameter (K^{-1})

κ_0 Insulator Phase Thermal Conductivity (W.K$^{-1}\mu$m^{-1})

κ_1 Metal Phase Thermal Conductivity (W.K$^{-1}\mu$m^{-1})

R_f Oscillator Feedback Resistance

$\bar{P}$ Average Macroscopic Polarization

V_{PULSE} Gate Voltage Pulse

G_{DS} Drain/Source Conductance

Contents

Chapter 1

Negative Capacitors and Applications

Abstract

The long-standing tug-of-war between off-state leakage power consumption and switching speed has posed severe challenges to the scaling of semiconductor devices. Deeply scaled short-channel transistors are faster, but consume more off-state power. This power vs speed trade-off stems from the fundamental physical limit related to the thermionic emission that governs the switching of field-effect transistors. There is a broad consensus in the semiconductor industry that future progress is impossible unless the next generation transistors and circuits overcome the so-called "Boltzmann Limit" associated with thermionic-emission over a barrier and offer a steeper on-off switching to enable a more aggressive voltage scaling.

In this chapter, we explain the need for and suggest an intuitive classification of the emerging transistor technologies. We use two illustrative examples of next-generation transistors (i.e. Negative Capacitance FET (NCFET) and Phase FET (PhaseFET)) to explain the relative merits of gate-controlled vs channel-controlled steep-slope switching. We explain the basic principle of device operation, summarize the experimental results reported in the literature, and highlight the speed and reliability challenges to be resolved before the devices are integrated into practical systems. In addition, the chapter includes a careful analysis of circuits based on these emerging transistor technologies with applications towards Boolean logic, memories and non-Boolean computing. The analysis suggests relative merits of various circuit designs and application-specific opportunities for significant power-performance improvement.

1.1 Introduction

Since the early 1970s, the progress in the semiconductor industry has been dictated by the scaling of (field-effect) transistors that allow each generation of devices to have significant performance improvements over their predecessors. The tremendous growth of the computing power was driven by Moore's law from the the cost/economical point of view, and by Dennard's scaling from the performance/physical point of view. A decisive change of course began to occur at the beginning of the 21^{st} century, when transistor speed began to saturate due to self-heating and the limits of power-dissipation ($\sim 100\,\mathrm{W/cm^2}$) in an integrated circuit.

This problem was initially solved (or better, circumvented) (a) from the system point of view by switching to multi-core architectures, and (b) from the device perspective by devising new scaling rules. These rules formed the so-called "equivalent scaling" roadmap, which relied on the introduction of new insulating materials (to limit the leakage power consumption) and of complex three-dimensional geometries (to improve electrostatic control and limit the short-channel effects). Although scaling was effectively preserved and performance could still improve, the issues brought up by new geometries in terms of self-heating (and thus temperature rise) threatened to stop transistor scaling once more. This aspect motivated researchers to focus on new device concepts with the ultimate goal of decreasing power dissipation to control the temperature rise in transistors. The equivalent scaling rules, which are expected to be effective until around 2025 [1], will need to be replaced by next-generation transistors and computing architecture to sustain the semiconductor industry.

1.1.1 A Simple Classification of the Next Generation Transistors

It has been clear since the 1990s that next generation transistors would have to circumvent the fundamental limits of classical Boltzmann Field Effect Transistors (FETs). The initial focus on Tunnel FET (TFET) and resonant-tunneling transistors has now broadened to include NCFET, PhaseFET, Mott FET (MottFET), MEMS-relay, etc. These beyond-Boltzmann FETs rely on new physics principles and device designs to overcome the fundamental limit of transistor switching. This limit is related to the energy required by electrons to overcome a potential barrier, expressed in multiples of k_BT (k_B is the Boltzmann constant, and T is the temperature), that in turn forces the minimum voltage swing required to decrease the transistor current by one order of magnitude to the value of $60\,\mathrm{mV/dec}$ at room temperature. This minimum voltage swing is

called sub-threshold swing (SS), and is expressed as follows:

$$\begin{aligned} SS &= \left(\frac{\partial \log I_D}{\partial V_{GS}}\right)^{-1} = \left(\frac{\partial \psi_s}{\partial V_{GS}} \times \frac{\partial \log I_D}{\partial \psi_s}\right)^{-1} \\ &= \left(\frac{\partial \psi_s}{\partial V_{GS}}\right)^{-1} \times \left(\frac{2.3 k_B T}{q}\right) \\ &= m \times n \approx m \times 60\,\mathrm{mV/dec} \end{aligned} \tag{1.1}$$

where I_D is the drain current, V_{GS} is the gate-to-source bias voltage, ψ_s is the surface potential, m is the body factor (described more in detail later), n is the transport factor, and q is the elementary charge. The SS imposes a lower limit on the minimum allowable operating voltage for a target on- to off-current ratio of $V_{min} \approx SS \times \log(I_{ON}/I_{OFF})$. It is then clear than to further reduce power dissipation, SS needs to be decreased. From Eq. (1.1), it is possible to devise different strategies to reduce SS, through either m or n. The classes of transistors belonging to the family of beyond-Boltzmann devices – originating from the attempts of reducing m and/or n – can be classified as follows:

- **Non-thermionic FETs ($m = 1$, $n < 60$)** exploit physical mechanisms different from the thermionic emission to control the channel conduction. One can either reduce the electron temperature below the lattice temperature to suppress off-state conduction, or use positive electro-thermal feedback to enhance on-state conduction. This category includes: the TFETs, [2, 3]) Impact Ionization FETs (IFETs) [4], PhaseFETs [5] and MottFETs [6].
- **Landau FETs** ($m < 1$, $n = 60$) exploit the "negative capacitance" effect to lower the body-factor [7, 8]. This category includes: the NCFETs and the Nano Electro-Mechanical FET (NEMFET) [9], Suspended-Gate FET (SGFET), etc.
- **Super FETs ($m < 1$, $n < 60$)** combine the benefits of Non-Thermionic FET and Landau FETs to obtain minimum subthreshold swing, such as the Negative Capacitance Tunnel FETs (NC-TFETs) [10] or Phase Change Tunnel FETs (PC-TFETs) (with the Phase Transition Material (PTM) layer inserted in the gate stack, see [11]).

Fig. 1.1 summarizes the different class of transistors in the space defined by the possible combinations of m and n, including the classical Boltzmann FETs, characterized by $m > 1$ and $n = 60$. In this chapter, we will focus on two illustrative examples of next generation switches, namely, the NCFETs and PhaseFETs. In the following, we will explain the device physics, reliability limits, as well as the circuit implications of these transistors.

1.1.2 Phase Transition and Landau Theory

We now briefly discuss some elements of phase transition and Landau theory which are at the foundation of both NCFETs and PhaseFETs operation. Phase

transitions are changes occurring in a thermodynamic system when a certain order parameter of the system itself varies suddenly in response to an external stimulus. Examples of materials that undergo phase transitions are $BaTiO_3$, that experience dielectric to ferroelectric transition [12], and VO_2, that instead experiences insulator-to-metal transition [5]. Regardless of the physical stimulus that triggers the phase transition, the order of the system is disrupted from its previous state, which can be restored if the reverse process is stimulated. Exploiting this interesting physical behavior is at the core of the operation of the devices discussed in this chapter.

In ferroelectric materials, the stored energy as a consequence of phase transition can trigger the so-called negative capacitance behavior [7]. This behavior occurs only if the instability connected with the Negative Capacitance (NC) effect can be stabilized (and this is indeed achieved by device design, as discussed in Section 1.2). The free energy of a ferroelectric U (in the case of uniform, mono-dimensional polarization) can be written as follows:

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - E \cdot P \tag{1.2}$$

where α, β, γ are material parameters, E is the external applied electric field and P is the polarization of the ferroelectric. For a negative capacitor, α is always negative [7]. Although the Landau theory allows for a phenomenological interpretation of ferroelectric behavior (based on a mean-field approach [13]), it can be shown that the Gibb's free energy as written in Eq. (1.2) can be derived also starting from microscopic physics arguments [14]. In practice, this allows to connect the Landau parameters (α, β, γ) to physical properties of the ferroelectric (such as dielectric constant, temperature dependence, and so on). In Section 1.2 we will discuss in which way from Eq. (1.2) the NC behavior can be deduced and exploited in realistic cases.

For PTMs employed in PhaseFETs, such as vanadium dioxide, VO_2, when the device temperature reaches a critical temperature, T_c, an abrupt transition occurs causing the material to switch between a metal and an insulator, and vice versa. Temperature in a PhaseFET varies due to self-heating determined by the current flow as controlled by the transistor. The phase transition of VO_2 leads to the sub-thermionic switching of the transistor, as we will discuss more in detail in Section 1.3.

1.2 Device Physics of NCFETs

In this chapter we will describe the fundamental aspects of the physics behind NCFETs operation. The discussion is built upon Landau Theory introduced in Section 1.1.2 that allows deriving the electrostatics of the system composed by a conventional Metal-Oxide-Semicondcutor FET (MOSFET) and the NC layer (i.e., a ferroelectric layer).

1.2.1 A Phenomenological Theory of a NCFET

Fig. 1.2 shows the two typical NCFET configurations: Metal-Ferroelectric-Insulator-Semiconductor (MFIS), Fig. 1.2(a), and Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS), Fig. 1.2(b). Regardless of the specific configuration, an appropriately designed ferroelectric layer can behave like a negative capacitor, storing energy and thus amplifying the applied gate bias [1, 7]: this phenomenon is the fundamental mechanism for the steep SS in NCFETs. The oxide layer between the ferroelectric and the semiconductor (either with the metal in between or not), is required in order to stabilize the ferroelectric in the NC region and to obtain sub-60 mV/dec SS.

Body-factor Reduction with Negative Capacitors

Before moving into the details of NCFET device physics, it is instructive to understand how the body-factor m can be reduced through the negative capacitance effect. To illustrate the concept, we will consider a simple network of three capacitors in series, as shown in Fig. 1.3(a). This network simplifies the gate stack of an NCFETs composed by the NC layer, C_{NC}, the gate oxide layer C_{ox} (SiO_2, normally), and the semiconductor layer, C_s. For the sake of argument, we will consider C_s to be constant. Thus, the relation between ψ_s and V_{GS}, can be written as (see Fig. 1.3(a)):

$$m \equiv \frac{\partial V_{GS}}{\partial \psi_s} = 1 + \frac{C_s}{C} \tag{1.3}$$

where $C = (C_{NC} + C_{ox})/(C_{NC}C_{ox})$. Since $C_{NC} < 0$, then $m < 1$ and $SS < 60\,\text{mV/dec}$. Reducing m and SS leads to lower power consumption, as the off-state current $I_{OFF} = I_D(V_G = 0)$ is reduced. This can be simply understood from the relationship between V_{GS} and sub-threshold current:

$$I_{OFF} = I_0 \times e^{\frac{q\psi_s}{kT}} \sim I_0 \times e^{\frac{-qV_T}{mkT}} \tag{1.4}$$

where V_T is the threshold voltage of the transistor and I_0 a proportionality factor (that depends on device properties). Fig. 1.3(b) shows graphically the reduction in I_{OFF} obtained with NCFETs compared to conventional MOSFETs.

Capacitance Matching Condition

Having clarified the role of NC in body-factor reduction, we can move on to discuss more in detail the physics of NCFETs. The discussion will focus on how to obtain effective reduction in SS by careful matching of the non-linear C_s and C_{NC}. The NCFET analysis is presented considering a bulk MOSFET as the underlying transistor (however, it can also be adapted to encompass different kinds of transistors). The capacitance network to discuss the body-factor reduction for a realistic NCFET is shown in Fig. 1.4. C_{FE} is the Ferroelectric Layer (FE) layer and C_{MOS} is the MOSFET gate stack capacitance, composed by the series of the gate oxide layer, C_{ox}, and the semiconductor capacitance, C_s.

Compared to a standard MOSFET, an NCFET has an extra capacitance C_{FE} that adds an additional voltage drop, V_{FE}, to that of the gate oxide, V_{ox}. If the FE is stabilized in the NC region, then V_{FE} can become negative, thus providing voltage amplification. The constraint to guarantee the stable operation in the NC region is defined as the Capacitance Matching Condition (CMC). We will derive the CMC starting with the ψ_s vs V_{GS} relation obtained by invoking the Kirchhoff Voltage Law (KVL) at the gate-to-source loop. This approach is equivalent to the minimization of the Gibb's free energy of the system [15], thus is physically sound within the limits of the validity of the theory. The KVL can be written as follows [16, 17]:

$$V_{GS} - V_{FB} = V_{FE} + V_{ox} + \psi_s \tag{1.5}$$

where V_{FB} is the flat-band voltage. V_{FE} is obtained from the phenomenological description of the FE behavior as given by the Landau-Khalatnikov Equation (LKE) [7]. The LKE in the case of one-dimensional polarization component reads as follows:

$$\rho \frac{\mathrm{d}P}{\mathrm{d}t} + \frac{\partial U}{\partial P} = 0 \tag{1.6}$$

where U is the Gibb's free energy of the ferroelectric, see Eq. (1.2), and ρ is the ferroelectric damping parameter (inversely related to the switching speed of the system). From Eqs. (1.2) and (1.6), it is possible to write an expression for the electric field applied to the ferroelectric as a function of the polarization, as follows:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{\mathrm{d}P}{\mathrm{d}t} \tag{1.7}$$

By equating the polarization of the ferroelectric, P, to the semiconductor charge Q_s (i.e., the second term in $Q = P + \varepsilon E$ is considered to be negligible for simplicity, as the electric field in the ferroelectric is small [16]) and by focusing on the steady-state response (i.e. $\rho \mathrm{d}P/\mathrm{d}t = 0$ in Eq. (1.6)), then V_{FE} can be written as:

$$V_{FE} = T_{FE}(2\alpha Q_s + 4\beta Q_s^3 + 6\gamma Q_s^5). \tag{1.8}$$

where T_{FE} is the ferroelectric layer thickness. From this equation, one can appreciate the NC region that gives rise to body-factor reduction, as shown in Fig. 1.5. The characteristic "S-shaped" curve between the two stable polarization branches (i.e., $-P$ and $+P$) represents the unstable NC region, where $\left(\partial U^2/\partial^2 P\right)^{-1} < 0$. This point will be discussed further in Section 1.2.2 for the whole class of NC systems, called Landau FETs (Landau FETs). Thus, in the NC region V_{FE} can assume negative values, so that the effective gate voltage seen by the MOSFET, $V_{GS,MOS}$, becomes larger than the applied bias. That is:

$$V_{FE} < 0 \Rightarrow V_{GS,MOS} = V_{GS} - V_{FE} > V_{GS} \tag{1.9}$$

We can define the internal voltage gain, A_V, as follows:

$$A_V \equiv \frac{\mathrm{d}V_{GS,MOS}}{\mathrm{d}V_{GS}}. \tag{1.10}$$

When the transistor is stabilized in the NC region (i.e. $A_V > 1$), the internal voltage amplification allows to achieve steep-slope operation. The capacitor divider network in Fig. 1.4 allows then to derive a simple equation for A_V through the expressions of C_{FE} and C_s. The former, C_{FE}, is derived by taking the inverse of $\partial V_{FE}/\partial Q_s$ [16]:

$$C_{FE} = \frac{1}{T_{FE}(2\alpha + 12\beta Q_s^2 + 30\gamma Q_s^4)} \tag{1.11}$$

Thus, simply:

$$A_V = \frac{C_{FE}}{C_{FE} + C_{MOS}} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \tag{1.12}$$

Clearly, A_V is maximized if $|C_{FE}| \to C_{MOS}$: this is the CMC. In the following, we will discuss the design constraints necessary for CMC.

Design Constraints for Gain Maximization

To maximize A_V and reduce SS, it is crucial to design C_{FE} to match C_{MOS}. Since both C_{FE} and C_{MOS} are non-linear and bias-dependent, CMC can only be obtained for a limited V_{GS}. Indeed, Fig. 1.6 shows that the ferroelectric thickness T_{FE} dictates the $I_D - V_{GS}$ characteristics (Fig. 1.6(a)), the internal voltage amplification $A_V - V_{GS}$ (Fig. 1.6(b)), and the corresponding $SS - V_{GS}$ (Fig. 1.6(c)) ($t_{FE} = 0\,\text{nm}$ in Fig. 1.6 corresponds to a stand-alone MOSFET). Fig. 1.6(c) confirms that SS is reduced significantly only over a limited range of V_{GS} because of the non-linear, voltage-dependent C_{FE} and C_s. In general, transistors based on other semiconductor technologies (such as Ge, 2D Metal Transition Dichalcogenides, Compound Semiconductors, and so on) will have different SS values and for different V_{GS} range [18]; thus each technology must be optimized based on their specific geometry and operating conditions. Section 1.2.4 summarizes the experimental results of NCFETs for different technologies, showing a relatively large scatter between SS values due to different CMC conditions.

Subthreshold Swing and Hysteresis Trade-Off

From Fig. 1.6, we notice that although SS is reduced with increasing T_{FE}, at some critical value, T_{FE}^*, hysteresis in the $I_D - V_{GS}$ characteristics appears. Thus, optimum design of NCFET must ensure that the SS reduction does not lead to excessive hysteresis. This undesirable feature arises when the total gate capacitance becomes negative, i.e., when $|C_{FE}|$ becomes smaller than C_{MOS}. During hysteretic operation, the ferroelectric starts switching between two stable states (indicated by the solid lines in Fig. 1.5) and skips the NC region. In this scenario, the SS might still be lower than $60\,\text{mV/dec}$ but not due to the NC effect but rather to abrupt polarization switching [18]. It is important to avoid hysteresis in digital and, more especially, in analog applications that would otherwise lead to larger power consumption and circuit overheads to manage

the non-symmetrical turn-on and turn-off characteristics. To summarize, maximization of A_V may lead to undesirable hysteresis; therefore, the design of a "well-tempered" NCFET must balance the two requirements of hysteresis-free and steep-slope operation.

Incidentally, we observe that a whole class of transistors called Ferroelectric MOSFETs (FeFETs) using the same device structure of NCFETs [18] relies on hysteresis in the $I_D - V_{GS}$ characteristics to enable a variety of applications. These include low-power and ultrafast non-volatile memories, computing elements embedded with memory capability (suitable for the Logic-In-Memory paradigm), and cross-bar arrays for artificial neural networks [19]. Some of the possible circuit applications of FeFETs (as well as NCFETs) will be discussed more in detail in Sections 1.4 and 1.5.

1.2.2 Tailoring the Negative Capacitance by Engineering the Energy Landscape

We move on with the discussion by generalizing the concept of NC operation to a wider range of devices. As discussed in the introduction, NCFETs belong to the family of devices called Landau FETs (or Landau Switches) [8]. This class of devices achieves the $SS < 60\,\mathrm{mV/dec}$ metric by reducing the body factor m below 1, see Eq. (1.1). The general behavior of Landau FETs can be understood in terms of their energy landscape, that determines the NC region as discussed in Section 1.2.1. The energy landscape for a NC system is expressed in Eq. (1.2), which is valid for any system that can switch between two stable states, such as a ferroelectric layer. Basically, an NCFET is a system that combines a positive capacitor with a negative capacitor so that the total energy U_{TOT} can be expressed by:

$$U_{TOT} = \left(\alpha + \frac{1}{2\varepsilon}\right) P^2 + \beta P^4 + \gamma P^6 - E \cdot P. \tag{1.13}$$

The positive capacitor adds up the $1/2\varepsilon \times P^2$ term to the Gibb's free energy of the NC, making it possible to stabilize the NC region. The energy landscape for a positive and negative capacitor are depicted in Fig. 1.8(a) and (b), respectively. Unfortunately, the Landau coefficients are material-specific and the higher-order terms, β and γ, make the body-factor m, voltage gain A_V, and SS improvement bias-dependent - making it more challenging, in turn, to reach the CMC condition with hysteresis-free operation for the whole V_{GS} range. In general, one could use various series combination of NC layers in a Landau FET (such as, FE, Anti-Ferroelectric Layer (AFE), Nano-Electro-Mechanical System (NEMS), each with their specific energy landscape) to tailor/flatten the total energy-landscape so that CMC is reached for the entire bias range of interest [20, 21].

Prospects of Hysteresis-Free Abrupt Switching

In principle, it is possible to design Landau FET exhibiting ideal $SS \approx 0\,\mathrm{mV/dec}$ with no hysteresis [8]. This can be achieved by properly compensating for the energy barrier present in between the two-wells of the energy landscape, see Fig. 1.8(b). The extra energy component to compensate for the switching barrier can be provided by a non-linear capacitor, as for example the depletion layer of a MOSFET. In this way, the intrinsic two-well energy landscape of a NC layer (be either an air-gap in a SGFET or a ferroelectric in a NCFET) can be effectively flattened out, removing the switching barrier and eliminating hysteresis. In more realistic cases, however, where neither the semiconductor capacitance nor the negative capacitance are constant throughout the bias range, then the SS cannot be arbitrarily reduced [20]. In fact, it can be proved that depending on the particular Landau FET, there exists a minimum SS that is dictated by stability constraints to achieve hysteresis-free operation [20]. We conclude by observing that the theory developed in Section 1.2.1 can be extended to any kind of Landau FET to achieve optimum design in terms of SS and hysteresis.

1.2.3 Reliability Physics of NCFETs

Having discussed the general theory for NCFETs and Landau FETs, we move on with the discussion of the reliability issues of NCFETs. The reliability issues have not yet been systematically quantified [18], thus we will summarize the current understanding regarding the reliability issues of NCFETs in comparison with stand-alone MOSFETs.

1. Negative Bias Temperature Instability (NBTI). Negative bias temperature instability is a major reliability concern for traditional MOSFET [22, 23]. It appears that NCFET suppresses NBTI as a consequence of two counter-balancing effects. First, the threshold voltage shift due to interface traps changes the internal potential of the transistor, thereby modifying the voltage amplification. Second, the charge balance requirement changes the range over which voltage-amplification is achieved. Combined with parasitic gate-to-drain capacitance, these two effects are predicted to suppress NBTI degradation in modern Fin(or Tri-Gate) FETs (FinFETs) [24].

2. Time Dependent Dielectric Breakdown (TDDB). The amplification of internal potential induces higher fields in the oxide layer between the ferroelectric and semiconductor, thus the TDDB reliability may be compromised if one wishes to increase drive current through voltage-amplification [25]. Instead, one should design the NCFET and scale the voltage appropriately so that the interface-field (and therefore I_{ON}) remains unchanged and TDDB robustness is preserved.

3. Hot Atom Damage (HAD). First analyzed for ferroelectric switching devices (such as FeFET), HAD is a novel reliability aspect of NCFETs that

is associated with the polarization overshoots that might occur during switching [26]. HAD raises reliability concerns as it can lead to dielectric breakdown in FeFETs and Landau FETs. However, in NCFETs, HAD is intrinsically mitigated, thanks to the operating voltage being lower than the coercive voltage of the ferroelectric layer, which reduces the required switching energy [27].

4. Gate Leakage. The presence of a finite current discharging the negative capacitance in NCFET can destabilize the system and cause a loss of the SS improvement. Nevertheless, it has been suggested that for fast enough gate voltage cycles, i.e., higher than the time it takes for the leakage current to discharge all the capacitors, NCFETs can still show steep-switching operation [28].

5. Flicker Noise. Fluctuations in the number of traps and in the mobility are at the origin of the so-called Flicker noise that, in turn, causes fluctuations in I_D [29]. Interestingly, NCFETs have been found to reduce Flicker noise, thanks to enhanced effective gate capacitance [30], with a scaling trend of I_D power spectral density with increasing T_{FE}.

As a general remark, we observe that reliability issues in NCFETs (and Landau FETs) can be potentially mitigated by the fact that these devices reduce static and dynamic power consumption simultaneously, so that the same I_{ON} compared to a stand-alone MOSFETs can be achieved at reduced V_{DD}. On the other hand, the fact that the internal potential between the ferroelectric and insulator layer has higher values than a normal MOSFET (due to voltage amplification) can lead to higher degradation in terms of TDDB, self-heating [31] and possibly also NBTI. Therefore, to ensure that NCFETs are able to meet requirements in terms of reliability, it is of paramount importance to properly design these transistors trading-off the reduction of SS with adequate lifetime.

1.2.4 Advanced Issues

We conclude the discussion on NCFETs by outlining the advanced issues related with the technology that are yet to be fully solved or that are still debated in the community. The reader should appreciate the fact that given the quite recent proposal of the NCFET, it is rather unexpected that fundamental theoretical aspects as well as valid experimental demonstrations are still under debate. We will briefly summarize these aspects, with the goal of addressing the most pressing questions that require further investigation to consolidate the NCFET technology.

Single- vs Multi-domain Models

The analysis of NCFETs in Section 1.2.1 relied on the tacit assumption that the polarization is uniform across the ferroelectric layer [7]. This simplified picture derives from the adoption of the phenomenological Landau theory, neglecting

the microscopic details of a ferroelectric layer. In general, a ferroelectric has multiple domains each associated with its polarization state (in the simplest case, either positive or negative) leading to an overall non-uniform polarization across the layer [32]. The models describing the spatial dependence of the polarization belong to the "multi-domain" models class compared to the "single-domain" class [18]. There are several practical implications of the non-uniform polarization. For example, it can lead to reduced [32] as well as complete loss of NC operation [33]. Further exploration of multi-domain aspects of ferroelectric layer in the NCFET is thus required to harness the negative capacitance behavior and to build-up predictive models to quantitatively characterize realistic NCFETs [34].

Quasi-static vs Dynamic NC Operation

The steady-state analysis of NCFET in Section 1.2.1 neglected the dynamical effects (recall that $\rho \mathrm{d}P/\mathrm{d}t = 0$). However, NCFET operation (in terms of steep sub-threshold switching) can also be interpreted with other models that rely on dynamical effects to explain the decrease of ferroelectric voltage with increasing applied bias. For example, in [35] the NC effect was attributed to the increase of the slope of the $P - V$ characteristic near the coercive field and to the polarization lag occurring during electric field AC sweeps. Thus, in [35], the internal voltage gain was explained with the Miller theory, which did not require the ferroelectric capacitance to be negative. Besides [35], there are other works that discuss possible other interpretations of the voltage amplification behavior observed in ferroelectric-dielectric stacks (FE-DE), as summarized in [18]. In the presence of different theories for the NC effect, a single model would need to prove self-consistently a whole set of features characteristic of these devices to convincingly explain NCFET operation. This is discussed more in detail in Section 1.2.4.

Experimental Results on NCFETs

Ever since the seminal paper by Salahuddin and Datta in 2008 [7], researchers have come up with experimental demonstrations of the NCFET concept, either on perovskite or doped-HfO_2 ferroelectrics and on a variety of different substrates [18]. However, published data have shown hitherto a relatively broad scatter of the measured SS values, especially related to the related hysteresis. This scenario is shown in Fig. 1.7, where experimental data of NCFET realized in different device technologies (i.e., Si, Ge/GeSn, 2D, III-V semiconductors) is compared. This level of scatter is a clear indication of the relatively limited maturity of the technology and needs to be reduced in order to guarantee the adoption of NCFETs into mainstream semiconductor industry.

NCFET Models for Advanced Transistor Architectures and Technologies

While in Section 1.2.1 we focused the analysis on long-channel bulk MOSFETs, the NCFET concept can be applied also to other transistor technologies. Indeed, there are several attempts in the literature to couple the LKE with electrostatic and transport equations to find self-consistently the solution to advanced transistor architectures and technologies. Some examples of such modeling efforts are: *i)* Dual(or Double)-Gate FET (DGFET) [36], *ii)* FinFET [37], *iii)* Gate-All-Around FET (GAAFET) [38, 39], and *iv)* MoS_2 Junctionless FET (JLFET) [40]. The interest in developing models for advanced transistor technologies is motivated by the scaling needs of the semiconductor industry, that require the reduction of the so-called short-channel effects as well as reduction in operating power. Indeed, NCFETs can prove instrumental in achieving these goals, provided that their distinctive features are proved in realistic devices, as discussed in the next paragraph.

Requirements to Prove the NCFET Concept

The interpretation of experimental demonstrations of NCFETs is further complicated by the debate around the theoretical aspects of the NC effect as derived from the Landau theory, as well as by the presence of other possible models explaining the observed reduction of SS. To unambiguously prove the NCFET concept on fabricated devices, it is not only necessary to demonstrate that SS is effectively reduced, but also a number of other features must be guaranteed. The necessary features to prove self-consistently the NCFET operation are [18]:

- Hysteresis-free steep sub-threshold switching with $SS < 60\,\mathrm{mV/dec}$;
- Negative Differential Resistance (NDR) in the output characteristics, i.e., the reduction of I_D with increasing V_{DS};
- Negative Drain-Induced Barrier Lowering (NDIBL), i.e., the increase in threshold voltage with increasing V_{DS};
- suppression of the $1/f$ Flicker noise measured in I_D.

The features outlined above (e.g., NDR, NDIBL, etc.) should be proven for a combination of dielectric and ferroelectric thicknesses, for different bias sweeps and also for a range of frequencies (to determine the speed limits of the technology). These requirements provide an operative procedure to conduct experiments to systematically prove NCFET operation.

1.3 Device Physics of PhaseFETs

In the Introduction, we mentioned that PhaseFET is a non-thermionic device that allows steep-slope switching by focusing on the channel transport and reducing channel transport factor, n, below 60 mV/dec. PhaseFETs are composed

of the series of a MOSFET and a non-linear variable resistor connected to the source, as sketched in Fig. 1.9(a). Less commonly, some devices connect the variable resistor (also called Threshold Selector (TS)) to the drain, as in [41]. The variable resistor connected in series to the MOSFET is realized with a PTM that shows an abrupt switching between two stable low- and high- resistance states. Some examples of PTM are vanadium dioxide (VO_2) [5] or Ag/TiO_2 [41]. In general, the phase-transition involves Insulator-To-Metal Transition (IMT) and Metal-To-Insulator Transition (MIT) as a response to an external stimulus (i.e., temperature, pressure, electric field) and this leads to sharp transitions in the current-voltage characteristics of the device. The corresponding transition between on- and off-operation leads to steep SS switching.

Compared to other options (e.g. tunnel FET or MEM-relay), a PhaseFET may be easier to integrate into an existing MOSFET process-flow because the phase-changing element can be embedded among the interconnects within the backend. In this section, we will discuss more details on the physics of phase transition and describe the general framework of operation of the PhaseFET. The theory of PhaseFET is not as well developed as tunnel-FET or Landau-FET. We will focus on two phonomenological approaches (e.g. behavioral model and coupled electro-thermal model) to provide a broad understanding of the potential of PhaseFET circuits.

1.3.1 Behavioral Models for Circuit Applications

To understand the operation of the PhaseFET, we can employ a simple behavioral model that captures the abrupt resistivity change in a general way and that can be coupled to a MOSFET model to obtain a self-consistent solution of the drain current vs gate-to-source voltage. The behavioral model assumes that the high- to low-resistive switching occurs at a threshold voltage, V_1, while the high-to-low switching occurs at a second threshold, V_2 [42]. Since $V_2 < V_1$, the device traces different I-V paths depending on the direction of voltage sweep, resulting in hysteretic switching in response to an off-on-off input pulse. This is illustrated in Fig. 1.9, where the simple circuit shown in panel (b) is simulated to obtain the $I_D - V_{GS}$ characteristic shown in panel (c). The characteristics of PhaseFET compared to the standalone MOSFET are much steeper during turn-on and turn-off, however, hysteresis is present, as mentioned previously. In this regard, both NCFET and PhaseFET must balance clear advantage of SS reduction against the hysteresis inherent in the transition. We note that while an NCFET can be designed to be essentially hysteresis-free, it is difficult to completely eliminate the hysteresis in PhaseFETs. This has to do with the physics of abrupt resistive switching that inherently occurs at different thresholds depending on the previous state of the device. Nevertheless, appropriate material choice [43] can reduce the PhaseFET hysteresis to a level tolerable for a given application.

1.3.2 Physic-based Phenomenological Model for Device Optimization

The PhaseFET behavioral model explains device operation empirically, but it does not allow to connect the abrupt resistance change to the physical mechanism inducing phase transition (i.e., either electrical or temperature switching). An improved phenomenological PTM model should self-consistently solve for the electrical and thermal behaviors of the PhaseFET. This would allow phase transition through Joule heating in the VO_2. The abrupt resistance variation can be captured by an empirical model [44, 45]:

$$R_{PTM} = R_{LRS} + \frac{(R_{HRS} - R_{LRS})}{1 + \exp\left[(T - T_c)/T_x\right]} \tag{1.14}$$

where R_{LRS} (R_{HRS}) is the low- (high-) resistance state value, T_c is the critical temperature at which transition occurs and T_x is an empirical parameter. The temperature variation is determined by the following first-order differential equation:

$$C_{th}\frac{\mathrm{d}T}{\mathrm{d}t} = V_{PTM} \times I_{PTM} - \frac{T - T_0}{R_{th}} \tag{1.15}$$

where C_{th} (R_{th}) is the thermal capacitance (resistance), T_0 is the ambient temperature and V_{PTM} (I_{PTM}) is the voltage across (current flowing in) the PTM. Notice that this equation connects the Joule heating term $\sim V \times I$ and the thermal properties of the device, i.e., C_{th} and R_{th}.

Although this modeling approach might be good enough for circuit simulations, it is still not adequate for realistic physics-based modeling, for which the resistivity variation needs to be connected to the material properties and more fundamental theory. One possible way of accomplish this, is to rely on MottFET theory, which provides a theoretical framework to explain phase transition [6]. Materials like VO_2 in fact, belong to the class of Mott insulators, that exhibit an abrupt (but reversible) IMT when the internal temperature exceeds a critical value, T_c [6]. Although the MottFET, employing a PTM as the channel of the transistor, has not been demonstrated yet, understanding the details behind PTM in Mott insulators is instructive to harness the interesting physics associated with phase transition.

The MottFET theory allows us to model the IMT/MIT with bandgap, E_G, and thermal conductivity, κ, variations. As temperature varies in a PTM, the bandgap is modified through the following relation [6]:

$$E_G = E_{G,0} - \frac{E_{G,0}}{1 + a\exp\left[-b(T - T_c)\right]} \tag{1.16}$$

where a, b are intrinsic material parameters specific to the Mott insulator. Associated with the bandgap collapse, which determines the electrical behavior, is the variation in thermal conductivity which effectively controls the thermal behavior:

$$\kappa = \kappa_0 + \frac{(\kappa_1 - \kappa_0)}{1 + a\exp\left[-b(T - T_c)\right]} \tag{1.17}$$

where κ_0 (κ_1) is the thermal conductivity of the insulator (metal) phase, respectively. This approach of modeling bandgap and thermal conductivity variations allows for an accurate description of the observed temperature dependence of carrier concentration and resistivity, enabling predictive analysis for a variety of novel devices based on Mott insulators [6].

1.3.3 Experimental Results on PhaseFETs

Similarly to Fig. 1.7 for NCFETs, we summarize in Fig. 1.10 the data of fabricated PhaseFETs present in the literature [5, 11, 41, 46, 47, 48, 49, 50]. The measured data for PhaseFETs also shows a relatively broad scatter of SS vs hysteresis values. We note that SS for PhaseFET is much lower than that of NCFETs: in fact PhaseFET have almost ideal on-off switching, i.e., $SS \sim 0\,\mathrm{mV/dec}$. On the other hand, hysteresis is generally much larger in PhaseFETs than NCFETs (always higher than 100 mV). Thus, once again, the technology choice for a given application must be based on the trade-off between SS and hysteresis.

1.4 Boolean Computing with NCFETs, FeFETs, and PhaseFETs

With the understanding of the device operation of NCFETs and PhaseFETs, we now present their circuit implications. To complete the picture on the applications of FE-based devices, we will also discuss FeFET-based circuits which utilize the hysteretic characteristics as opposed to NCFETs that utilize steep switching. In this section, we will focus on applications targeted towards Boolean computing in the context of both digital logic and memories. In Section 1.5, we will discuss the potential of using such new technologies for non-Boolean computing.

1.4.1 Logic Design

In the context of the design of digital logic primitives, NCFETs and PhaseFETs exhibit promising characteristics such as steep switching (either due to NC effect or abrupt polarization switching, respectively) and therefore, can potentially enable aggressive voltage scaling. The question, however, is whether or not these devices can be or should be used as drop-in replacements of standard transistors or if new design techniques will be needed to translate the device-level benefits to optimal circuit performance. Here, we will address this question and highlight the importance of technology-circuit co-design to enable NCFET and PhaseFET-based low power logic. We will discuss the circuit behavior both from the perspective of DC Voltage Transfer Characteristic (VTC) (which dictates the gain and noise margins of the logic gates) as well as transient response (which determines the energy efficiency and speed).

NCFET-based logic

Logic gate implementation prefers non-hysteretic NCFET operation to avert polarization switching (and the associated delay/energy overheads) as well as to simplify the design of logic gates (since NCFETs can be directly used as drop-in replacements of MOSFETs). Hence, in this section, the focus of our discussion will be on logic design with non-hysteretic NCFETs.

The very NC effect that gives rise to steep switching in NCFETs also leads to a concomitant increase in their gate capacitance [51]. Thus, for digital logic, the benefits of higher on-current at iso-off current (due to steep switching) may be offset by the increase in the fanout (gate) capacitance. Also, the viscosity coefficient of the ferroelectric, ρ, may affect circuit delay [51]. In addition, the steep switching in NCFETs is often accompanied by NDR in the output characteristics [51, 52]. Here, we will discuss the overall effect of such unique NCFET properties on circuit behavior.

From the perspective of the DC response, steep switching in NCFETs leads to sharper VTCs compared to Complementary Metal-Oxide-Semiconductor (CMOS) circuits, which implies higher gain and improved noise margins [51]. However, the story does not end here. NDR in NCFETs leads to some unique VTC attributes, especially at sufficiently large ferroelectric thickness. Specifically, the VTC becomes hysteretic due to NDR (Fig. 1.11(a) - see [51] for more details), even though the device is non-hysteretic. This leads to improved noise margins for Boolean applications. This unique feature can be used to design oscillators, as discussed later in Section 1.5.1.

Let us now come to the energy-delay analysis of NCFET-based logic. Here, we need to consider the interplay between higher on-off current ratios and larger gate capacitance (compared to CMOS) as well as the viscosity coefficient of the ferroelectric layer, ρ. While the viscosity coefficient still needs further characterization, recent experiments have indicated that ρ may be as low as $0.18\,\Omega$.cm [53]. Nevertheless, here (in Fig. 1.11(b) adapted from [51]), we show the characteristics for different values of ρ to illustrate its effect. It can be observed that NCFETs show lower delay at iso-energy compared to CMOS circuits in the low voltage regime due to higher on-current. At high voltages however, the delay associated with charging/discharging of the circuit nodes is small, and thus, the relative contribution of ρ to the overall circuit delay increases [51]. As a result, NCFET-based logic can show delay increase for large ρ. However, if ρ can be reduced, the benefits of NCFETs can be extended to a larger voltage range. In addition, NCFET circuits show higher energy-delay improvements over CMOS with the increase in the contribution of wire (back-end load) to the overall load. This is because large wire capacitance mitigates the effect of higher gate capacitance of NCFETs [51].

We will end this section by emphasizing that to maximize the benefits of NCFETs, design of devices (e.g., T_{FE} optimization) needs to be coupled with circuit design (e.g. voltage optimization, back-end and front-end fanout etc.). With proper design, NCFET-based circuits exhibit performance benefits, especially at low voltages. Further, their unique NDR characteristics can lead to

Schmitt trigger action in NCFET-based logic gates, which can be beneficial for noise immunity.

PhaseFET-based logic

Similar to NCFETs, PhaseFETs offer steep (in fact, abrupt) switching, which can potentially be beneficial for logic design. However, one important distinction is that unlike NCFETs, PhaseFETs cannot have non-hysteretic characteristics [43]. (The only exception to this is a very specific design point where the gate voltage associated with IMT and MIT can theoretically be matched by design; however, such a design would be impractical as a small variation can lead to the phase transition material going into the oscillatory mode [54], which is detrimental for logic operation). With hysteretic and abrupt transfer and output characteristics of PhaseFETs, logic design becomes non-trivial [55].

In order to obtain proper functionality and performance gains, the resistance ratio of the insulating and metallic state of the PTMs can neither by too high (in which case, the devices and circuits will fail to function) nor too low (in which case, PhaseFETs will not show any improvement in the on-off current ratio [43]). Moreover, the transition voltages associated with IMT and MIT need to be tailored by proper device-circuit co-design to ensure that the phase transitions in the PTM occurs to enable the required circuit functionality (for instance, complete voltage swing in the logic gates [55]).

The VTC of properly-designed PhaseFET-based logic gates (obtained from DC characteristics - Fig. 1.12(a)) are quite unconventional, showing hysteresis in the non-transition region (which is a result of the intrinsic device hysteresis). VTCs also indicate an "apparent" reduction in the noise margins [43] due to the high insulating state resistance of the PTMs in the pull-up and pull-down paths. However, this effect is not as severe as predicted by the DC characteristics and the dynamic change in the resistance of the PTMs during the circuit operation due to IMT significantly improves the noise margins by establishing a low resistance path to either V_{DD} or ground [55].

The energy-delay analysis of PhaseFETs (see Fig. 1.12(b) [55]) shows that PhaseFETs exhibit delay reduction at iso-energy at low voltages (similar to NCFETs) by virtue of their steep switching and higher on-off current ratio. At high voltages however, the transition time associated with IMT and MIT degrades the performance of PhaseFETs. Hence, novel PTMs may need to be explored that not only meet the resistance and transition voltage requirements to support the logic gate functionalities but also exhibit low transition times and high stability to enhance the benefits of PhaseFET-based logic at high operating voltages as well.

It is noteworthy that for multiple-input gates, it may not be judicious to use PhaseFETs as drop-in replacements of standard MOSFETs (unlike for NCFETs). Instead, only one PTM is needed for a set of series-connected transistors in a logic gate [55]. For instance, a 2-input NOT-AND (NAND) gate is shown in Fig. 1.13(a). This design employs 2 parallel PhaseFETs in the pull-up network (PUN), but instead of using two series PhaseFETs in the pull-down

network (PDN), a single PTM is placed in series with the n-type transistors. This design has the following advantages: (1) by avoiding two series PTMs, the effect of the metallic resistance of the PTM on the logic gate speed is reduced, (2) diffusion/contact sharing between the two series n-transistors (as in standard CMOS) becomes possible, thereby averting area penalty due to PTMs (Fig. 1.13(a)) and (3) the regulation of IMT/MIT of a single PTM and its interactions with the network of series-connected transistors becomes easier (compared to two PTMs in series), which makes the design more robust to variations. Note, similar to an inverter, the width of the series-connected transistors and the PTM geometry need to co-optimized, to achieve the correct functionality of the gate, sufficient noise margins, complete voltage swing and energy-delay benefits. The idea of using a single PTM per series network of transistors can be easily extended to other complex gates. For instance, an AND-OR-INVERT (AOI) gate based on PhaseFETs is shown in Fig. 1.13(b).

1.4.2 SRAM Design

Similar to the logic design, the implementation of Static Random Access Memories (SRAMs) with NCFETs and PhaseFETs requires careful co-design of devices and circuits to harness the maximum benefits. In fact, the importance of utilizing the unique attributes of the devices becomes even more critical in SRAMs because of the self-conflicting design requirements for read and write. In this section, we briefly review NCFET- and PhaseFET-based Six Transistors SRAMs (6T-SRAMs).

NCFET-based SRAM

NCFETs, in their non-hysteretic mode, can be used as drop-in replacements of MOSFETs in a 6T-SRAM cell (Fig. 1.14(a)). By virtue of their steep switching, NCFETs naturally offer higher read and hold stabilities (Fig. 1.14(b)) [56]. However, by utilizing the NDR in their output characteristics (with proper optimization of T_{FE}), Schmitt trigger action (or hysteretic response in their DC characteristics) is achieved, which further improves the read and hold noise margins [57]. Furthermore, access time of NCFET-based SRAMs at iso-leakage and iso-area is lower due to higher I_{ON}. The overhead of higher gate capacitance in NCFETs is significantly mitigated due to the wire capacitance associated with word-lines and bit-lines. The write-time of NCFET-based SRAMs is strongly dependent on ρ: for ρ close to $0.18\,\Omega$.cm [53], write time improvement is observed, mainly due to higher I_{ON} in NCFETs. However, increase in ρ lessens these benefits and may even degrade write time [56]. Hence, proper device design coupled with cell optimization (including the possible use of read/write assist techniques) is needed in NCFET-based SRAMs to mitigate the design conflicts and achieve superior design solutions compared to their CMOS counterparts.

PhaseFET-based SRAM

Unlike NCFETs, employing PhaseFETs as drop-in replacements in 6T-SRAMs may yield a sub-optimal design. As an example, the additional resistance given by the PTM in the access PhaseFET in 6T-SRAMs may reduce the cell leakage and bit-line leakage, but can lead to a significant degradation in the write-ability and read speed. Similarly, if both the pull-up and pull-down transistors of6T-SRAM are implemented using PhaseFETs, the stability of the cell (especially during read) may be degraded considering process variations. Therefore, it becomes important to selectively employ PhaseFETs in conjunction with standard transistors in SRAMs to utilize their unique properties (such as abrupt switching) for mitigating the read-write conflicts.

In [58], it is shown that using PhaseFETs as the pull-down transistors, while using MOSFETs as pull-up and access transistors can be beneficial to simultaneously increase the read stability, hold stability and write-ability without any increase in the area, albeit at the cost of the access time. The key idea is as follows. During read, the cell is designed to trigger IMT in the PTM of the PhaseFET driving the node storing '0' so that read current can flow. On the other hand, the other PTM remains insulating, which increases the trip point (or logic threshold voltage) of the corresponding inverter in the SRAM cell. This significantly improves the read stability. During write, two scenarios can occur depending on the design: either (1) the PTM driving node storing '0' undergoes IMT followed by MIT while the other PTM remains insulating or (2) both PTMs remain insulating. Irrespective of which case occurs, write-ability is significantly improved due to insulating PTMs. Thus, by triggering operation-driven phase transitions in the PTM, the read-write conflicts present in standard SRAMs can be mitigated. For the details of this design and other related aspects (such as hold stability, area, the impact on the unaccessed cells etc.) the reader is referred to [58].

In addition to the 6T-SRAMs, PTMs have also been shown to improve the read functionality in SRAMs and Dynamic Random Access Memorys (DRAMs) with separate read-write paths at a minimal area cost [59]. Besides, PTMs have also been used as a technology assist to design non-volatile SRAMs [60].

1.4.3 Non-Volatile Memory Design

In the following we discuss the design of novel Non-Volatile Memory (NVM) technologies based on FeFET and PhaseFET, and the specific constraints introduced by the integration of either the ferroelectric or PTM layer with conventional devices.

FeFET-based NVMs

FE materials have been widely accepted as an attractive storage element for non-volatile memories. Therefore, in addition to the applications of FE in NCFET-based logic/SRAM designs, we consider it is important to briefly review the applications of FeFETs in NVM designs.

Traditionally, NVMs based on FE-Capacitor RAMs (FeRAMs) have been amongst the most promising technologies and have been implemented in industry using their unique property of polarization retention in the absence of an external electric field [61]. They offer high endurance along with high integration densities close to DRAMs. However, they suffer from low read distinguishability. Moreover, their read operation is destructive and requires a write back operation, leading to large energy overheads [62].

More recently, the possibility of direct integration of FE layer in the gate stack of MOSFETs, as skematically depicted in Fig. 1.15(a), has led to the realization of non-volatile FeFETs [63]. Moreover, the HfO_2-based FE enable a scalable (and CMOS compatible) emerging NVM that keeps up the pace with the scaling demands of leading-edge logic technologies [63]. In this memory device, the binary states are encoded in the form of the FE polarization (P). The direction (and value) of P determines the resistance state, either Low Resistive State (LRS) or High Resistive State (HRS), of the underlying transistor [64], see Fig. 1.15(b). For storing the memory state in the FE layer (and to switch between LRS and HRS), a V_{GS} of appropriate polarity and value greater than the coercive voltage of the FE is applied. To sense the memory state, I_D of the FeFET is used, thus separating the read and write paths. Moreover, the read operation (in FeFETs with MFIS gate stack - see Fig. 1.2(a)) is no longer destructive and the distinguishability is significantly improved by virtue of the gain of the transistor coupled with polarization switching [64].

Although FeFETs are immensely promising due to their electric field-driven write, read-write path separation and CMOS compatibility of HfO_2-based ferroelectrics, the variability associated with the domain nucleation and propagation as well as the traps in FeFETs (especially with MFIS gate stack [65]) needs to be tackled. FeFETs with MFMIS mitigate this issues and other challenges related to hysteresis optimization [66]. However, gate leakage can adversely affect such devices, resulting in the need for more advanced read schemes, which may incur in energy overheads [67].

For FeFETs with dominant single-domain behavior, especially for MFMIS gate stacks [68] or those at highly scaled technology nodes, the design of NVM arrays is fairly distinct compared to FeFETs with explicit multi-domain characteristics [66]. Here, we will briefly review both.

For the former category, various designs spanning highly compact 1T NVM to a more robust 4T NVM have been explored, as shown in Fig. 1.16 [69, 62, 70, 71]. To design the NVM arrays, selective access of the FeFET NVM cells needs to be facilitated. In the 1T design [69], this is achieved by utilizing the drain coupling with the ferroelectric layer in the FeFET. While highly compact, the design margins of this cell needs further exploration. The other designs [62, 70, 71] achieve selective access in the array by employing access transistors. In all these designs, a write access CMOS transistor is required to isolate the write paths of the unaccessed cells from that of the accessed cell. In the 2T (one MOSFET and one FeFET) design proposed in [62], an unconventional read scheme is adopted to minimize the flow of the read current through the unaccessed cell. To circumvent the overheads of the complex read scheme, 3T (two

MOSFETs and one FeFET) design uses a read access transistor, albeit at the cost of area. The write operation of 1T, 2T and 3T designs needs both positive and negative voltages [69, 62, 70]. To avert the use of negative write voltages (thereby, reducing the associated energy overheads), 4T (three MOSFETs and one FeFET) design [71] uses a third access transistor. The other design option for all-positive write voltages is to use a 2-phase write operation, as explored in [72]. The features common to all designs include: (a) the application of write voltages on bit-lines so that positive or negative V_{GS} greater than the coercive gate voltage appears across the FeFET of the accessed cell and (b) the application of read voltages on the sense lines to facilitate drain current flow through the accessed transistor, which can then be sensed by the sense amplifier.

Recently, Multi Domain FeFET (MD-FeFET) (with MFIS gate stack) have been explored for memory applications [66]. Their unique characteristics of polarization-dependent threshold voltage shifting (similar to NAND flash memories) has enabled the possibility of a ultra-high density 1T FeFET NVM [66]. Moreover, the same multi-domain characteristics have also been extensively proposed for multi-level memory cells as synapses in neuromorphic applications [73], as we will discuss later. However, the scalability of multi-domain ferroelectrics needs further exploration and the techniques to engineer the domain sizes and distributions can potentially pave the path for MD-FeFET-based NVM designs.

In addition to standard memories, FeFETs have been utilized to design Content Addressable Memories (CAMs) showing promise of high energy efficiency [74]. In addition, novel device structures such as Reconfigurable FeFETs (R-FeFETs) have been proposed that dynamically change their operation between non-volatile and volatile modes. These devices lower the power consumption of NVMs, mitigate the issues associated with gate leakage [75] and achieve differential memory designs [76]. In addition, the run-time modulation of hysteresis in R-FeFETs enables efficient logic-memory coupling for new applications such as logic-in-memory [76] as well as memory-in-logic [77].

PhaseFET-augmented MRAMs

Unlike FEs in FeFETs, PTMs employed for the design of PhaseFETs do not offer non-volatile characteristics. Hence, they cannot be directly utilized to design NVMs. However, by virtue of the large resistance ratio between their insulating and metallic states, PhaseFETs can be harnessed to augment the design of NVMs that inherently have low distinguishability (such as spin-based memories [78]). In [79], Magnetic Random Access Memories (MRAMs) have been designed with PhaseFETs (Fig. 1.17(a), (b)) by coupling the non-volatility of Magnetic Tunnel Junction Memories (MTJs) with the high ratio of insulating resistance and metallic resistance of the PTMs. The key idea behind MRAMs is to trigger operation-driven phase transitions in the PTM depending on the data stored in the MTJ. During the hold operation, the PTM remains in the insulating state. During the write operation, the PTM operates in its metallic state by design. This minimizes the adverse effect of PTM resistance on the write speed. During the read operation, PTM undergoes data-dependent selective phase transition.

First, on the assertion of the word-line, IMT is triggered in the PTM. The cell is designed such that if the MTJ is in the low resistance parallel state, cell current is high enough to keep the PTM metallic. However, if the MTJ is in the high resistance anti-parallel state, low cell current triggers MIT, thus significantly increasing the resistance of the cell. In this manner, the distinguishability of the spin-memories can be enhanced by synergistically utilizing the non-volatility of MTJs with orders of magnitude resistance difference between insulating and metallic phases of the PTMs. Results from [80] (Fig. 1.17(c)) show that in addition to a large increase in the sense margin, a simultaneous increase in read disturb margin and a moderate write power reduction is achieved with this technique without any area penalty but with a negligible write time increase. In [79], read improvements under process variations is also established.

In addition to this technique (with series MTJ-PTM connection), PhaseFETs can be used in spin-memories with separate read-write paths such that the PTM is connected in parallel with the MTJ [81]. This design also considerably improves the read operation without affecting the write operation (due to the separation of read-write path). Moreover, instead of amplifying the distinguishability at the cell level (as in the aforementioned techniques), this design principle can be extended to the array level, wherein PhaseFETs are utilized to design compact low power sense amplifiers, in which the core amplification occurs in the PTM (see [82] for details).

Furthermore, PTMs (without transistors) have also been explored to design cross-point NVM architectures, wherein the abrupt switching of the PTMs is utilized to design selectors with high non-linearity [83].

1.5 Non-Boolean Computing with NCFETs, FeFETs, and PhaseFETs

In the previous section, we presented the potential applications of NCFETs, FeFETs and PhaseFETs for standard Boolean computing and storage. In this section, we will extend our discussion to non-Boolean computing, wherein we will highlight how the unique attributes of these technologies enable circuits that can cater to the demands of emerging applications. Before we dive into the discussion, let us understand the application perspective for non-Boolean computing. Traditional computing based on Boolean logic and von-Neumann architectures has been immensely successful in the era of predominant compute-intensive tasks. However, with the advent of data-intensive applications such as recognition, machine learning etc., the standard architectures prove to be inadequate to meet efficiency demands. Hence, new computing approaches are being explored that mitigate the limitations of Boolean computing by customizing the architectures, circuits and technologies to meet the demands of the new applications. Here, we will focus on two non-Boolean computing approaches: (1) coupled-oscillators-based computing and (2) neuromorphic computing.

1.5.1 Coupled-Oscillators-based Computing

For certain tasks involving associative computing (e.g. pattern matching) or solving of optimization problems (e.g. graph coloring), coupled-oscillator-based processing has emerged as a promising computing paradigm. The key idea is to couple multiple oscillators whose oscillation frequency is controlled by the inputs. If the degree of matching of the inputs is high or other interactions are strong, the oscillators get frequency- or phase-locked. Otherwise, they show asynchronous oscillations. This working principle is utilized to find the minima in optimization problems or perform recognition/matching tasks. While CMOS-based oscillators have been utilized for this purpose, it has been shown that emerging technologies can potentially offer higher energy efficiency [84, 85, 86]. Here, we will discuss how NCFETs, FeFETs and PhaseFETs enable the design of energy-efficient coupled oscillators.

NCFET/FeFET-based Coupled Oscillators

FE-based transistors, namely - (a) NCFET which shows steep switching and NDR and (b) FeFET with hysteretic transfer characteristics have emerged as promising candidates for compact and low-power beyond-von-Neumann architectures powered by their unique device features. An example application based on these architectures is associative computing, for which oscillator-based networks has been a subject of recent study [85, 86]. By leveraging special device-circuit capabilities of NCFET/FeFET, oscillators with significantly reduced transistor count compared to their CMOS-based counterparts are realizable [85, 86].

In [85], an oscillator with one FET and one FeFET (Fig. 1.18(a)) was proposed. The design utilized abrupt polarization switching and hysteretic transfer characteristics of FeFETs. The key idea is illustrated in the load-line plot of Fig. 1.18(c). This circuit would show stable solution if the load line (corresponding to the FET) intersected with the transfer characteristics of the FeFET. With proper design, it can be ensured that the load does not intersect in the flat (solid-line) regions of the FeFET characteristics, ensuring that (as a result of the lack of a stable DC solution) oscillations build-up as shown in Fig. 1.18(d). This technique is similar to the approach explored for other technologies such as PTMs that we will discuss later on. The design proposed in [85] shows relaxation-type oscillations. Synchronization between two oscillators has also been shown, which can be useful for non-Boolean applications. The oscillatory behavior has also been experimentally demonstrated in [87] utilizing a perovskite-based (e.g., $BaTiO_3$) FeFET. However, since this oscillator design relies on abruptness of polarization switching, it needs to be further explored in the context of CMOS-compatible HZO based ferroelectrics, which are polycrystalline and hence, are expected to have smoother polarization switching due to multi-domain effects [88].

In [86], NCFET/FeFET-based oscillators (Fig. 1.19(a)) utilize a different mechanism to achieve oscillations. They rely on Schmitt trigger action or hys-

teretic VTC of inverters (see - Fig. 1.11(a)). In contrast to the 6T CMOS based-Schmitt trigger, NCFETs and FeFETs lead to hysteretic VTC with just two transistors by virtue of: a) NDR in NCFETs (discussed in Section 1.4 - Fig. 1.11(a)) or b) hysteretic transfer characteristics ($I_D - V_{GS}$) of FeFETs (discussed in Section 1.4 - Fig. 1.15(b)). Hysteretic VTC is translated to voltage controlled oscillations by a feedback, R_f, from output to input of the inverter. Depending on whether R_f is realized as a Pass Transistor (PT) or Transmission Gate (TG), the oscillator outputs a variety of oscillations, viz. (a) relaxation type with PT in both NCFET (Fig. 1.19(b)) and FeFET (Fig. 1.19(d)) implementations, (b) 'sinusoid-like' with TG in NCFET-based design (Fig. 1.19(c)) and (c) 'pulse-like' in with TG in FeFET design (Fig. 1.19(e)). Moreover, dynamic re-configuration between relaxation and 'sinusoid/pulse-like' characteristics is achievable by tuning the bias of P-transistor in TG. Their coupled-dynamics have also been analyzed, which show promise for non-Boolean computing ([86]).

Each of the aforementioned designs have their own benefits and trade-offs. While the design in [85] offers a highly compact solution, the oscillator in [86] has been shown to achieve higher oscillator frequencies in simulations and can be implemented even if the polarization switching dynamics is not abrupt. Moreover, the latter design can be realized by both NCFETs and FeFETs.

PhaseFET-based Oscillators

Phase transition materials (PTMs) and PhaseFETs offer intrinsic abrupt characteristics and therefore, are highly suitable for the realization of relaxation oscillators. In [84], VO_2 has been used in the design of nano-oscillators (Fig. 1.18(b)). The working principle is based on using a series-connected resistor (or transistor) to prevent the system to stabilize in a particular phase (or find an intersection point in the load line plot - Fig. 1.18(c) by leveraging the abruptness in the current-voltage characteristics. Recall that a similar principle was used in FeFET-based oscillators [85] discussed before. Here, we describe this mechanism in a greater detail.

Let us consider in Fig. 1.18(c) that the PTM is in the insulating state initially. Hence, the resistor (or transistor) will charge the output node (V_0 - Fig. 1.18(c)). As the output voltage (or voltage across PTM) increases, IMT is triggered in the PTM. This establishes a low resistance path from the output to ground and the output start discharging. As the output (and hence, PTM) voltage decreases, PTM undergoes MIT. This breaks the path to ground and the resistor (or transistor) again begins to charge the output. This keeps repeating, leading to sustained oscillations as shown in Fig. 1.18(d). The gate voltage of the series transistors (not shown in Fig. 1.18(b)) can be used to tune the oscillation frequency, thus achieving voltage-controlled oscillations.

Further, the coupled dynamics of PTM based oscillators have also been analyzed in [89] suggesting that the dynamics can be tuned by modulating the resistance of the series transistor, effective capacitance of PTM devices (dependent on PTM dimensions) and coupling capacitance.

1.5.2 Neuromorphic Computing

Neuromorphic computing is yet another form of non-Boolean computing that draws its inspiration from the way our brain processes data (or at least the little that we understand of it). Like for the human brain, the primitives of neuromorphic computing are neurons (or thresholding elements that fire when their weighted sums of inputs exceed a certain value) and synapses (or weights that determine the strengths between different neurons) [90]. Amongst the many challenges of neuromorphic computing, low power hardware implementation of neurons and synapses remains one of the key areas of exploration.

While several existing neuromorphic architectures [91] employ CMOS technology, their energy efficiency is nowhere close to our brain. To bridge (or at least narrow) this gap, post-CMOS technologies that are intrinsically more amenable to the functionalities of the neuromorphic primitives are being actively investigated. Here, we review how FeFETs and PhaseFETs can enable low power neurons and synapses by virtue of their unique attributes.

FeFET-based Synapses

In FeFETs, under certain conditions [92], the FE can form multi-domains with alternating polarization directions (see Fig. 1.20(a)). In this Multiple Domain (MD) scenario, the average macroscopic polarization, $\bar{P}$, depends on the relative size of the $+P$ and $-P$ domains, which can be tuned by applying a gate voltage pulse, V_{PULSE} as shown in Fig. 1.20(b) and thereby, inducing a domain-wall motion. Such changes in $\bar{P}$ modify the channel carrier concentrations due to the electrostatic coupling between the FE and the semiconductor. Alternately, the V_T of FeFET changes due to the change in $\bar{P}$ (see Fig. 1.20(c)), which is analogous to the dependency of V_T on the fixed oxide charge in MOSFETs. Moreover, the change in $\bar{P}$ is dependent on the magnitude and time duration of V_{PULSE} [88]. Therefore, by modulating V_{PULSE}, the V_T of the FeFET can be tuned and thus the channel conductivity ($G_{DS} = I_D/V_{DS}$) can be modified gradually. This gradual change in G_{DS} in MD-FeFETs (see Fig. 1.20(d)) can readily be exploited to mimic multi-level synaptic behavior.

FeFET based multi-level analog synaptic devices have been experimentally demonstrated in [93], where the G_{DS} potentiation and depression via a gradual V_T tuning were obtained by applying a voltage pulse at the gate terminal. However, in case of identical voltage pulses, the observed potentiation and depression characteristics are highly non-linear and asymmetric with respect to the number of pulses. To overcome such non-idealities, different non-identical pulsing schemes were proposed in [93]. These schemes utilize a gradual modulation of pulse amplitude or duration to improve the potentiation/depression linearity and symmetry. However, if pulses are not identical throughout the programming process, an additional step of accessing the synaptic weight (G_{DS} value) is needed every time an update takes place so that an appropriate pulse can be applied. This leads to design overheads and may increase the energy consumption of the network during training. In this regard, by using identical

pulses, an improved linearity and asymmetry was experimentally demonstrated in a Ferroelectric Germanium NanoWire FET (Fe-GNWFET) [94].

In addition, an FeFET synapse featuring Spike Time-Dependent Plasticity (STDP)-based update scheme has been demonstrated in [73] for Spiking Neural Networks (SNNs). The proposed circuit design is shown in Fig. 1.21(a), where a resistor is connected between the gate and the drain terminals of the FeFET to enable the two-terminal operation of the synapse. With this circuit design and the spiking waveform proposed in [73], the relative spike timing between the pre- and the post-neuron can be converted into a voltage-drop across the FeFET. As a consequence, closer the pre- and post-neuron spiking in the time domain, higher is the voltage-drop across the FeFET, and larger is the change in G_{DS}. The STDP pattern considering the synaptic potentiation and depression is qualitatively depicted in Fig. 1.21(b).

FeFET-based Neurons

In a spiking neural network, the basic functionality of a spiking neuron is to integrate the voltage spikes fed to its excitatory input over a period of time and to generate an output spike (called fire) when the integrated quantity becomes higher than a threshold value. In addition to these Integrate and Fire (IF) behaviors, a neuron may also feature a leaky property while integrating spikes, and is referred to as Leaky Integrate and Fire (LIF) neuron. So far, different flavors of FeFET-based spiking neurons have been experimentally demonstrated, which we briefly discuss in this section.

The FeFET spiking neuron demonstrated in [87] comprises of 1T-1FeFET structure, where the FE layer, made out of Lead Zirconium Titanate (PZT), is separately connected at the gate of the underline transistor with a metal (Fig. 1.22(a)). In this design, the 'leaky' and 'integration' functionalities of the neuron have been implemented in the the external RC circuit, whereas the abrupt 'firing' event has been mimicked through the abrupt polarization switching of FE in response to the input spikes at the gate of the FeFET (Fig. 1.22(a)).

The FeFET neuron demonstrated in [95] (comprising of 1R-1FeFET as shown in Fig. 1.22(b)) does not need an RC network and can mimic the leaky-integration behavior by utilizing the inherent polarization switching dynamics of FE. In this design, a M-FE-M capacitor is connected to the gate of the underlying transistor to form the FeFET structure. A thin partially-crystallized Zirconium-doped Hafnium Oxide (HZO) layer is used so that the tunneling current can induce the leaky behavior in M-FE-M capacitor. For integration functionality, multi-domain polarization switching behavior is utilized (described earlier in the context of MD-FeFET synapse), so that the spiking inputs at the FeFET gate terminal gradually modulate the channel conductivity and hence, change the output voltage of the 1R-1FeFET circuit to generate a voltage spike (Fig. 1.22(b)).

The FeFET based neuronal dynamics demonstrated in [96] utilizes the polarization accumulation of FeFETs. Unlike the previous designs [95, 87], the FE layer (HZO) is directly integrated in the gate stack of FeFET. When a voltage pulse is applied to the FeFET gate for a limited time duration (typically less than

the writing time of FeFET NVM) the polarization does not switch completely but merely changes incrementally. However, after a certain number of pulses are received, the FeFET abruptly switches to the LRS. Such phenomenon can be understood as the initial nucleation of nano-domains followed by an abrupt polarization reversal of the entire FE layer. Now, the applied pulses prior to the latching of the LRS can be regarded as the process of 'integration' of excitatory inputs, whereas, the subsequent abrupt transition from HRS to LRS can be regarded as the 'firing' event. To obtain the leaky behavior, a proposed option is the insertion of a negative inhibitory voltage in the intervals between consecutive excitatory pulses.

Apart from this externally emulated leaky feature (by applying an additional inhibitory signal), the possibilities for an intrinsically leaky process has been theoretically predicted in [88], which originates from the domain-wall instability leading to spontaneous relaxation in average polarization. Such leaky characteristics has been experimentally demonstrated in an HZO thin-film [97]. Moreover, the polarization leak rate exhibits a dependence on the initial polarization value, which is distinct from the conventional leak rate of first-order system (i.e. RC network). Utilizing such Quasi Leaky (QL) behavior along with the IF characteristics, a Quasi-Leaky-Integration-Fire (QLIF) type FeFET-based neuron was realized [97]. QLIF analysis predicted a reduction in firing rate in SNNs compared to traditional LIF neuron at iso-accuracy.

PhaseFET-based Neurons

By virtue of their abrupt phase transitions, PTMs (and hence PhaseFETs) can potentially be ideal candidates for the implementation of the thresholding function of neurons. In addition, the ability of PTMs to oscillate (see Section 1.5.1) offers an elegant method of generating a train of output spikes where the spiking frequency can be used to encode the data. These features have been used in [54] to design a spiking neuron, as shown in Fig. 1.22(c). Moreover, by biasing the neuron close to the critical voltage for IMT and leveraging the inherent randomness of the phase transition in PTMs, stochasticity in the neuron firing can be achieved. Stochastic neurons have been known to facilitate better generalization by preventing over-fitting of data during training [54]. PhaseFETs offer an ultra-low power hardware solution to design stochastic neurons. It is noteworthy that the PhaseFET only provides the thresholding (or fire) functionality; the leaky integrate functionality is obtained using additional circuitry. In contrast, FeFETs have been shown to exhibit a wide range of unique characteristics the can potentially achieve the LIF with a minimal number of transistors.

1.6 Summary and Conclusions

In this chapter, we presented a systematic overview of the fundamental device physics and the applications of NCFETs and PhaseFETs, given their immense potential to outperform MOSFETs in specific applications where low power con-

sumption is of paramount importance. These devices were first conceptualized to overcome the fundamental physical limits dictated by the Boltzmann tyranny that lead to the unbearable power dissipation in standard MOSFETs, especially at deeply scaled technology nodes.

We presented a theoretical analysis of NCFETs based on the phenomenological Landau theory that describes the negative capacitors as special capacitors with double-well energy landscape. Their unique properties enable a voltage step-up action in the gate stack that, in turn, leads to steep switching. We described the conditions to achieve sub-thermionic switching (i.e., sub-threshold swing lower than the Boltzmann limit of 60 mV/dec at room temperature) for a particular class of NCFETs employing ferroelectrics as a negative capacitance layer. We also provided a comparison of the reliability physics of NCFETs with conventional MOSFETs to outline the advantages and drawbacks of the technology. We finally discussed the advanced issues along with open questions that need to be answered to to fully harness the potential of NCFETs. Similarly, we discussed the theoretical aspects of PhaseFETs, that utilize a phase transition material in series with a conventional transistor to obtain steep-switching. We also outlined their current stage of development (presenting experimental data from the literature).

We also discussed various circuit applications of NCFETs and PhaseFETs. We began by presenting the implications of steep switching and other unique features of NCFETs and PhaseFETs on the performance of Boolean logic and SRAMs, showing delay reduction at iso-energy at low voltages and improvements in stability/noise immunity. In addition to steep-switching, ferroelectric-based transistors offer hysteretic characteristics, which can be highly beneficial for low power non-volatile memory (NVM) designs. In contrast, PhaseFETs cannot be used as NVMs; however, they can be employed to augment MRAMs to improve their read stability and distinguishability. Furthermore, the unique characteristics of FeFETs, NCFETs and PhaseFETs enable low power hardware for non-Boolean computing such as coupled oscillators and neuromorphic primitives. Our discussion points to the importance of understanding the unique device-circuit interactions in these technologies to translate their rich physics into useful circuit functionalities.

Every couple of years or so, new predictions about the demise (and confirmation) of Moore's law are discussed in conferences as well as in the general media. Although we cannot predict with certainty when the final chapter of this very fortunate roadmap will be written, newer devices like NCFETs and PhaseFETs provide researchers with confidence that the ability of mastering new challenges and overcoming the limits of current technology will never completely falter. In this sense, steep-switching devices belong to an exciting novel class of transistors that not only can potentially improve conventional logic switches and semiconductor memories, but also offer advantages to novel applications, as for example to realize Super-Nernstian nano-biosensors [98, 99]. In general, both NCFETs and PhaseFETs pave the way for a brand-new design space for a variety of applications that is yet to be explored, and that we expect will continue to grow in the decades to come.

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1.7 Figures

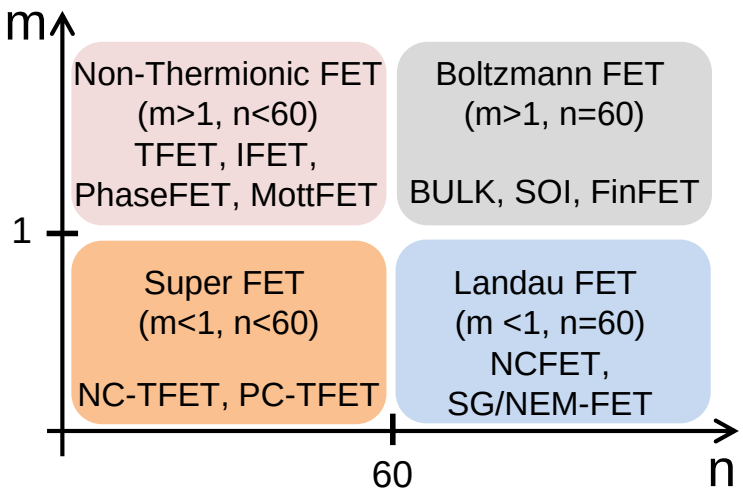

Figure 1.1: Transistors classes in the $m \times n$ space. The NCFET belongs to the Landau switches category, where m is reduced thanks to the stabilized negative capacitance effect. PhaseFET (or MottFET) belong to the Non-Thermionic FET class as they alter the channel transport to achieve $n < 60$

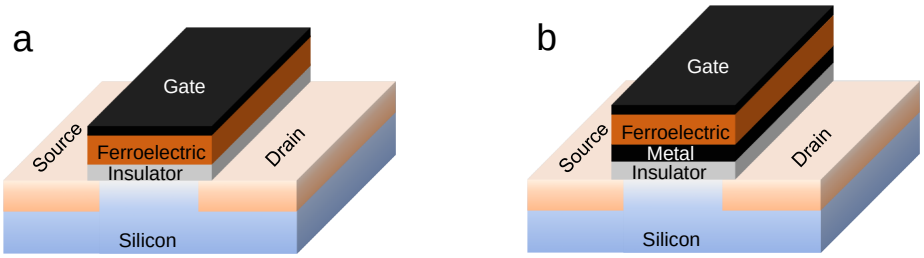

Figure 1.2: Sketch of the NCFETs configurations: (a) MFIS and (b) MFMIS. If stabilized, the ferroelectric layer in the gate stack can provide voltage amplification to reduce sub-threshold slope

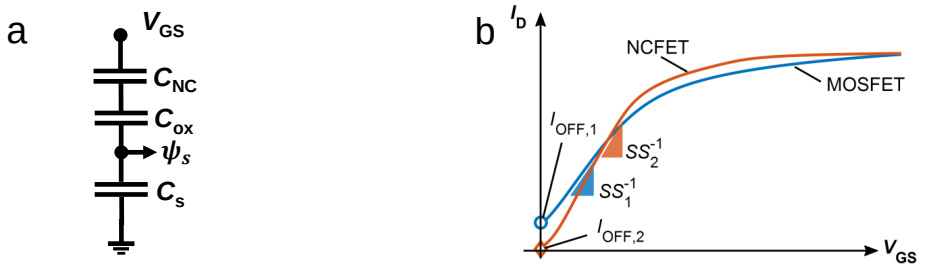

Figure 1.3: (a) Simplified capacitor divider network of the gate stack to illustrate the concept of body-factor m reduction. If a negative capacitance layer is used, such that $C_{NC} < 0$, then $m \equiv \partial V_{GS}/\partial \psi_s < 1$ and SS is reduced. (b) $I_D - V_{GS}$ characteristics of a MOSFET (blue solid line) and NCFET (red solid line) showing that reduced SS leads to reduced I_{OFF} and thus lower power consumption

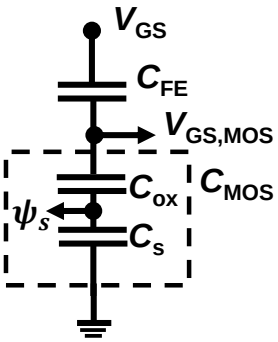

Figure 1.4: Network capacitance for deriving the KVL at the gate-to-source loop. The voltage gain A_V between V_{GS} and $V_{GS,MOS}$ becomes > 1 when C_{FE} is negative and with magnitude close to C_{MOS}

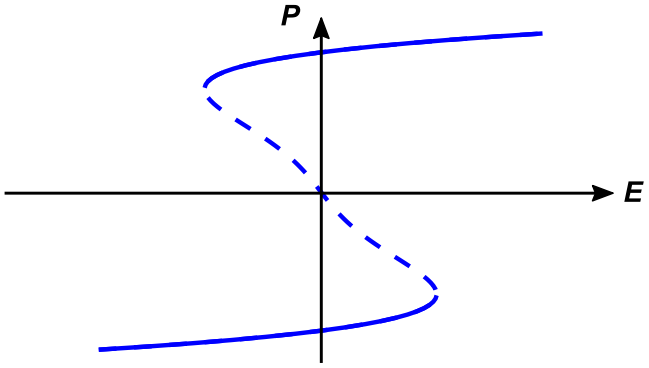

Figure 1.5: $P-E$ loop representing the solution of the time-independent LKE. The parameters chosen are $\alpha = -1.0\times10^{7}\,\mathrm{m/F}$, $\beta = -8.9\times10^{8}\,\mathrm{m^5/F/C^2}$, $\gamma = 4.5\times10^{10}\,\mathrm{m^9/F/C^4}$ are for $BaTiO_3$ [7, 17]. The dashed line represents the part of the loop for which negative capacitance occurs

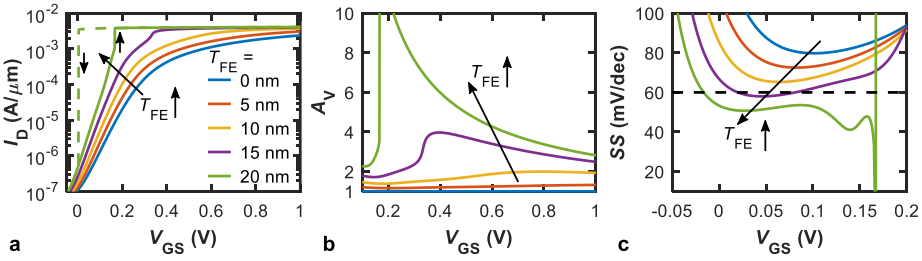

Figure 1.6: (a) $I_D - V_{GS}$ characteristic of a NCFET for different T_{FE} values (see legend). By increasing T_{FE} the voltage gain A_V is increased (b) and at the same time the SS is reduced (c). When $|C_{FE}|$ becomes smaller than C_{MOS} then the total gate capacitance becomes negative (i.e., unstable) and hysteresis starts to appear, as shown in panel (a)

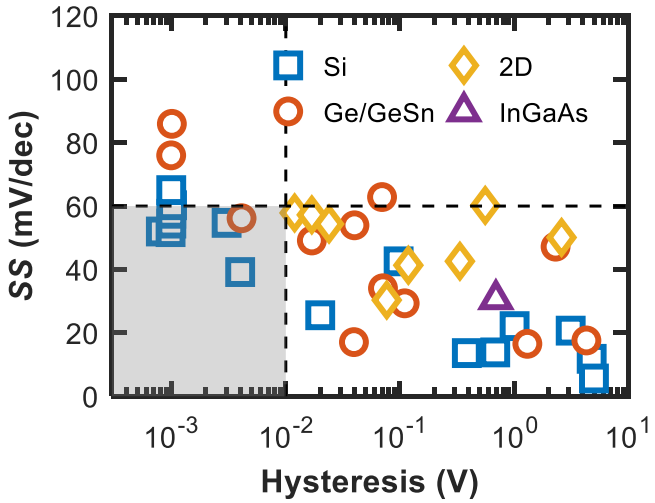

Figure 1.7: Published data of various NCFET experimental data of SS vs hysteresis for different technologies, i.e., Si, Ge/GeSn, 2D and III-V semiconductors. The shaded area represents a 'sweet-spot' for a NCFET with $SS < 60\,\mathrm{mV/dec}$ and moderate hysteresis. Reproduced from [18], with the permission of AIP Publishing

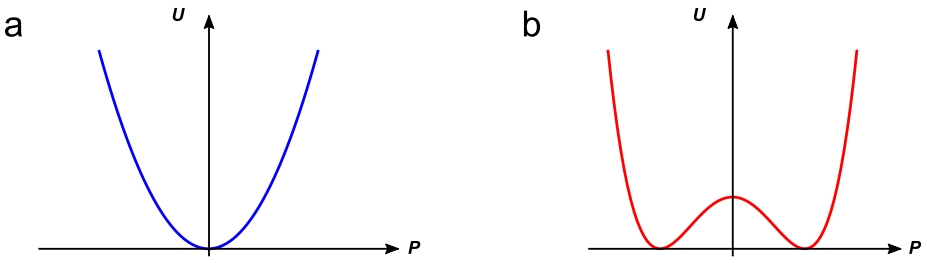

Figure 1.8: Energy landscape plot, $U - P$, of (a) the classical positive capacitor and (b) the negative capacitor. The capacitance is proportional to $\left(\partial U^2/\partial^2 P\right)^{-1}$ thus its sign is defined by the concavity (up, positive and down, negative) of the $U - P$ plot

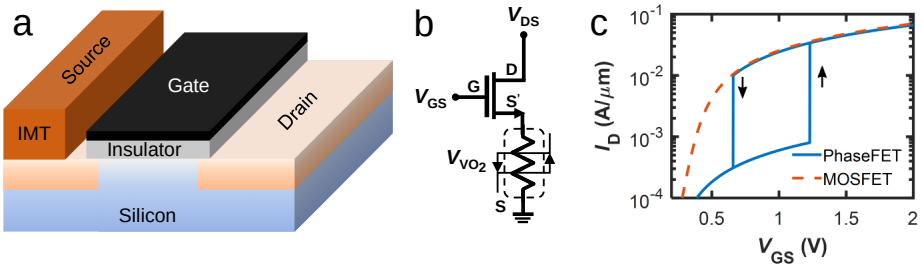

Figure 1.9: (a) Sketch of the PhaseFET cross-section, which consists of a MOSFET with in series to the source a variable resistor undergoing phase transition (PTM). (b) Circuit schematic of the PhaseFET and (c) its $I_D - V_{GS}$ characteristic (blue solid line) compared to that of the standard MOSFET (orange dashed line). The PhaseFET has much better sub-threshold swing than the MOSFET though it exhibits hysteresis

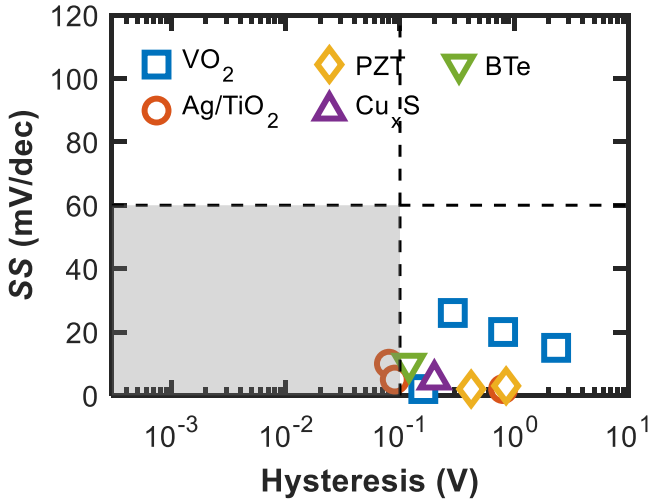

Figure 1.10: Published data of various PhaseFET experimental data of SS vs hysteresis for different variable resistance materials, i.e. VO_2 [5, 11], Ag/TiO_2 [41, 46], PZT [47, 48], Cu_xS [49], and BTe [50]. The shaded area represents a 'sweet-spot' for a PhaseFET with $SS < 60\,\mathrm{mV/dec}$ and moderate hysteresis

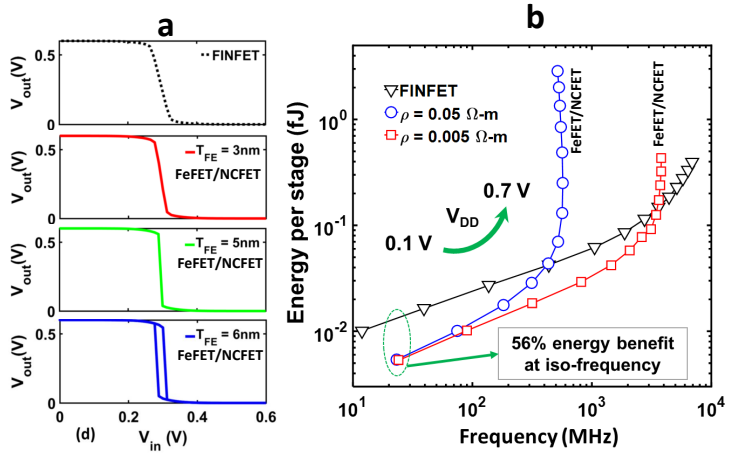

Figure 1.11: (a) Voltage transfer characteristics (VTC) of NCFET inverter for different FE thickness, T_{FE} (from [51] © 2017 IEEE). (b) Energy-Delay for NCFET-based ring oscillator for different ρ

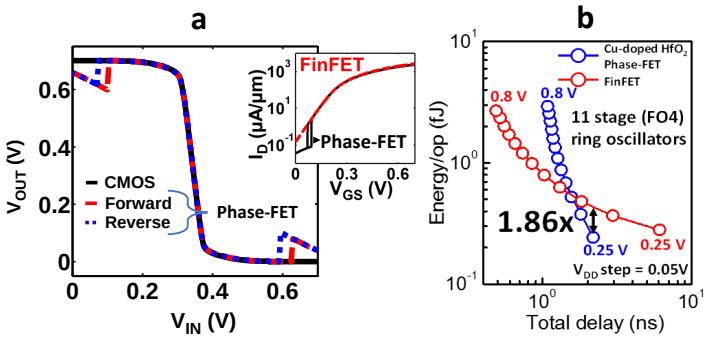

Figure 1.12: (a) Voltage transfer characteristics (VTC) of PhaseFET based inverter. (b) Energy-Delay of PhaseFET based 11 stage ring oscillators (from [55] © 2017 IEEE)

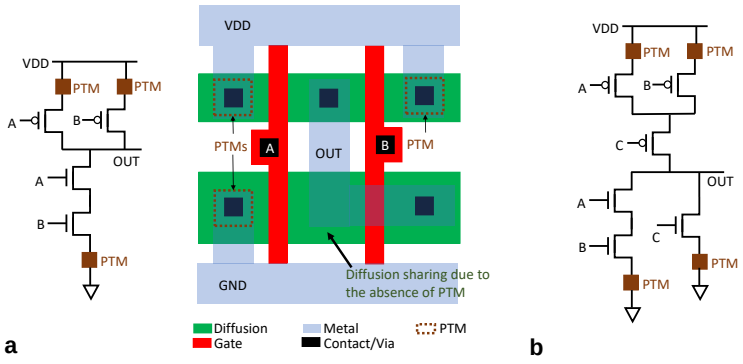

Figure 1.13: (a) Schematic and layout of PhaseFET based 2-input NAND gate and (b) Schematic of PhaseFET based AND-OR-INVERT (AOI) gate, showing one PTM per network of series-connected transistors in the pull-up and pull-down paths

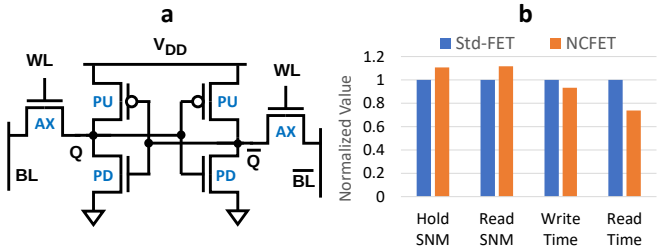

Figure 1.14: (a) SRAM cell showing pull-up (PU), pull-down (PD) and access (AX) transistors. (b) Comparison of performances (Read time and Write time) and stability (Hold SNM and Read SNM) between Std-FET based and NCFET based SRAM cell (from [56] © 2016 IEEE)

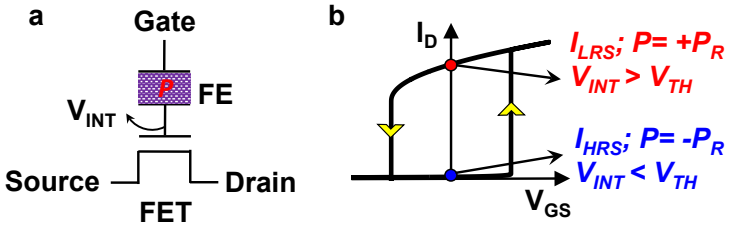

Figure 1.15: (a) Schematic of FeFET with FE integrated in the gate stack of a FET. (b) $I_D - V_{GS}$ characteristics of FeFET illustrating the bi-stability of polarization, P at $V_{GS} = 0\,\mathrm{V}$.

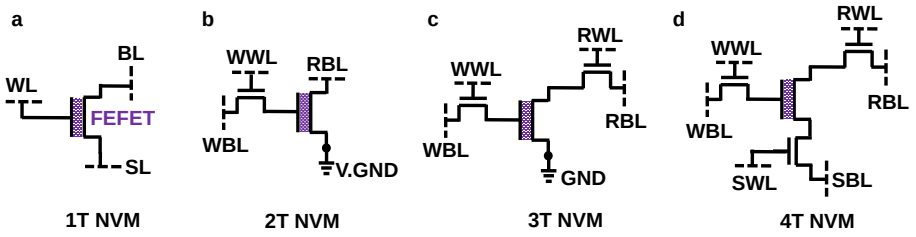

Figure 1.16: (a) 1T, (b) 2T, (c) 3T and (d) 4T FeFET-based non-volatile memory (NVM) designs

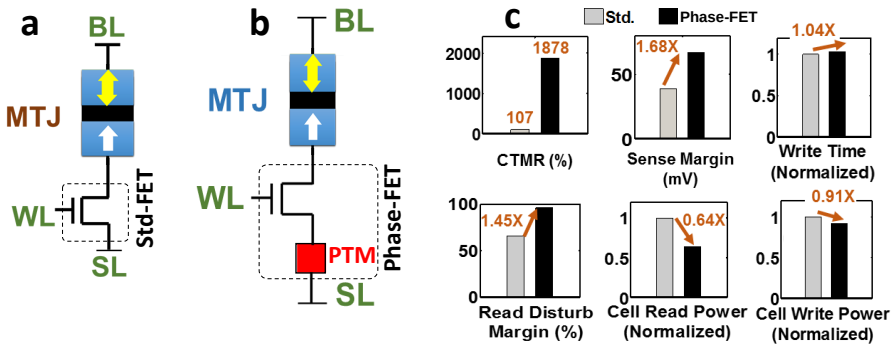

Figure 1.17: Schematics of Magnetic Tunnel Junction (MTJ) NVM cell based on (a) Std-FET and (b) PhaseFET. (c) Comparison of performances and stability between std-FET and PhaseFET based MTJ NVM cell

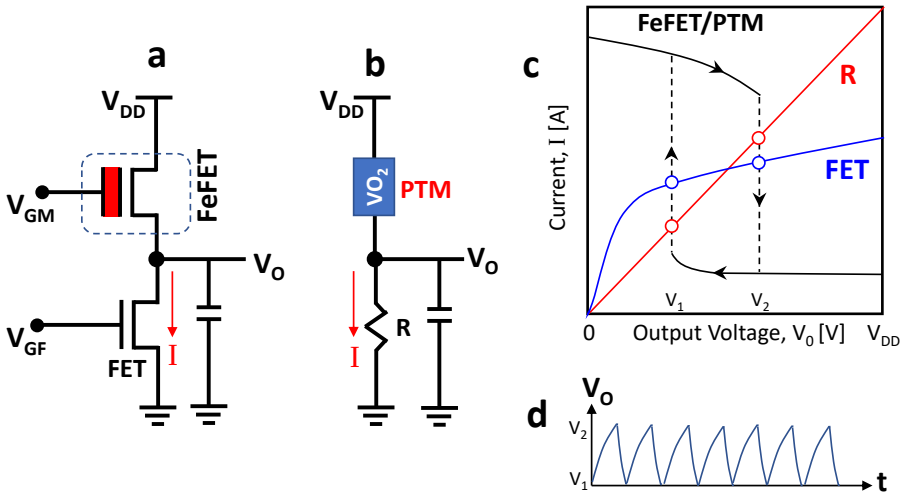

Figure 1.18: Schematics of (a) FeFET-based and (b) PTM (or PhaseFET)-based oscillators. (c) Load-line plot portraying the working principle of the oscillators. (d) Illustration of oscillatory output waveform

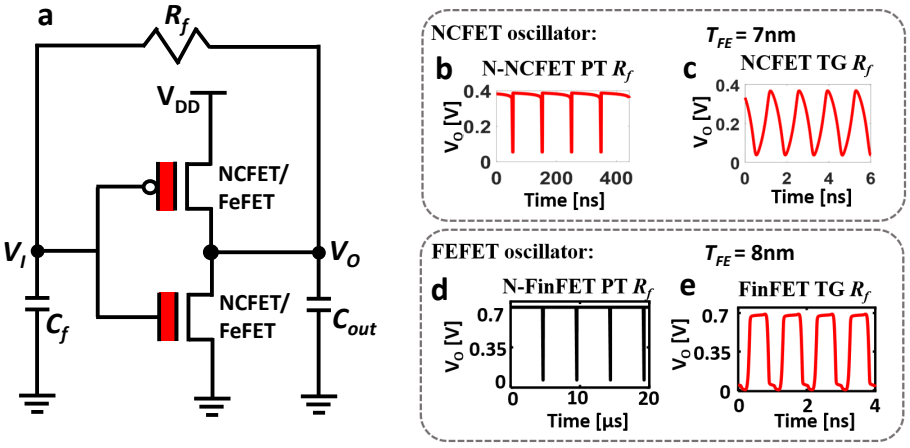

Figure 1.19: (a) Schematic of NCFET/FeFET inverter-based oscillator with a feedback resistor, R_f implemented with pass transistor (PT) or transmission gate (TG). Simulated oscillatory waveform for (b) NCFET oscillator with PT. (c) NCFET oscillator with TG. (d) FeFET oscillator with PT and (e) FeFET oscillator with TG (from [86] © 2019 IEEE)

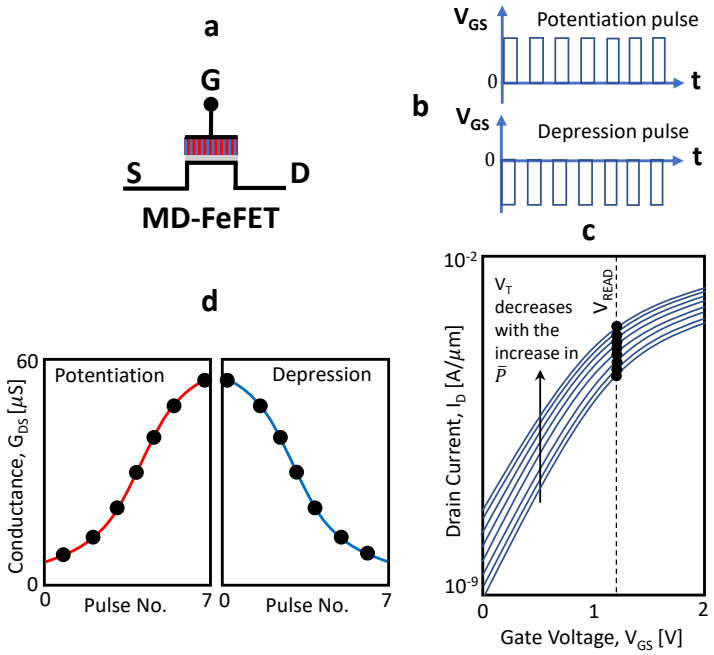

Figure 1.20: (a) FeFET with multiple-domains (MDs) in FE. (b) Voltage pulse scheme for synaptic potentiation and depression. (c) $I_D - V_{GS}$ characteristics of MD-FeFET for different $\bar{P}$ that corresponds to the change in V_T. (d) Synaptic potentiation and depression characteristics of MD-FeFET

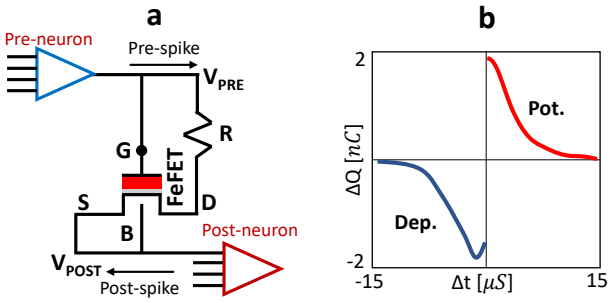

Figure 1.21: (a) Schematic of FeFET-based synapse and the corresponding (b) Spike time dependent plasticity (STDP) pattern

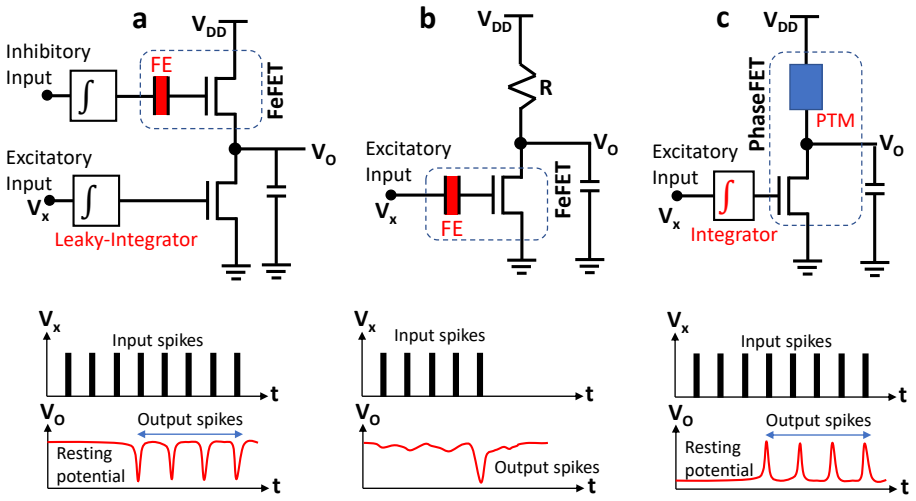

Figure 1.22: Schematics and input-output spiking waveform for (a) 1T-1FeFET neuron, (b) 1R-1FeFET neuron and (c) PhaseFET (1T-1PTM) neuron

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